PowerPC™

IBM

PowerPC 602 Microprocessor

Highlights

Control Unit
- *Dispatches one instruction per cycle*
- *Supports superscalar execution*
- *Branch folding implemented*
- *Retires up to one instruction per cycle*

Load/Store Unit
- *One cycle cache access*
- *Speculative cacheable loads (for no data dependencies)*

Integer Unit
- *One cycle add, subtract, shift, or rotate*
- *Hardware multiply and divide*
- *32 x 32-bit general purpose registers*

Floating-Point Unit
- *IEEE-754 compliant single-precision operations*
- *32 x 32-bit floating point registers*

Cache Unit
- *Separate 4K instruction and data caches, 2-way set associative*
- *3-state coherency protocol*
- *Physically addressed tag and cache arrays*
- *Copy-back or write-thru data cache*
- *Data coherency in hardware*

Memory Management Unit
- *Separate 32-entry instruction and data TLBs*
- *Separate instruction and data BATs (4 each), offer protection and translation for 128K - 4MB of memory*
- *32-bit PowerPC Architecture compliant mode*
- *Additional "protection-only-mode" offers protection of up to 4MB per TLB*

Bus Interface Unit
- *General purpose interface for a wide range of system configurations*
- *Multiplexed 32-bit address and 64-bit data bus*
- *Powerful diagnostic and test interfaces through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface*

Power Management Unit
- *Static low-power design*
- *Dynamic power management*
- *Hardware support for power saving modes*
- *Internal clock multiplier for operation at 2x and 3x of bus clock*

Product Description

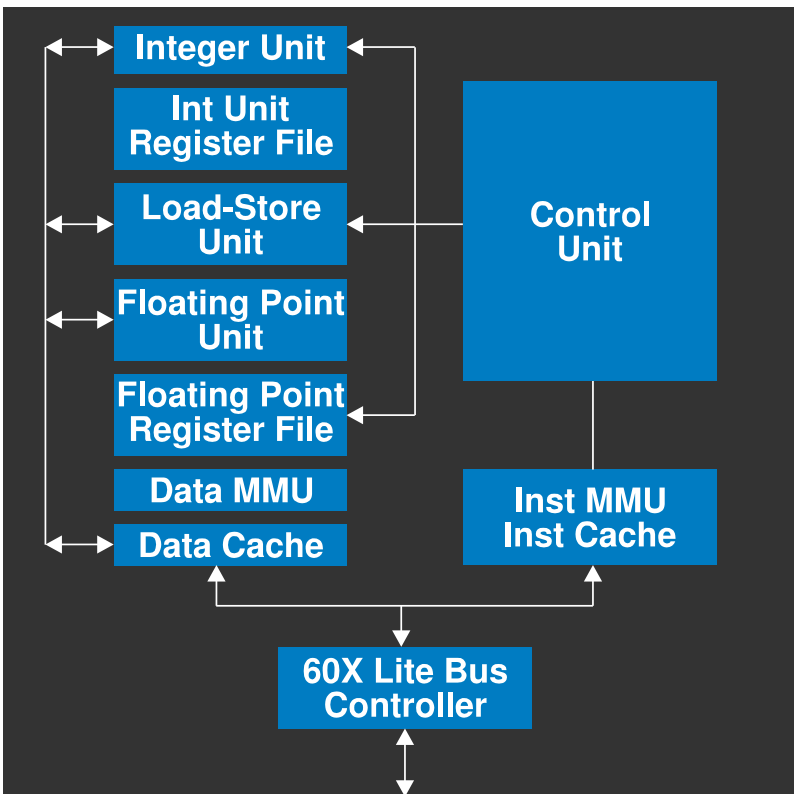
The PowerPC 602* is a 32-bit implementation of the PowerPC* family of Reduced Instruction Set Computer (RISC) microprocessors. It is intended for use in portable and small form factor uniprocessor applications such as PDAs. It achieves its performance through concurrent execution of up to two instructions per cycle in its four parallel execution units: the fixed-point unit, floating point unit, branch processing unit, and the load/store unit. The low-power design of the PowerPC 602 microprocessor, and the power management features it incorporates, offer competitive advantages in performance-oriented, power-sensitive portable applications.

The PowerPC Architecture* is derived from the IBM Performance Optimized With Enhanced RISC (POWER*) architecture. The PowerPC Architecture shares all the benefits of the POWER Architecture*, but is optimized for single-chip implementation. The PowerPC architecture is a major component of the PowerOpen* environment.

The PowerPC Architecture offers a complete range of processor solutions for computing needs from embedded applications through multi-processor mainframe systems. Its unique combination of high performance, wide operating systems applicability, and small die size has resulted in its unprecedented success in the RISC computing market.

Specifications

Technology	0.5µm CMOS, four levels of metal
Die Size	7.04mm x 7.04mm (50 mm^2)
Number of Transistors	~ 1 million
Temperature Range (Tj)	0° C to 105° C
Performance	40 SPECint92 @ 66 MHz (est.) 48 SPECint92 @ 80 MHz (est.)
Signal I/O	98
Power Supply	3.3 V ± 0.3 V
Power Dissipation (typical)	Less than 1200 mW @ 66 MHz, 3.3 W
Packaging	Plastic quad flat pack (144 pins)
Part Number	IBM25EMPPC602-FA-066 IBM25EMPPC602-FA-080



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GK10-3089-01