PowerPC™

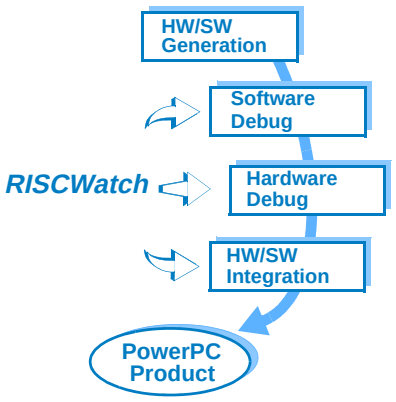
IBM

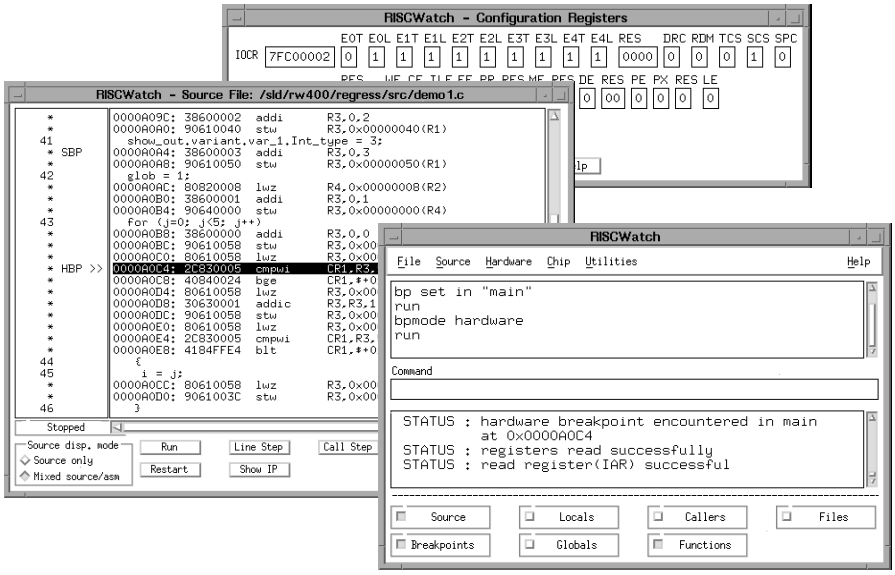
RISCWatch

Debugger for PowerPC Processors

Highlights

- *On-chip debugging via IEEE 1149.1 (JTAG) interface*
- *Target monitor debugging*
- *OS Open Real-Time Operating System aware debugging*
- *Source-level and assembler debugging of C/C++ executables*
- *Real-time trace support via the RISCTrace* feature for the PowerPC 400Series*
- *Network support for remote debugging of the system under development*
- *Supports industry standard Embedded ABI for PowerPC and XCOFF ABI*
- *Command-file support for automated test and command sequences*
- *Simple and reliable 16-pin interface to the system under development*
- *Ethernet to target JTAG interface hardware*
- *Multiple hosts supported*
- *Intuitive and easy-to-use windowed user interface that reduces development time*





Overview

RISCWatch* is a hardware and software development tool for the PowerPC* 600 Family of microprocessors and the PowerPC 400Series of Embedded Controllers. The source-level debugger and processor-control features provide developers with the tools needed to develop and debug hardware and software quickly and efficiently.

Developers who take advantage of RISCWatch are provided a wealth of advanced debug capabilities. Among the advanced features of this full-functioned debugger are: real-time trace, ethernet hardware interface, C++ support, extensive command file support and on-chip debug support. In the future, multi-processing will be supported. All this in a debugger that supports both XCOFF and the Embedded ABI for PowerPC industry standard.

Features

Source and Assembler Debugging

The source and assembler debugger runs in a multi-window environment, enabling improved user productivity. Features include program execution control, stepping, breakpoints, variable viewing/updating, user defined screens and buttons, caller stack and a full set of watch capabilities.

RISCWatch fully supports code debug at both the C/C++ source and assembler levels. Run control functions allow stopping/starting the program, and the ability to restart the program while retaining the setting of current breakpoints and watchpoints. The program can be single-stepped by assembler or C/C++ source line. Function calls can either be stepped into or over as desired.

Breakpoints take full advantage of the debug capability in the PowerPC

processor. In addition to standard trap-based software instruction breakpoints, hardware assisted instruction and data breakpoints are also available. Managing the many types and methods of setting breakpoints is made easy through a single breakpoint control screen.

Assembler level debug is supported in a number of ways. The source screen provides a mixed source/assembler mode which shows each source line and its associated lines of assembler code. An assembler-only screen can also be used to provide actual memory disassembly of the code and the ability to change it dynamically.

Other screens provide the ability to easily navigate through the program during the debug session. A caller's screen allows the program context to be switched between the various levels of the call chain. Files and functions screens provide the ability to decide what files/functions appear in the source window. The functions screen also allows breakpoints to be set or cleared at the beginning of functions. Local and global variable screens not only allow variables to be displayed and updated, they also provide extensive control over what gets shown and when.

On-Chip Debugging

On-chip debugging is accomplished via the IEEE 1149.1 (JTAG) interface, which allows access to the debug logic built into the PowerPC processors. Since the debug logic is separate from the rest of the processor logic, access to processor resources is possible even if the processor is in an error state.

Low-level processor control functions allow the developer complete control of the processor. Processor control features include run, start, step, set breakpoints, reset and initialize the processor. Low-level processor watch functions include displaying and modifying memory, registers, and cache. Memory can also be loaded and disassembled.

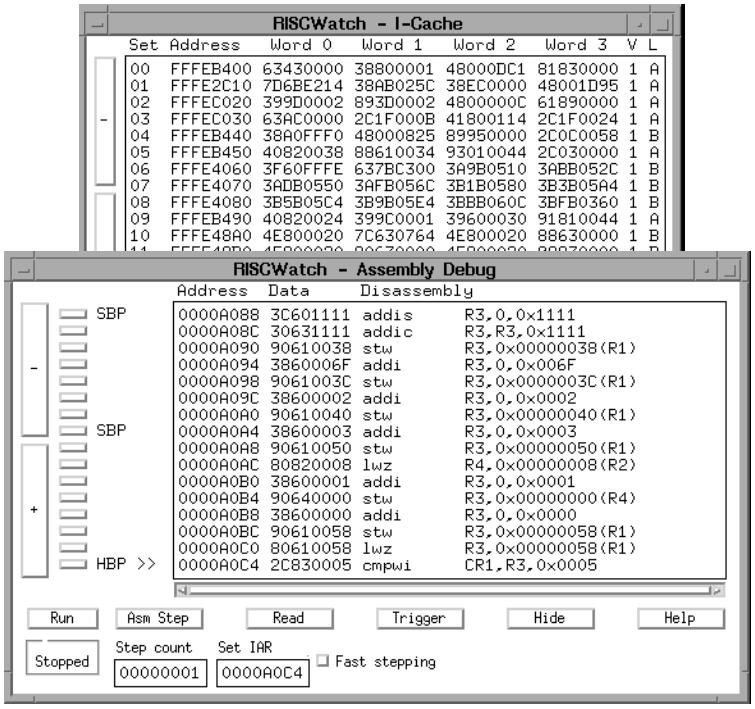
Target Monitor Debugging

RISCWatch has the ability to communicate with target monitor software included in the PowerPC evaluation kit. This communication can take place via a serial (SLIP) or ethernet (TCP/IP) connection.

Additionally, custom target monitors can easily be created using the available board support debug libraries. Combined with the connection options, this provides the ability to extend the powerful software debug capabilities of RISCWatch to custom board solutions.

Operating System Support

RISCWatch supports task level debugging for users of the OS Open Real-Time Operating System from IBM. RISCWatch assists OS Open application developers by displaying task-sensitive debug information.



User Interface

The user-friendly multi-windowed user interface provides an extensive set of predefined screens, pulldowns and utilities. All are designed to present complete representation and control of the system under development. Some screens also allow the user to customize the data being presented. For example, the developer can choose which variables are to be shown, the update policy for variable refresh, the data representation, and the attributes to display (address, type, and size).

RISCWatch supports even more detailed user interface customization by providing user-defined screen capabilities. They allow the developer to easily build custom screens and buttons that contain resources and control facilities of particular interest to a specific debugging task. This enhances productivity by increasing the ability to readily see key pieces of information and directing host processor activity to only those functions.

Command File Support

Command files allow test cases to be written off-line and then run automatically. Command files can also be used for running regression tests, initializing the processor, and automating command sequences.

The rich command file language provides program flow control commands like if-then-else, while, and do-while. Special expressions indicating the processor state and other error conditions are also provided. A command file single-step capability is provided to aid in command file development.

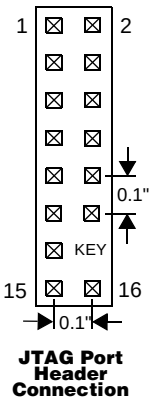
Processor Specific On-Line Help

RISCWatch provides extensive on-line help. Most windows contain a help button to display context sensitive help. A help window with a search option can also be displayed. Help topics include command syntax, processor instruction sets and registers, and field definitions.

RISCTrace

RISCTrace* is a RISCWatch feature that takes advantage of the trace capabilities in the PowerPC 400 family processors, providing a totally non-intrusive reconstruction of application code execution flow. Trace information is collected from the trace status port in real-time and then used with the contents of processor memory to reconstruct program flow. This applies whether the code is running out of the instruction cache or memory.

Processor Interface Assembly Connections to a PowerPC JTAG Port



JTAG Port Header Connection

Header Pin # and I/O		Processor Signal	601 [1]	602 [1]	603 [1]	604 [1]	403GA 403GC	403GB	Board Resistor [2]
1	Out	TDO		28	198	248	16	12	
		SCAN_OUT	78						
2		NC							
3	In	TDI				250	8	13	10KΩ PU
		SCAN_SIN	186	24	199				1KΩ PD
4	In	$\overline{\text{TRST}}$		27	202	253			10KΩ PU
		$\overline{\text{ESP\_EN}}$	275						10KΩ PU
5	Out	RUN_NSTOP	74						10KΩ PU
6		+POWER [3]							1KΩ SR [4]
7	In	TCK		26	201	252	6	18	10KΩ PU
		SCAN_CLK	187						10KΩ PU
8		NC							
9	In	TMS		25	200	251	7	21	10KΩ PU
		SCAN_CTL	184						10KΩ PU
10		NC							
11	In	$\overline{\text{SRESET}}$ [6]	264	10	189	236			10KΩ PU
		HALT					9	22	10KΩ PU
12		NC							
13	In	$\overline{\text{HRESET}}$ [6]	279	9	214	265			10KΩ PU
14		KEY							
15	Out	$\overline{\text{CHECKSTOP}}$			216				10KΩ PU
		$\overline{\text{CKSTP\_OUT}}$	72	3		267			10KΩ PU
16		GND							
	In	RESUME	277						1KΩ PD
	In	$\overline{\text{QACK}}$ [5]		142	235				1KΩ PD
		$\overline{\text{SYS\_QUIESC}}$	260						1KΩ PD
	In	L2_TEST_CLK				254			10KΩ PU
	In	L1_TEST_CLK				255			10KΩ PU
	In	$\overline{\text{LSSD\_MODE}}$				256			10KΩ PU
	In	ARRAY_WR				271			10KΩ PU

1 Pin numbers for PQFP package

2 PU = pullup, PD = pulldown, SR = series

3 The +POWER signal is sourced from the target development board and is used as a reference signal. It should be the power signal being supplied to the processor (either +3.3V or +5V). It does not supply power to the RISCWatch hardware.

4 This series resistor provides short circuit current-limiting protection only. If present, it should be 1K ohm or less.

5 If the target development board does not use this signal, the board must have a 1K ohm pulldown resistor connected to this pin. This signal allows the processor to enter the soft stop state.

6 The $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{TRST}}$ signals from the RISCWatch Processor Interface Assembly connector must be logically ORed with the $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{TRST}}$ signals that connect to the target on the target development board. They cannot be "dotted" or "wire-ORed" on the board. In addition, the ORed signals should only reset the processor and no other devices on the target board.

A screen is provided to allow control and management of events that can initiate the trace collection activity. Essentially, any or all of the PowerPC 400 family processor debug events can be used to trigger the trace event.

Target Connections

IEEE 1149.1 (JTAG)

A 16-pin male 2x8 header connector must be available on the target development board. This connector links the RISCWatch Processor Interface Adapter to the target development board's PowerPC processor JTAG port, using the connections described in the above table.

There is a high-performance ethernet processor probe that supports both the 400Series and 600 family of PowerPC processors.

To ensure JTAG signal integrity, the header connector should be placed as close as possible to the processor socket. Its 2x8 pin array is shown above next to the table. Note that position 14 is not a pin. It is used as a key.

RS-232 Serial and 10base2 Ethernet

RISCWatch supports standard RS-232 and 10base2 ethernet connections to the target development board, in the ROM Monitor mode.

RISCTrace Status

A 20-pin male 2x10 header connector is suggested for connecting to the RISCTrace Status Port. This connector definition matches the requirements of the RISCTrace feature of RISCWatch 400. There are seven (7) Trace Status signals, TS0 – TS6, which are active high outputs from the 403GA and GC processors. They are designed to be sampled on the rising edge of the processor clock. To ensure signal integrity, the connector should be placed as close to the processor as possible.

Chips Supported

- PowerPC 600 Family of Microprocessors
- PowerPC 400Series of Embedded Controllers

Technical Support

- Documentation
- Phone/fax/email links
- Maintenance services

Host Platform Requirements

RISC System/6000 and Sun

Hardware:

- RS/6000* or PowerPC, or Sun SPARCstation** 5, 10, or 20
- One 3.5” diskette drive
- 3 MB hard disk space (3 MB additional during installation)
- Requires 10base2 or 10baseT ethernet connection
- May require AUI cable and an IEEE 802.3 10base2 network transceiver

Software (RS/6000)

- AIX* Version 3.2.5 or later
- AIX/Windows with X11R5 and Motif 1.2

Software (Sun)

- SunOS** 4.1.3 (or later) or Solaris 2.3 (or later)
- OpenWindows** 3.0 (SunOS 4.1.3) or 3.3 (Solaris** 2.3)

IBM compatible PC

Hardware

- IBM compatible PC 486DX2 (50 MHz) or better, and 8 MB RAM
- One 3.5” diskette drive
- VGA/SVGA display (minimum 640 x 480)
- 3 MB hard disk space (3 MB additional during installation)
- Requires 10base2 or 10baseT ethernet connection

Software

- Microsoft Windows** 3.1 or Windows 95**
- A TCP/IP suite compliant with the Microsoft Windows Socket API will be needed.

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