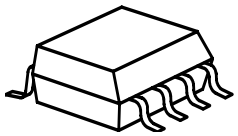
Single-Wire-Transceiver TLE 6259

Target Data Sheet

1 Overview

1.1 Features

- Single-wire transceiver, suitable for **LIN** protocol
- Transmission rate up to 20 kBaud
- Compatible to LIN specification
- Compatible to ISO 9141 functions
- Very low current consumption in sleep mode
- Control output for voltage regulator
- Short circuit proof to ground and battery
- Overtemperature protection



P-DSO-8-3

Type	Ordering Code	Package
TLE 6259 G	on request	P-DSO-8-3

Description

The single-wire transceiver TLE 6259 is a monolithic integrated circuit in a P-DSO-8-3 package. It works as an interface between the protocol controller and the physical bus. The TLE 6259 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

In order to reduce the current consumption the TLE 6259 offers a sleep operation mode. In this mode a voltage regulator can be controlled in order to minimize the current consumption of the whole application. A wake-up caused by a message on the bus enables the voltage regulator and sets the RxD output low until the device is switched to normal operation mode.

The IC is based on the Siemens Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuit.

The TLE 6259 is designed to withstand the severe conditions of automotive applications.

1.2 Pin Configuration (top view)

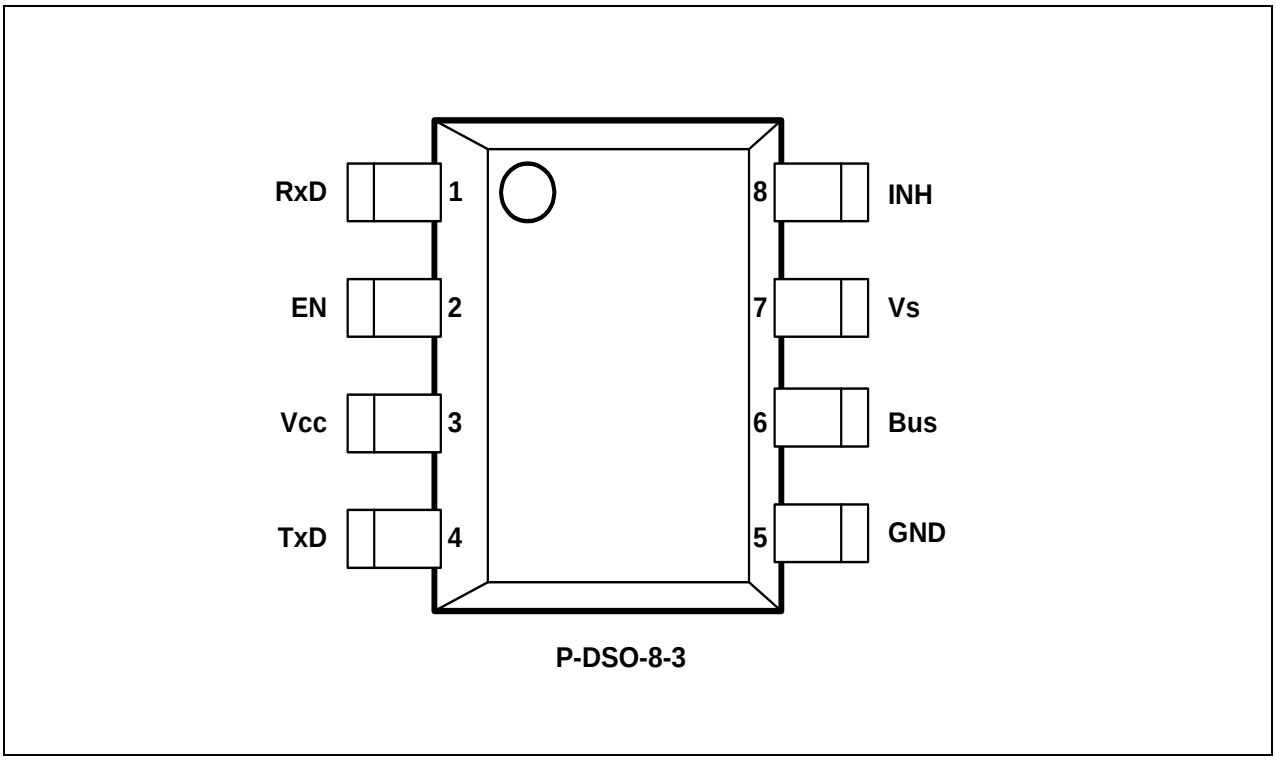


Figure 1

1.3 Pin Definitions and Functions:

Pin No.	Symbol	Function
1	RxD	**Receive data output;** integrated pull up, LOW in dominant state,
2	EN	**Enable input;** integrated 30 kΩ pull down, transceiver in normal operation mode when HIGH
3	V_{CC}	**5V supply input;**
4	TxD	**Transmit data input;** integrated pull up, LOW in dominant state
5	GND	**Ground;**
6	Bus	**Bus output/input;** internal 30 kΩ pull up, LOW in dominant state
7	Vs	**Battery supply input;**
8	INH	**Inhibit output;** to control a voltage regulator, becomes HIGH when wake-up via LIN bus occurs

1.4 Functional Block Diagram

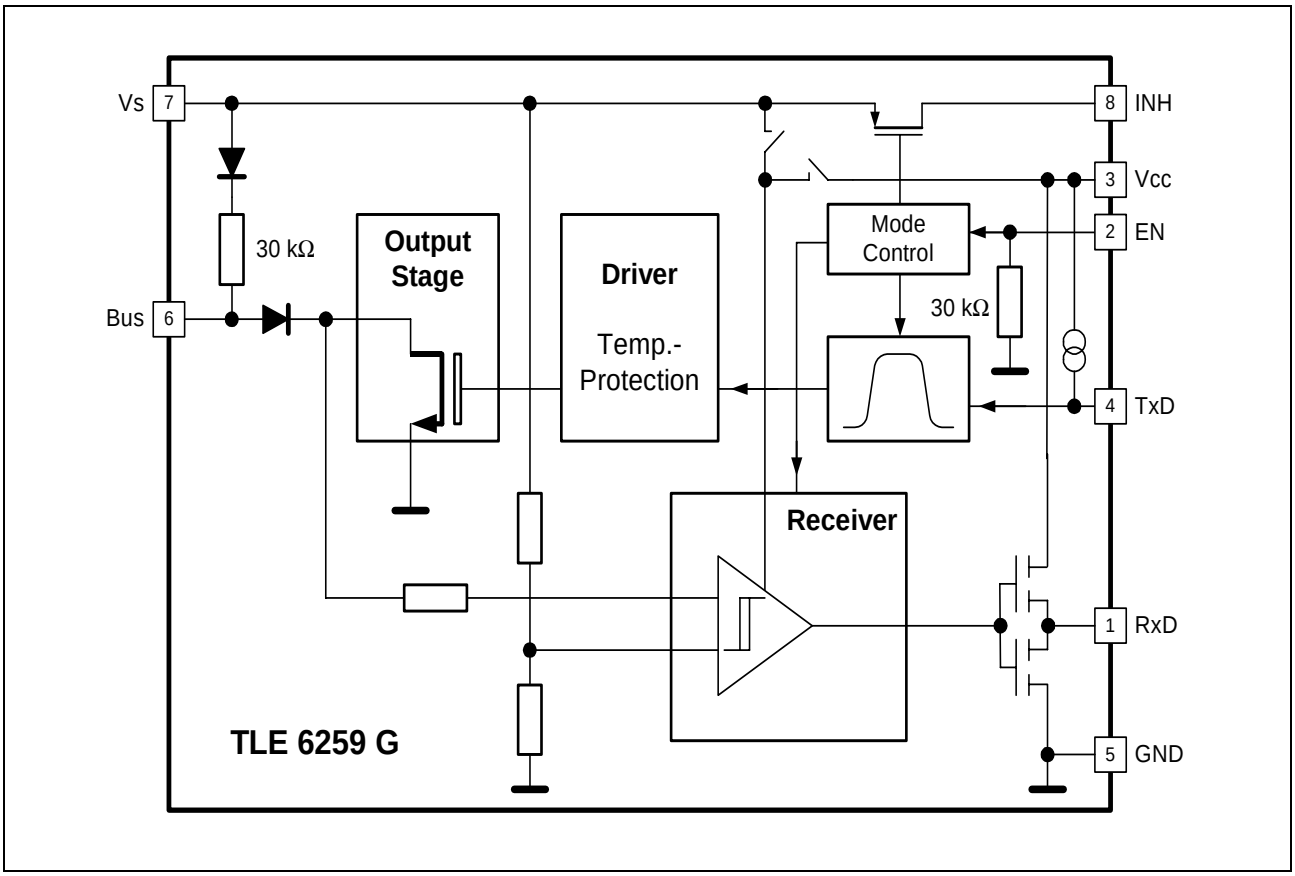


Figure 2

1.5 Application Information

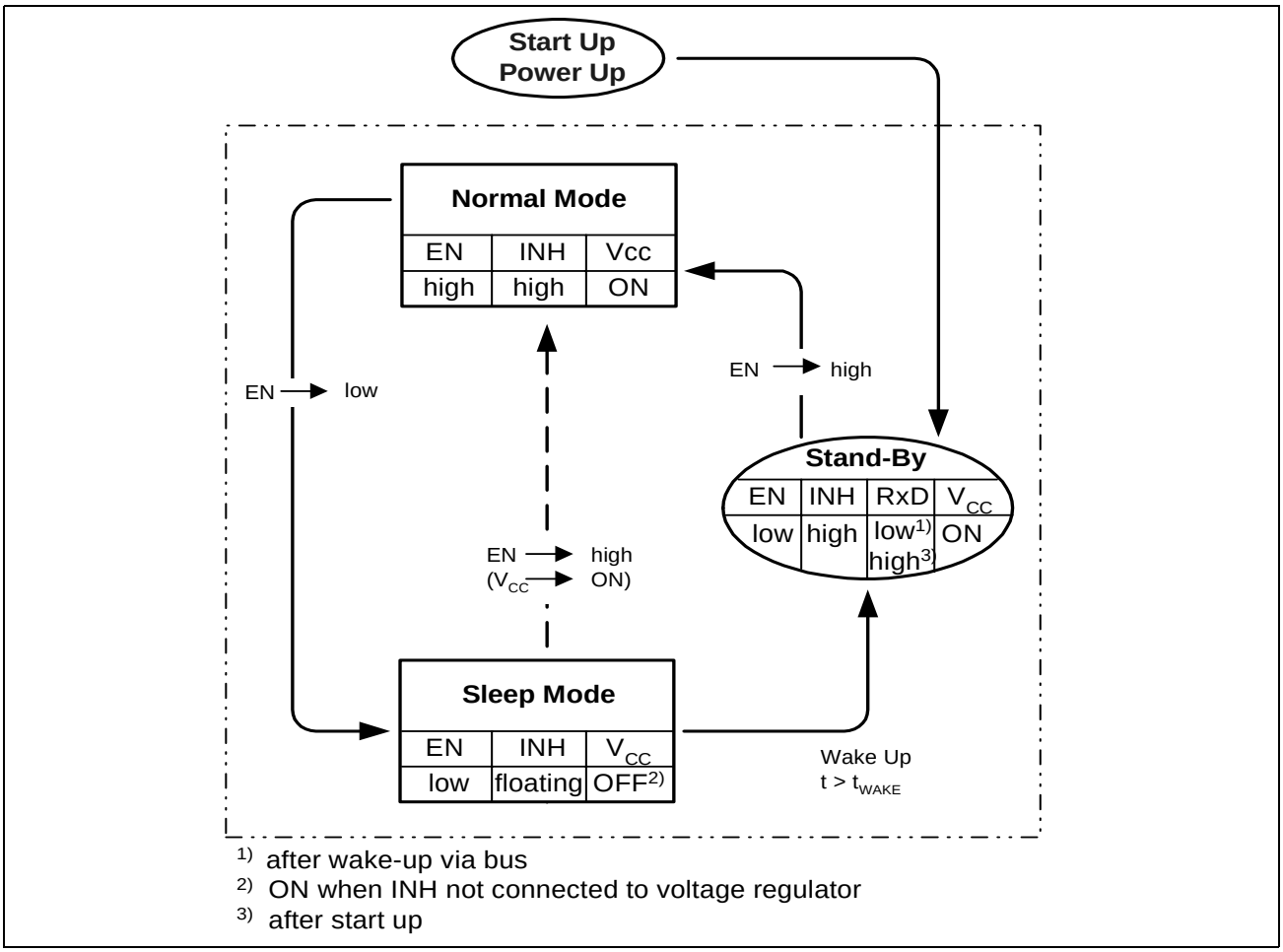


Figure 3: operation mode state diagram

For fail safe reasons the TLE6259 has already a pull up resistor of 30kΩ implemented. To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1kΩ is required. It is recommended to place this resistor in the master node. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is recommended to place a diode in series to the external pull up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1nF in the master node (see figure 6, application circuit).

An capacitor of 10µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

In order to reduce the current consumption the TLE 6259 offers a sleep operation mode. This mode is selected by switching the enable input EN low (see figure 3, state diagram).

In the sleep mode a voltage regulator can be controlled via the INH output in order to minimize the current consumption of the whole application. A wake-up caused by a message on the communication bus automatically enables the voltage regulator by switching the INH output high. In parallel the wake-up is indicated by setting the RxD output low. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

In case the voltage regulator control input is not connected to INH output or the microcontroller is active respectively, the TLE6259 can be set in normal operation mode without a wake-up via the communication bus.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_{CC}	-0.3	6	V	
Battery supply voltage	V_S	-0.3	40	V	
Bus input voltage	V_{bus}	-20	32	V	
Bus input voltage	V_{bus}	-20	40	V	t < 1 s
Logic voltages at EN, TxD, RxD	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_{CC} < 5.5 V
Input voltages at INH	V_{INH}	-0.3	V_S + 0.3	V	
Output current at INH	I_{INH}		1	mA	
Electrostatic discharge voltage at Vs, Bus	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

2.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	4.5	5.5	V	
Battery Supply Voltage	V_S	6	20	V	
Junction temperature	T_j	– 40	150	°C	–

Thermal Shutdown (junction temperature)

Thermal shutdown temp.	T_{jSD}	150	170	190	°C
Thermal shutdown hyst.	ΔT	–	10	–	K

Thermal Resistances

Junction ambient	$R_{thj\text{-}a}$	–	185	K/W	–

2.3 Electrical Characteristics

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Current Consumption						
Current consumption	I_{CC}		0.5	1.5	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	I_S		0.5	1.0	mA	recessive state; $V_{TxD} = V_{CC}$
Current consumption	I_{CC}		0.7	2.0	mA	dominant state; V_{TxD} = 0 V
Current consumption	I_S		0.7	1.5	mA	dominant state; V_{TxD} = 0 V
Current consumption	I_S		20	30	µA	sleep mode; T_j = 25 °C
Current consumption	I_S		20	40	µA	sleep mode
Receiver Output R×D						
HIGH level output current	$I_{RD,H}$		-0.7	-0.4	mA	V_{RD} = 0.8 x V_{CC},
LOW level output current	$I_{RD,L}$	0.4	0.7		mA	V_{RD} = 0.2 x V_{CC},
Bus receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 x V_S	0.48 x V_S		V	-8 V < V_{bus} < $V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$		0.52 x V_S	0.56 x V_S	V	$V_{bus,rec}$ < V_{bus} < 20 V
Receiver hysteresis	$V_{bus,hys}$	0.02 x V_S	0.04 x V_S	0.06 x V_S	mV	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$
wake-up threshold voltage	V_{wake}	0.40 x V_S	0.55 x V_S	0.70 x V_S	V	
Transmission Input T×D						
HIGH level input voltage threshold	$V_{TD,H}$		2.9	0.7 x V_{CC}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	300	600		mV	

2.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
LOW level input voltage threshold	$V_{TD,L}$	0.3 x V_{CC}	2.1		V	dominant state
TxD pull up current	I_{TD}	-150	-110	-80	µA	V_{TxD} < 0.3 Vcc
Bus transmitter						
Bus recessive output voltage	$V_{bus,rec}$	0.9 x V_S		V_S	V	V_{TxD} = V_{CC}
Bus dominant output voltage	$V_{bus,dom}$	0		1.5	V	V_{TxD} = 0 V;
Bus short circuit current	$I_{bus,sc}$	40	85	125	mA	$V_{bus,short}$ = 13.5 V
Leakage current	$I_{bus,lk}$	-350	-100		µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = -8 V, T_j < 85 °C
			5	20	µA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = 20 V, T_j < 85 °C
Bus pull up resistance	R_{bus}	20	30	47	kΩ	
Enable input (pin EN)						
HIGH level input voltage threshold	$V_{EN,on}$		2.8	0.7 x V_{CC}	V	normal mode
LOW level input voltage threshold	$V_{EN,off}$	0.3 x V_{CC}	2.2		V	low power mode
EN input hysteresis	$V_{EN,hys}$	300	600		mV	
EN pull down resistance	R_{EN}	15	30	60	kΩ	
Inhibit output (pin INH)						
HIGH level drop voltage $\Delta V_{INH} = V_S - V_{INH}$	ΔV_{INH}		0.5	1.0	V	I_{INH} = - 0.15 mA
Leakage current	$I_{INH,lk}$	- 5.0		5.0	µA	sleep mode; V_{INH} = 0 V

2.3 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 6.0 V < V_S < 20 V; R_L = 1 kΩ; V_{EN} > $V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Dynamic Transceiver Characteristics						
falling edge slew rate	$S_{bus(L)}$	-3	-2.0	-1	V/µs	80% > V_{bus} > 20% C_{bus}= 3.3 nF; $T_{ambient}$ < 85 °C; V_{CC} = 5 V; V_S = 13.5 V
rising edge slew rate	$S_{bus(H)}$	1	1.5	3	V/µs	20% < V_{bus} < 80% C_{bus}= 3.3 nF; V_{CC} = 5 V; V_S = 13.5 V
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{d(L),TR}$	2	5	10	µs	C_{bus} = 3.3nF; V_{CC} = 5 V; V_S = 13.5 V C_{RxD} = 20 pF
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{d(H),TR}$	2	5	10	µs	C_{bus} = 3.3 nF; V_{CC} = 5 V; V_S = 13.5 V C_{RxD} = 20 nF
Propagation delay TxD LOW to bus	$t_{d(L),T}$		1	4	µs	V_{CC} = 5 V
Propagation delay TxD HIGH to bus	$t_{d(H),T}$		1	4	µs	V_{CC} = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$		1	4	µs	V_{CC} = 5V; C_{RxD} = 20pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$		1	4	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Receiver delay symmetry	$t_{sym,R}$	-2		2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$
Transmitter delay symmetry	$t_{sym,T}$	-2		2	µs	$t_{sym,T} = t_{d(L),T} - t_{d(H),T}$
Wake-up delay time	t_{wake}	30	100	200	µs	

3 Diagrams

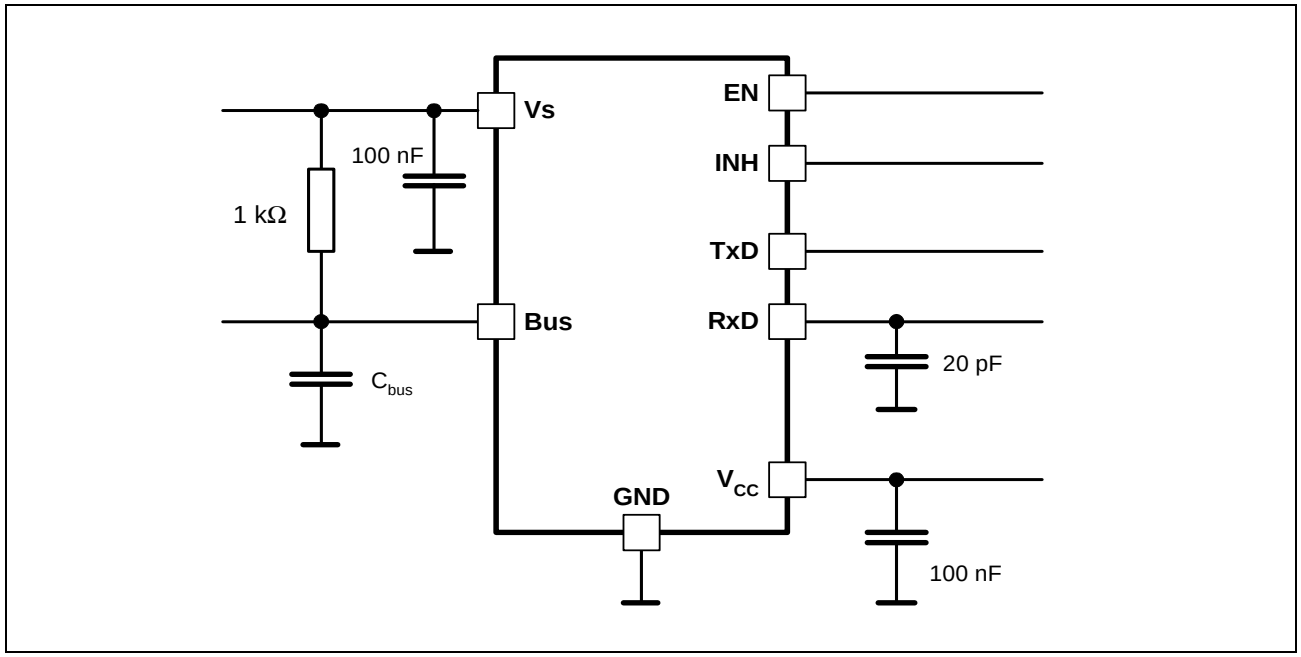


Figure 4: Test circuits

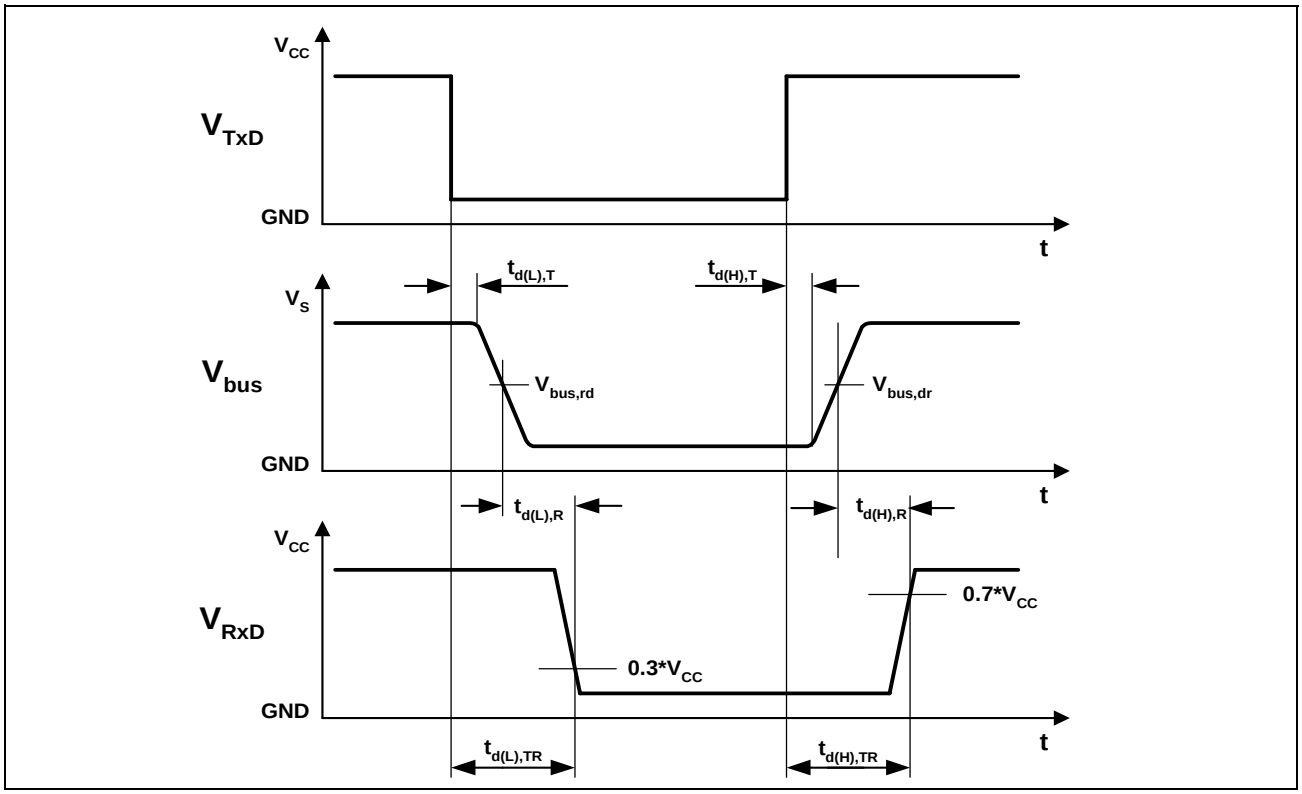


Figure 5: Timing diagrams for dynamic characteristics

4 Application

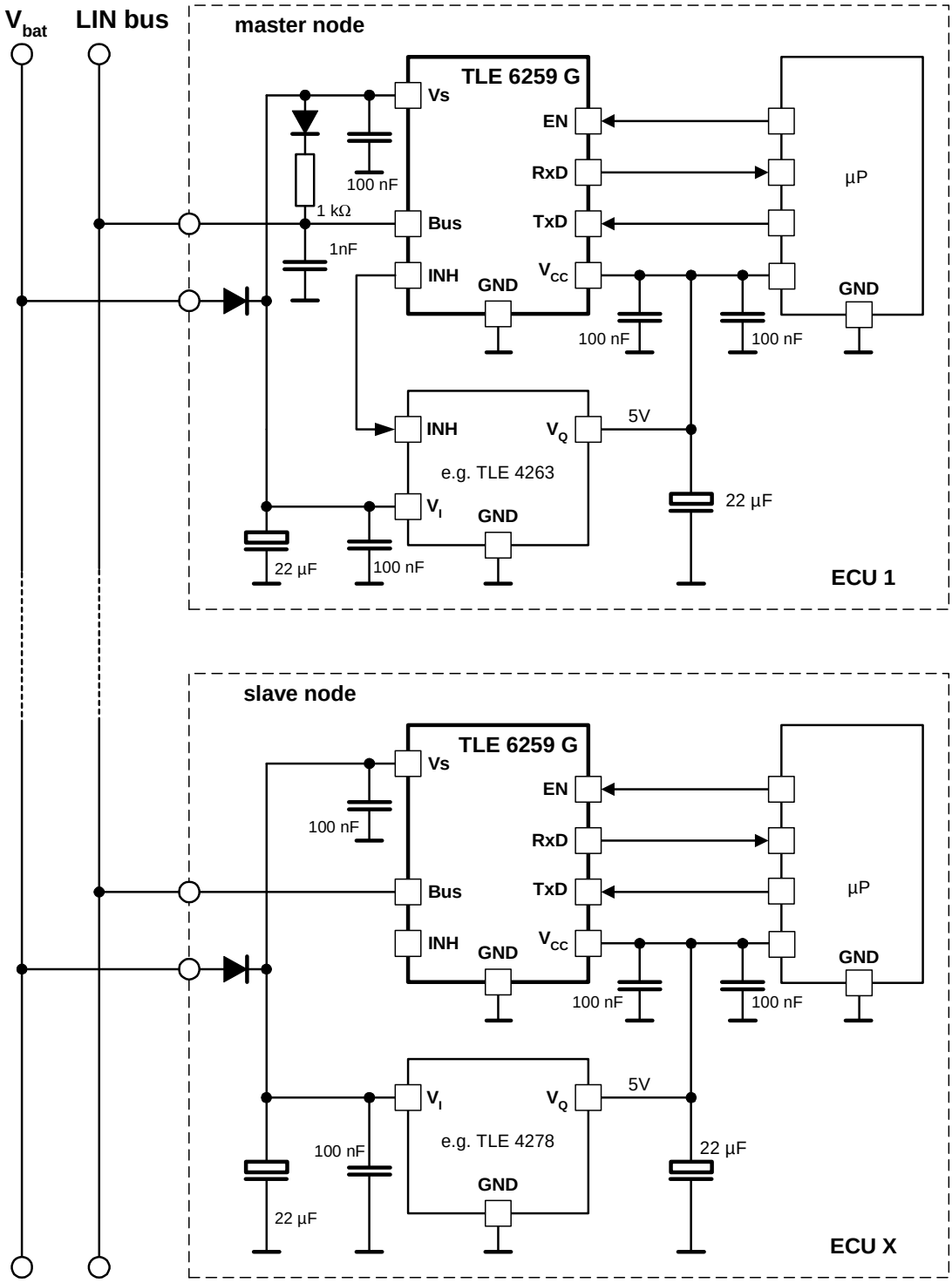
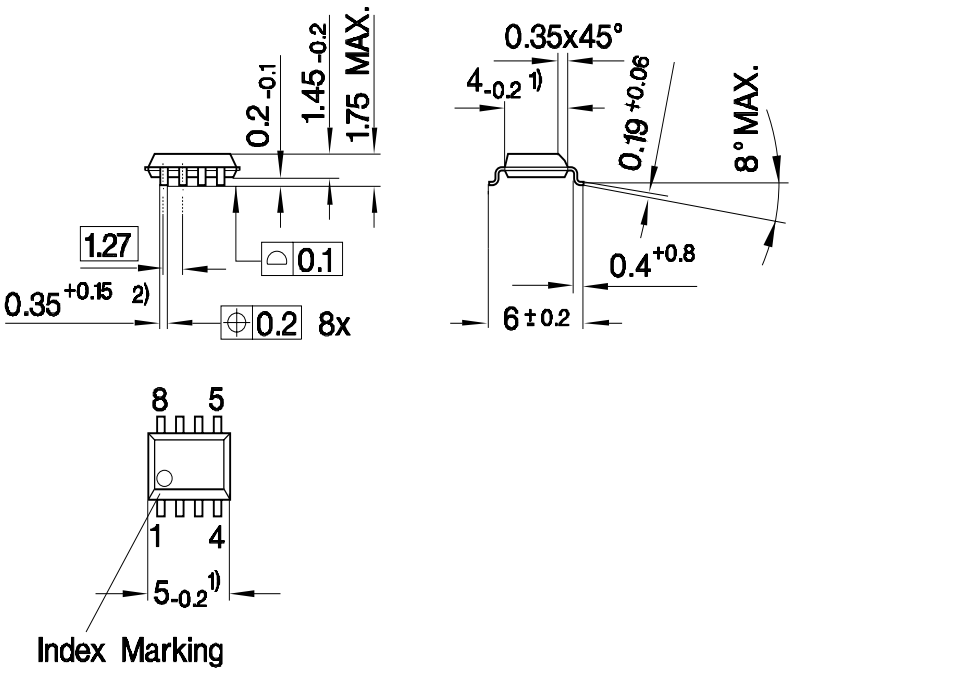


Figure 6
Application Circuit

5 Package Outlines

P-DSO-8-3
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

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Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Edition 1999-10-12

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