Printed Circuit Board Design Guidelines for Ball Grid Array Packages

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Abstract

This paper is a printed wiring board layout guide for designing system cards which incorporate ball grid array packages. The differences in designing for plastic and ceramic ball grid arrays is emphasized as well as wiring patterns for reducing the number of circuit board layers.
The capability and limits of routing wires on two signal layers for several array sizes and circuit board layout rules are shown. Routing of several products in ball grid array packages is shown also.

Introduction

Ball grid arrays enable integrated circuit chips to exceed the lead count beyond quad flat pack limitations. Some microprocessor I/O already exceed the limitations of a quad flat package. One such example is the PowerPC 620™ microprocessor which is packaged in a 624 lead Ceramic Ball Grid Array.
Quad flat packs are limited to about 376 pins total. JEDEC registration documents allow standards for Ball Grid Array lead counts as high as 2401.

This paper addresses the printed circuit board design issues surrounding the use of ceramic and Plastic Ball Grid Array packages.

Incoming material requirements

Standard FR-4 laminate printed wiring board (PWB) material with a glass transition temperature exceeding 115°C ($T_g \geq 115°C$) is a minimum requirement. The coefficient of thermal expansion (CTE) is recommended to be industry typical of 16 to 18 ppm.
The PWB flatness may be flat within industry standards which is approximately 10 microns (µm) per mm (10 mils per inch).

The recommended solder mask and outer metal configuration is a solder mask over bare copper (SMOBC) board. A SMOBC board is preferred because the polymer mask on the copper prevents solder deposited on the pads from migrating away, typically into a nearby via.

The final metal coatings on the board can be of several types. Perhaps the two most common types are the hot air solder leveled (HASL) finish and copper pads treated with a benzotriazole (BTA) based coating, the latter being used often in PWB designs that include fine pitch Quad Flat Packs (QFP's). Electroless gold over nickel may also be used but the gold volume must not exceed the maximum amount that leads to solder joint embrittlement.

Solder pad designs

The basis for a successful design is the copper solder pad site. Figure 1 shows the design features associated with one solder site. Table 1 lists dimensions of the features highlighted in Fig.1.

Two pad types may be used. The first type defines the solder joint by an opening in the solder mask over the copper pad, a" Solder Mask Defined" pad (SMD). The other pad type is called "Non Solder Mask Defined" (NSMD), which is defined by the diameter of the copper pad. The solder mask is larger than the copper pad. The non solder mask design is preferred over solder mask defined because its smaller pad allows more space for wiring traces between the pads.

Paste Mask Dimensions

The recommended solder paste mask openings for each pad type are listed in Table 1. Paste mask openings for all BGA's are rather large and forgiving to the paste deposition process compared to fine pitch perimeter leaded packages. The paste mask openings are typically the same size as the solder pad site on the PWB for PBGA designs. CBGA designs, however use a paste mask opening 2 mils larger in diameter than the PWB pad. the extra solder increases the reliability of the joints.

Top Surface Feature Dimensions

Figure 2 shows traces passing between the outer solder pads of an array. Table 2 shows the relation of pad size, pad pitch and maximum allowable line widths for one, two or three lines between the pads of Figure 2. For example a design using a 1.27 mm pitch PBGA non solder mask defined (NSMD) pad and that requires two traces to pass between the pads allows a maximum line width of 0.138 mm (5.4 mils). If only one trace is required between the pads then the line width may be increased to 0.230 mm (9.1 mils). Also notice that the line width must be narrow only between the pads. Beyond this distance the lines may be expanded.

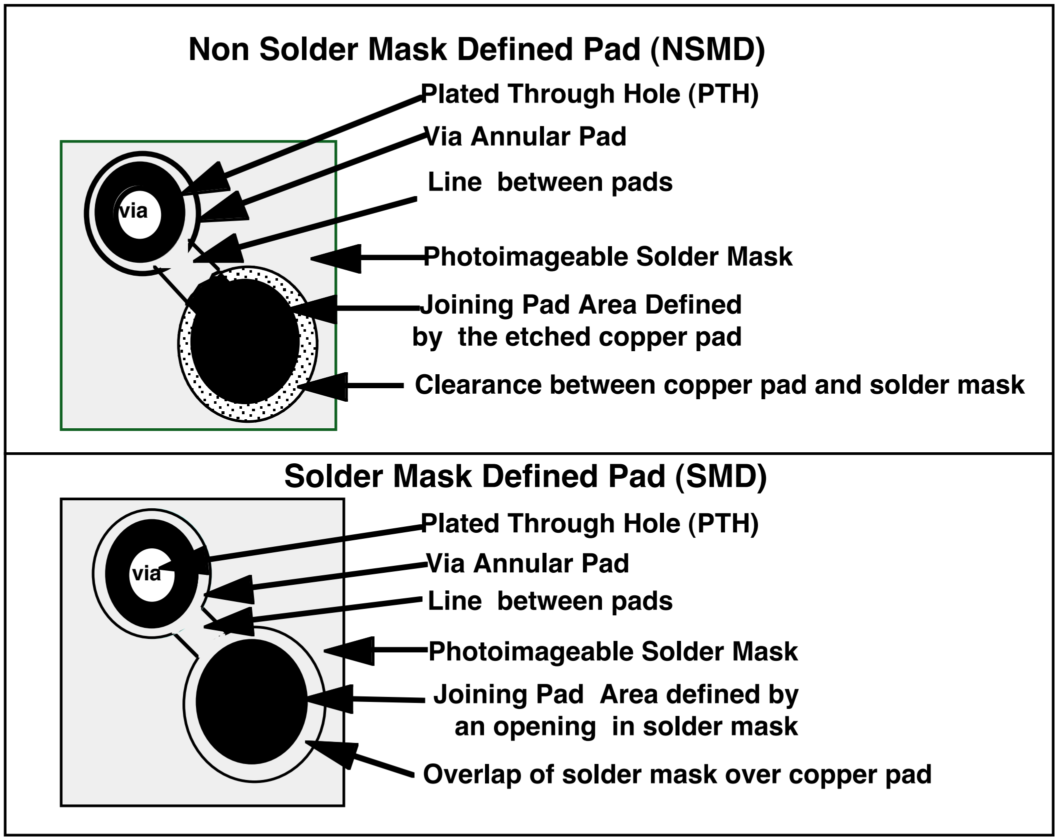


Figure 1. Design Features of a Ball Grid Array Solder Pad

Table 1 Dimensions of BGA Solder Pad Sites in Figure 1

	1.5 mm PBGA		1.27 mm PBGA		1.27 mm Ceramic BGA	
Design Feature	SMD* mm (mil)	NSMD* mm (mil)	SMD mm (mil)	NSMD mm (mil)	SMD mm (mil)	NSMD mm (mil)
PTH via DIA	0.3 (12)	0.3 (12)	0.3 (12)	0.3 (25)	0.3 (25)	0.3 (25)
PTH Pad DIA	0.65 (25)	0.65 (25)	0.65 (25)	0.65 (25)	0.65 (25)	0.65 (25)
Solder Pad DIA	0.79 (31) 0.89 (35)	0.65 (25)	0.79 (31) 0.89 (35)	0.58 (23)	0.84 (33)	0.72 ±.037 (28 1/2 ±11/2)
solder mask clearance (pull back)	n/a	0.076 (3) ±.025. (±1)	n/a	0.076±.025 . (3±1)	n/a	0.076 ±.025 . (3±1)
paste mask opening (stencil)	0.65 (25)	0.65 (25)	0.58 (23)	0.58 (23)	0.81 (32)	0.81 (32)

* SMD= Solder Mask Defined and NSMD= Non Solder Mask Defined Pads

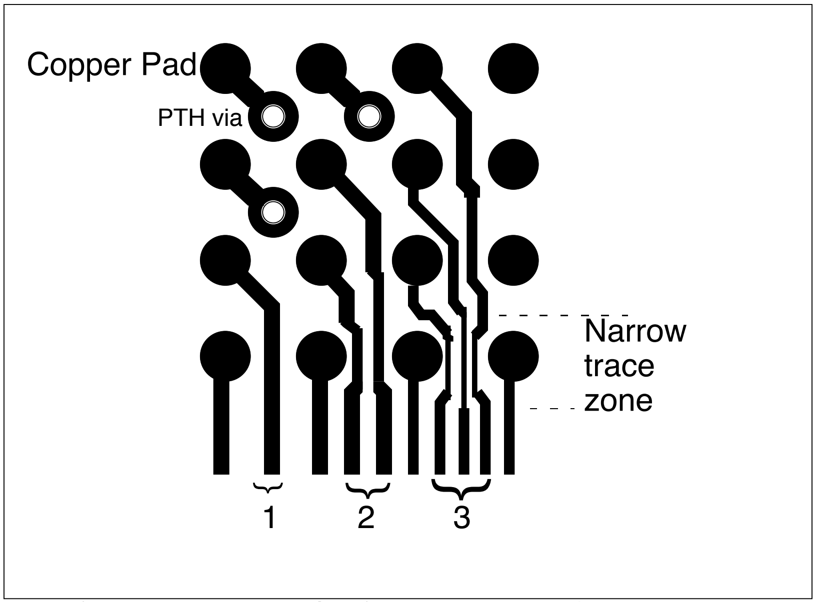


Figure 2. Trace Options between Copper Pads

Table 2. Feature Dimensions Shown in Figure 2

	1.5 mm PBGA		1.27 mm PBGA		1.27 mm Ceramic BGA	
Design Feature	SMD mm (mil)	NSMD mm (mil)	SMD mm (mil)	NSMD mm (mil)	SMD mm (mil)	NSMD mm (mil)
Copper Pad DIA	0.79 (31) 0.89 (35)	0.65 (25)	0.79 (31) 0.89 (35)	0.58 (23)	0.84 (33)	0.72 (28 1/2) ±0.037(±11/2
Space between pads	0.71 (28) -0.61 (24)	0.85 (33.5)	0.48 (19) 0.38 (15)	0.69 (27)	0.43 (16)	0.5 (20.0)
Line Width for 1 trace between pads**	0.237 (9.3) to 0.203 (8.0)	0.283 (11.2)	0.160 (6.3) to 0.127 (5.0)	0.230 (9)	0.143 (5.6)	0.17 (6.7)
Line Width for 2 traces between pads**	0.142 (5.6) to 0.122 (4.8)	0.170 (6.7)	0.096 (3.8) to 0.076 (3.0)	0.138 (5.4)	0.086 (3.4)	0.110 (4.3)
Line Width for 3 traces between pads **	0.101 (4.0) to 0.087 (3.4)	0.121 (4.8)	0.069 (2.7) to 0.054 (2.1)	0.099 (3.9)	0.061 (2.4)	0.079 (3.1)
* SMD= Solder Mask Defined and NSMD= Non Solder Mask Defined Pads **Assumes equal line widths and spaces.						

Table 2 implies that a wide choice of design rules can be used to meet wiring needs. However a well designed package footprint can be escaped using comfortable design rules of 0.2mm (8 mil) lines and spaces on only two to four PWB layers.

Wiring patterns using 0.2 mm (8 mil) lines

Figures 3 and 4 show a wiring pattern principle which can be used to escape a large number of traces using 0.2mm (8 mil) lines and spaces. The example BGA array is a 1.27 mm (50 mil) pitch Ceramic BGA. This pattern has the least space between the preferred NSMD pads 0.5 mm (20 mils). The other NSMD pad types will be able to follow this example easily. The example solder pad is an NSMD 0.76 mm (30 mil) diameter. Allowing only one trace between pads, the line width is limited to 0.18 mm (6.7 mils). The traces are narrowed to 6.7 mils on the top surface (Figure 3) for only a length of 17 mils between the pads. Knowing this could be a yield sensitive feature, the PWB vendor can use these spots to monitor the overall process. This requires "early vendor involvement" in the design and prototyping cycle. The other areas in the design use the 0.2 mm (8 mil) lines.

The interior pads that can not escape on the top surface must escape on "subsurface" layers (either interior layer or bottom side layer). Figure 4 shows the subsurface wiring pattern of 0.2mm pads between 0.65 mm via pads. Line narrowing on the subsurface layer is not required.

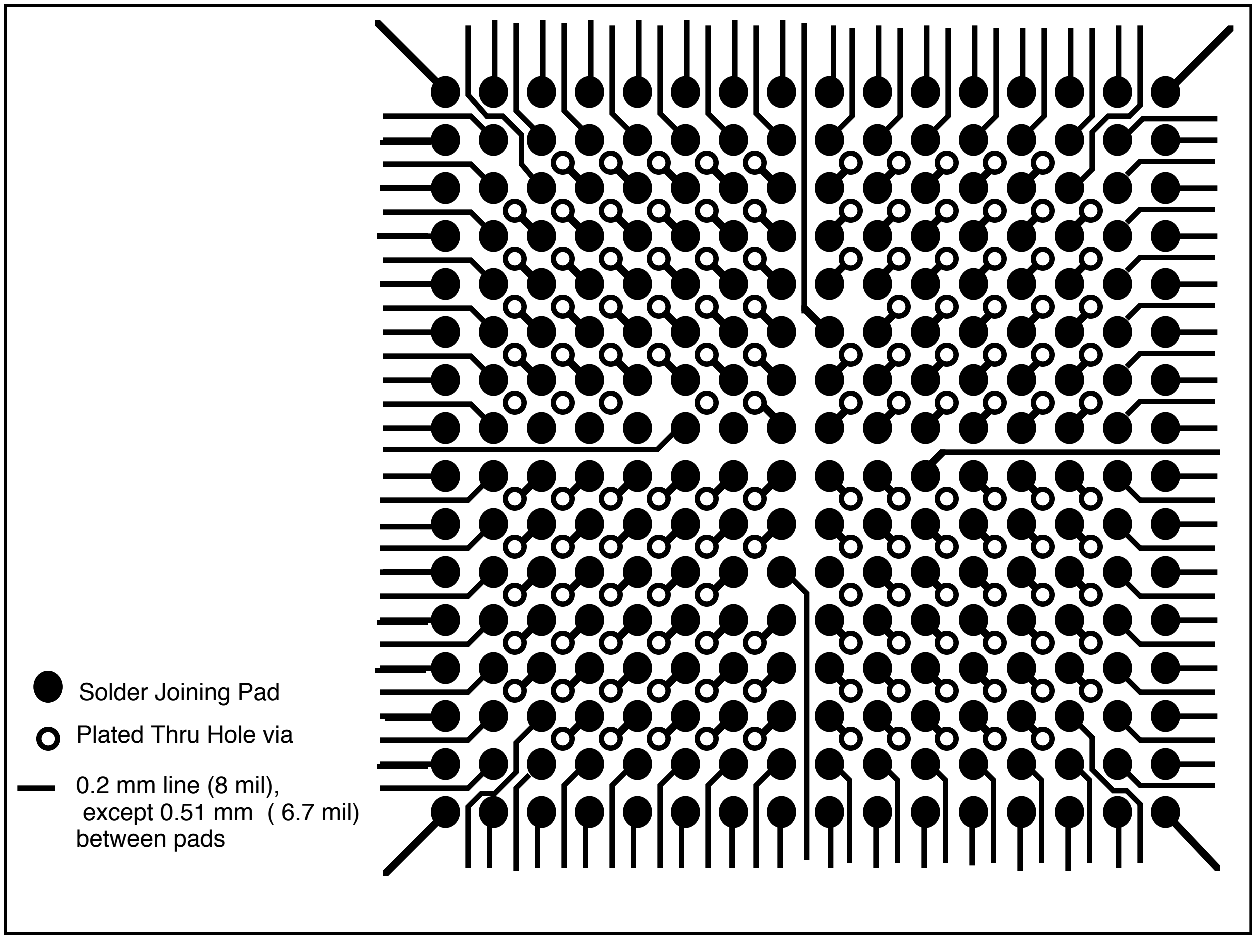
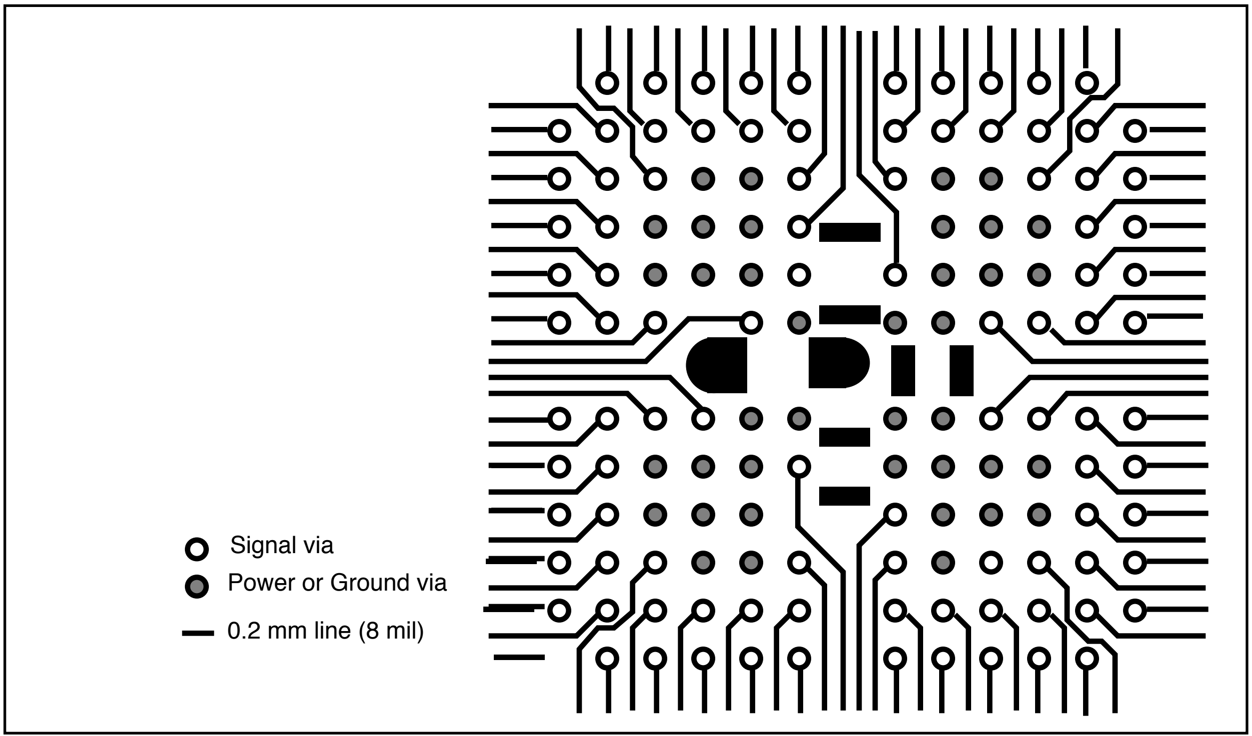


Figure 3. Top Surface Footprint



.Figure 4. Subsurface Vias, Wiring Pattern and Capacitor Pads

Figures 3 and 4 show the four outer rows plus a few more signals can be escaped using just two PWB layers. The above example is a 16 x 16 array. Of the 256 sites 236 are connected on two PWB layers using 0.2 mm (8 Mil) lines and spaces. Table 3 shows the number of signals that can be wired for several sizes of arrays when using the same wiring approach of Figures 3 and 4. Though the ratio of escapable pads to total pads decreases with array size, it should be evident that most of the escape wiring can be achieved in two PWB layers.

Table 3. Number of Signal Escapes on only Two PWB Layers

array size	total pads	No. of Traces between subsurface vias 1	2	3
14 x14	196	**184**	**196**	**196**
16 x 16	256	**216**	**256**	**256**
16 x 19	304	**240**	**286**	**316**
19 x 19	361	**264**	**316**	**352**
21 x 21	441	**296**	**356**	**400**
25 x 25	625	**360**	**436**	**496**
31 x 31	961	**456**	**556**	**640**
35 x 35	1225	**520**	**638**	**736**
Only 1 trace between solder pads on top surface				

The examples shown are idealized pin assignments. It is important for chip designers and package designers to plan for system level interconnect. Even though an idealized case is demonstrated, it should be apparent that the required number of PWB layers can be reasonable.

Decoupling Capacitors

The example in Figure 4 also shows footprints of decouplimg capacitors which can be placed opposite the BGA site in areas where some of the plated thru vias are omitted. Standard 0805 and 0603 size capacitors and smaller can be used. These locations are several millimeters closer to the integrated circuit die than if it were placed alongside the BGA. Of course, a designer must choose whether a single or double sided assembly is warranted before placing the capacitors opposite the BGA.

Test Points

Bare board test and in circuit tests apply a test probe at the PTH via associated with a solder joint. These vias are noticeably absent on the outer two rows of the BGA escape examples. However a via in the net often exists somewhere in the circuit net. Additionally JTAG testing and circuit card functional testing are test options which do not require the use of a probe at each lead. The test strategy of a circuit card ought to be established prior to initiating the PWB design.

Application Examples

The pinout scheme of signal, power and ground of the PowerPC 604™ in a 255 lead Ceramic Ball Grid Array is shown in Figure 5. The signals are placed in the outer four rows allowing the wiring escape in two layers. The interstitial vias are shown to indicate they are used only for the third and fourth rows.

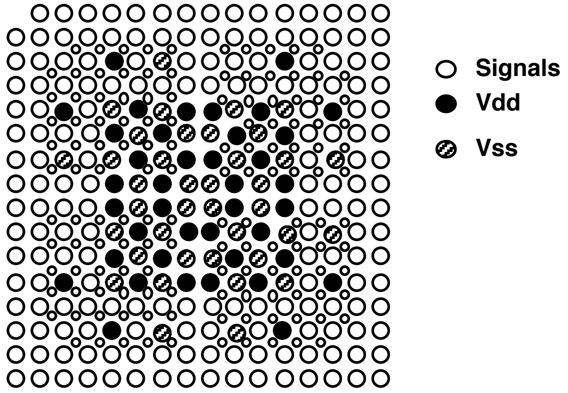


Figure 5. PowerPC 604™ Microprocessor CBGA Signal Power and Ground Scheme.

In a more complicated case the Motorola MPC105 PCI Bridge/Memory Controller is packaged in a 16 x19 CBGA (1.27 mm pitch). As shown in Figures 6 and 7, the chip has 248 signals. Using 0.2mm (8 mil) line and spaces allows only 240 lines to escape on two layers leaving 8 lines that must either escape on a third layer or force the use of finer lines on the second layer, such as 0.125 mm (5 mils) in the region of the footprint. Using a third layer to escape is an easy choice if the interconnection of the other components on the PWB require a third signal layer or more. However, if the rest of the system can be designed in just two layers then a designer should consult the PWB vendor(s) as to whether to add an extra layer or use finer lines.

Conclusion

Footprint design rules for reliable BGA assemblies has been presented. Common layout wiring rules are compatible with these BGA footprint rules allowing circuit board designs of a reasonable complexity.

Acknowledgments

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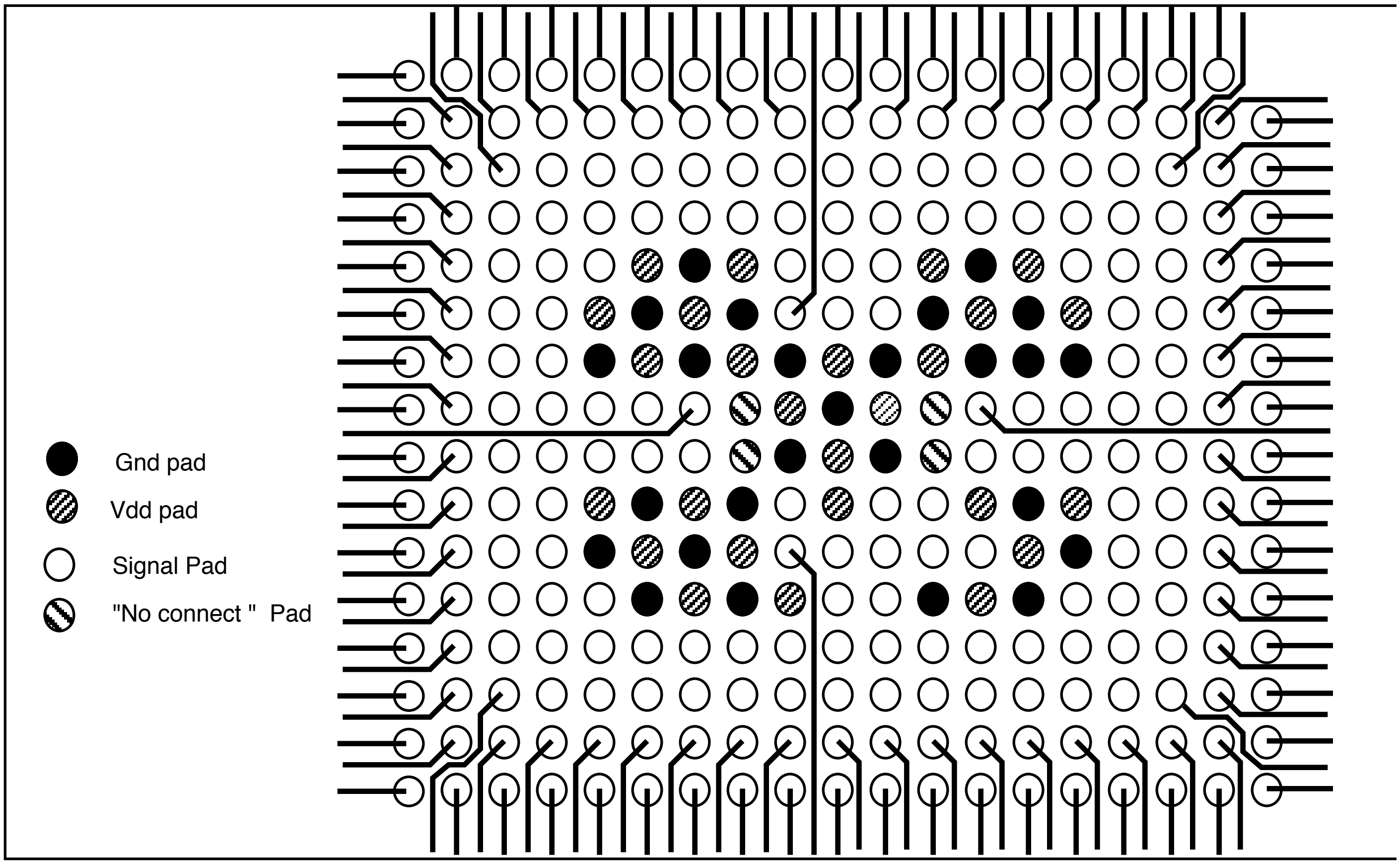

Figure 6. MPC105 Package Footprint and Top Layer Escape Pattern

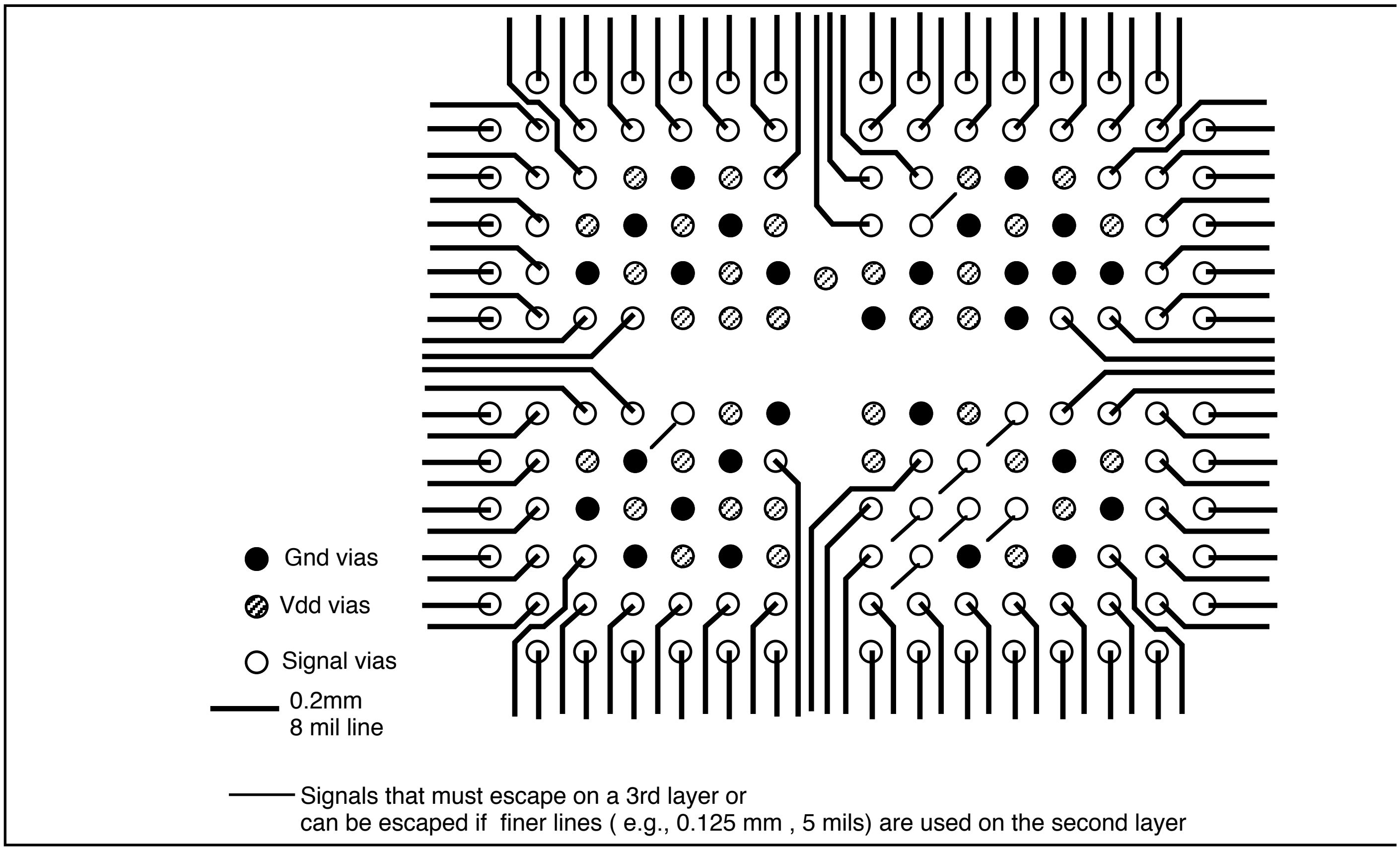

Figure 7. Subsurface Escape pattern for MPC 105, 16 x 19 BGA