Precision Voltage Reference Using EEPROM Technology

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Need For Better Voltage References

Precision Voltage References have been difficult to achieve using conventional process technology. This is evident by the high cost of such products. One measure of the need for a more precise reference is the existence of 12-16 bit ADC and DAC products that achieve integral linearity but are limited to only 10 bit absolute accuracy because of the voltage reference. In some applications better absolute accuracy is desirable. Consider the case of a 5 volt 12 bit converter operating over the industrial temperature range. If 100% of the converter error is allocated to the voltage reference then less than 0.5 LSB error over the 125°C range would be allowed. This would correspond to 122ppm or 0.012% or 0.61mV initial accuracy with 0 ppm/°C temperature dependence. Conversely, 100% error allocation to temperature would require a performance of less than 1ppm/°C. Present technology has difficulty providing 1mV initial accuracy and 5ppm/°C. As a result, products that provide this performance are expensive and the industry is left with 12-16 bit accurate quantizers degraded by 10 bit accurate references. Markets that require better performance include medical, industrial control, instrumentation and test and measurement. A novel circuit has been developed that will provide better performance at lower cost than is presently available.

The Conventional Voltage Reference

Conventional precision reference techniques employ either buried-zener diodes or laser trimmed bandgap references. Both utilize special bipolar or BiCMOS process technology and require manufacturing adjustments. Trimming is required in order to achieve accuracy and temperature dependence better than 10mV and 10ppm/°C respectively. Quantum adjustment using fuses or continuous adjustment using laser trimmed thin film resistors are expensive but allow 1mV initial accuracy and 5ppm/°C to be achieved in a production environment. Lower cost and higher integration favor a CMOS-based technology. An example of an early CMOS reference is shown in Figure 1. This simplified schematic shows an amplifier connected as a voltage follower with an approximate output voltage:

$$V_{OUT} = V_{T1} - V_{T2} \qquad \text{equation (1).}$$

Using the depletion device threshold V_{T2} of -2.5V and the enhancement device threshold V_{T1} of 1.0V, a typical V_{OUT} reference voltage of 3.5V can be achieved. One drawback of this approach is that process variations result in an initial accuracy error of ±15% thus requiring a subsequent high-resolution adjustment. Another problem with this technique is that the depletion and enhancement input device mismatches generate a differential temperature variation due to the temperature dependence of mobility and threshold voltage. Using special circuit techniques, 10-20ppm/°C can be achieved in production but

the initial accuracy limitation remains. The origin of both limitations is the input device mismatch caused by inexact threshold implants, and these cannot be corrected by trimming. Furthermore, the technique does not permit continuous trimming of the output voltage. These limitations can be overcome using EEPROM technology to implement a reference based upon a differential charge rather than a differential implant as described below.

Using EEPROM Technology to Set Charge on the Floating-gate

Before describing the differential charge amplifier, it is instructive to review EEPROM techniques for charging and discharging the gate of a device. For many years EEPROM technology has routinely used "programming" techniques to add and subtract charge ? Q on a floating-gate device thereby changing the threshold voltage as given by the approximate equation (2).

$$V_T = ?Q / C_{OX} + V_{TO} \qquad \text{equation (2).}$$

Programming an array of floating-gate devices to represent logical data EEPROM memories provides non-volatile storage of digital data. The floating-gate device shown in Figure 2 is one element of a conventional EEPROM memory cell. The device comprises an NMOS transistor, an equivalent capacitance C_E, and 2 tunnel diodes. Structurally the tunnel diode is fabricated as an oxide insulation between 2 conducting electrodes. Note that the 2 diodes are connected such that the interior conducting node is isolated by oxide in all directions. Because this node is also the NMOS gate terminal it is referred to as the "floating-gate". Typically the charge trapped on this floating-gate can remain without loss for between 10 to 100 years.

The ideal tunnel diode "current-versus-voltage characteristic" (I_{TD} vs. V_{TD}) is shown in Figure 3. This asymmetric curve is desirable and represents a preferential direction of charge flow thereby precluding a parasitic charge loss by reverse conduction. The mechanism that describes the relationship between current I_{TD} and voltage V_{TD} is called Fowler-Nordheim Tunneling. Current flows when the oxide field exceeds approximately 10MV/cm (10 to 100MV/cm). This electric field would correspond to 10V on a 100Å oxide. As illustrated ideally in Figure 3, no current flows until V_{TD} reaches V_{FD} the turn-on voltage of the diode. For voltages below V_{FD} negligible current flows and the charge remains trapped on the floating-gate.

Figure 2 can now be used to explain the process of removing charge from the floating-gate. Assume that the equivalent capacitance C_E represents all capacitors connected to the floating-gate and that all other device capacitance is negligible. Let V_{FG} be zero volts initially and all terminals be at ground. V_P is now driven negative until

$$V_P = V_{FG} - V_{FD} \qquad \text{equation (3).}$$

At this point the lower tunnel diode begins to conduct and for more negative values of V_P the floating-gate voltage is given by:

$V_{FG} = V_P - V_{FD}$ for $-2V_{FD} < V_P < -V_{FD}$ equation (4).

When VP is returned to ground the floating-gate voltage remains stable. In a likewise manner adding charge to the floating-gate begins by raising V_E to a positive potential. At a sufficiently high voltage the floating-gate voltage will now track V_E as given by:

$V_{FG} = V_E - V_{FD}$ for $2V_{FD} < V_E < V_{FD}$ equation (5).

When V_E is returned to ground, the floating-gate voltage remains stable. For V_{FD} in the range of 10V the swing in V_{FG} could ideally be as large as ±10V before conduction. The new reference described in this paper only requires a 1-5V range of V_{FG} thereby insuring negligible charge loss by parasitic tunneling. This also reduces the long term drift of the reference.

Technique for Accurately Setting the Floating-gate Voltage

The previous section describes two distinct operations to increase and to reduce charge on the floating-gate. To meet the goal of continuous adjustment these must be combined into one operation that allows an arbitrary floating-gate voltage setting without excessive current flow. This is accomplished by connecting V_P to a current source that pulls down to a negative voltage thereby limiting the diode conduction current to an appropriate value. At the same time V_E is connected to a large positive voltage source. From equation (5) it can be seen that the floating-gate voltage is one tunnel diode drop (V_{FD}) below V_E. By the simultaneous actions of charge removal by the current source and charge addition by the voltage source, the precise floating-gate voltage can be set by the adjustment of V_E. This is illustrated in Figure 4. As the current source pulls down V_{FG}, the action of the voltage source pulls V_E up until the precise V_{FG} is achieved. At time point T_S the sources are disconnected and V_{FG} remains at its precise setting. This novel technique is used to provide real-time analog control of the floating-gate voltage.

Precision Floating-gate Voltage Reference

A new high performance voltage reference based upon EEPROM floating-gate technology will now be described. By starting with the threshold difference amplifier of Figure 1 and replacing the depletion device with the floating-gate device of Figure 2 a charge difference amplifier is constructed. With the addition of a feedback amplifier and a feedback network to drive the tunnel diode string a precision voltage reference is realized. The simplified schematic of the new floating-gate analog voltage reference is shown in Figure 5.

The reference amplifier input devices are identical except for the floating-gate device at the non-inverting input. The current source I_1 connected to the negative voltage supply V_{NV} is able to pull V_P to the desired negative voltage. The source follower voltage can

drive V_E to the desired high voltage because its drain is connected to a large positive supply V_{HV}. Both positive and negative high voltages are generated by on-chip charge pumps. The reference amplifier is connected as a voltage follower.

Initially an external supply V_{EXT} is connected as shown to the feedback amplifier. The switches connect the current source I1 and the source follower. Consider that initially V_{REF} is less than V_{EXT}. In this case the feedback amplifier output V_X is a large positive voltage. This drives the follower on hard and raises the voltage V_E which increases the floating-gate charge and increases V_{REF}. Ideally the value of V_{REF} converges asymptotically to V_{EXT}. After final value is reached the switches are thrown and this grounds the tunnel diode terminals and terminates conduction to and from the floating-gate. After equilibrium has been reached an external meter measures the V_{REF} output. If the desired initial accuracy has not been achieved a subsequent minor adjustment is made in V_{EXT} and the charge-discharge cycle is repeated until V_{REF} reaches its ideal final value. This technique reduces error sources to a negligible value.

Measured Results

A voltage reference based upon the floating-gate technique described above was designed and fabricated. Novel techniques were used in both the process technology and the circuit design. In the actual implementation the reference amplifier is 2 stages plus output buffer that achieves 130dB D.C. open loop gain. Measured data from the voltage reference is shown in Table 1. The performance achieved is equivalent to some of the most accurate voltage references available. The measured initial accuracy of better than 0.2mV reflects the accuracy of the novel analog technique to precisely set the floating-gate charge. The low temperature dependence is due to the low temperature coefficient of the MOS capacitor used in the design together with good analog technique. Low drift over time is achieved because of the negligible charge loss from the thick oxide isolated floating-gate. Special analog techniques allow circuit operation with only 500nA supply current and consequently provide an ideal solution for battery powered applications.

As with other precision voltage references unique process technology brings some performance benefits and such is the case for this reference. Unlike more conventional technology that uses thin tunnel oxides the thick tunnel oxide process used by Xicor allows larger voltages on the floating-gate. This improves the initial accuracy setting and reduces the drift over time as confirmed by measurement. Furthermore tunnel diode currents are substantially smaller than current needed for conventional channel hot-electron programming techniques and as a result this approach is more amenable to in-circuit calibration.

Data shows that further improvements are possible. Using iterative techniques an initial accuracy better than 100uV can be achieved. Temperature dependence can also be reduced by additional trimming. Future applications include voltage references,

regulators, voltage detectors and data acquisition products such as A/D and D/A converters.

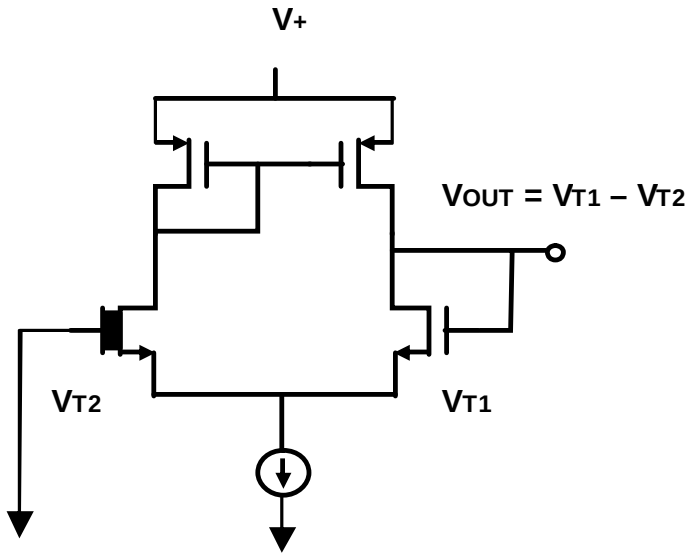

Figure 1. Conventional Threshold Difference Reference

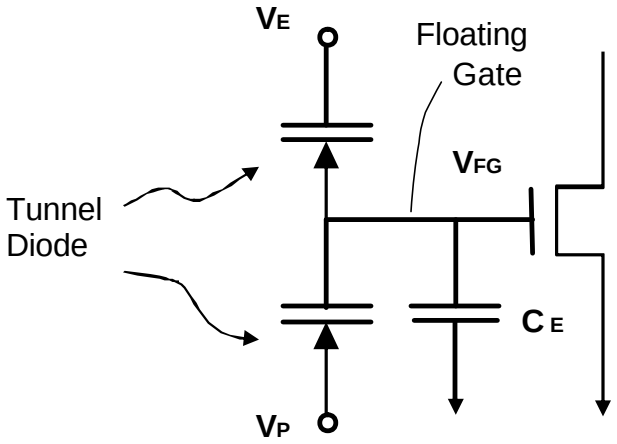

Figure 2. Simplified Schematic of Floating-gate Device

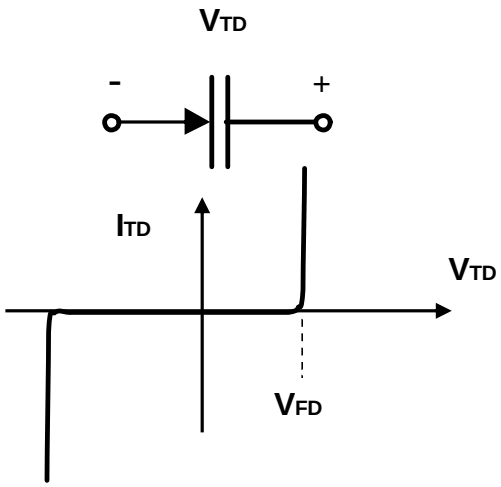

Figure 3. Ideal Tunnel Diode Characteristic

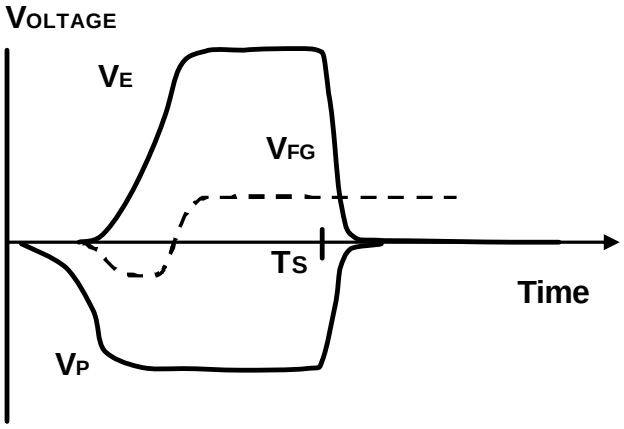

Figure 4. Floating-gate Voltage Waveform During An Accurate Set Operation

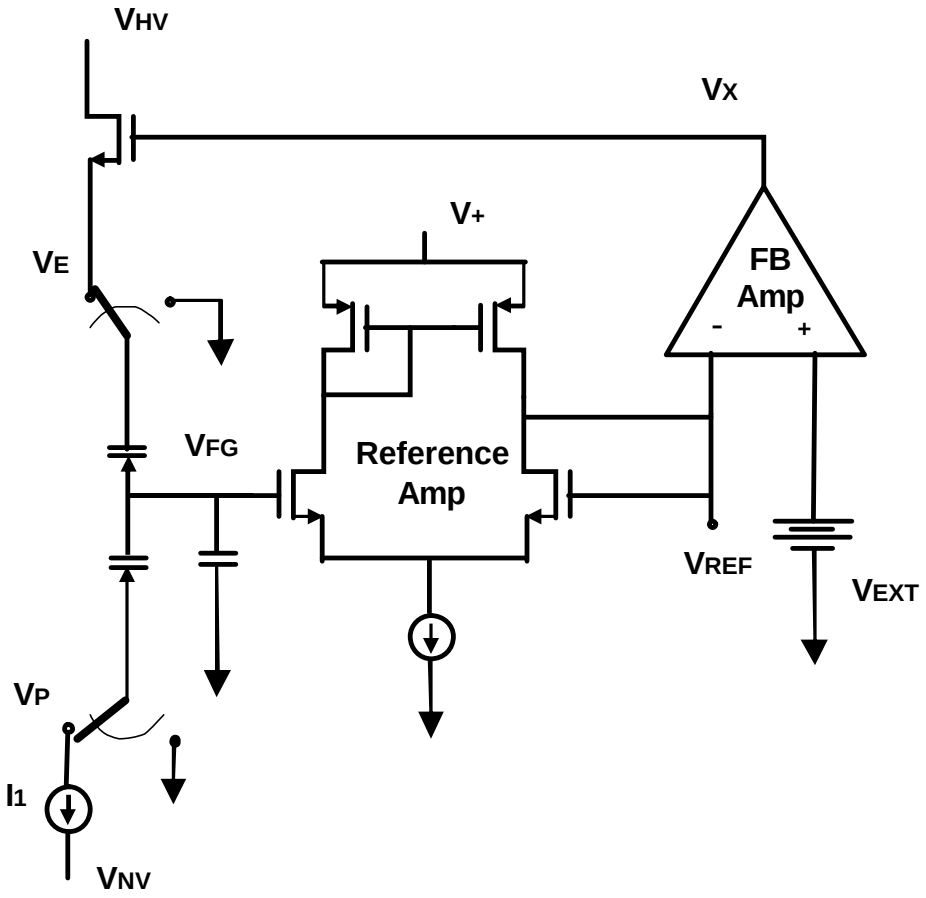

Figure 5. Internal Analog Circuits Perform Precise Charge Storage

• Initial Accuracy	< 0.2mV
• Low TC	3 ppm / ° C
• Low Drift	10ppm/1000hr
• Low power	500nA at 5V

Table 1. Floating-gate Voltage Reference Measured Data