AND8032/D

Conducted EMI Filter Design for the NCP1200

Prepared by: Christophe Basso
ON Semiconductor
Avenue Eisenhower, BP1056, 31023 TOULOUSE Cedex France
33 (0)5 61 19 90 12 e–mail: christophe.basso@onsemi.com

ON Semiconductor

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

If the NCP1200 easily lends itself to designing Switch–Mode Power Supplies (SMPS) in a snap–shot, its presence among other equipments necessitates an adequate ElectroMagnetic Interference (EMI) input filter. Fortunately, friendly methods such as SPICE exist to isolate the guilty harmonics and make them stay below the limit. This application note briefly describes the mechanism of conducted EMI noise generation and depicts a way to circumvent it.

The Bulk Capacitor is a Natural Shield

As Figure 1a depicts, an SMPS is supplied by a network made of a diode bridge rectifier and a bulk capacitor. Every time the mains peak voltage exceeds the bulk capacitor level, two diodes of the input bridge conducts for a period of time given by the DC rail ripple: the larger the ripple, the longer the conduction time (≈ 1–3 ms). As a result, Cbulk is recharged at a rather low rate (every 10 ms for a 50 Hz mains) while the SMPS load draws pulses at its high switching frequency. During the refueling by the diodes, Cbulk stores energy and delivers this energy during the time the diodes are off (high series resistance, but still weakly capacitive).

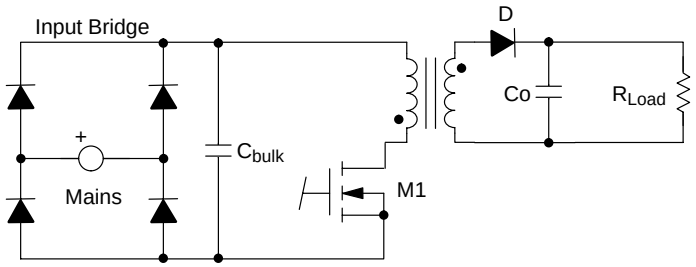

Figure 1a. A typical component arrangement for an SMPS (here a FLYBACK).

The current flowing through Cbulk is thus the ON time drain current for a FLYBACK converter. Cbulk is unfortunately not a perfect element and Figure 1a can be refined into Figure 1b where parasitic elements appear: the Equivalent Series Inductance (ESL) and the Equivalent Series Resistor (ESR).

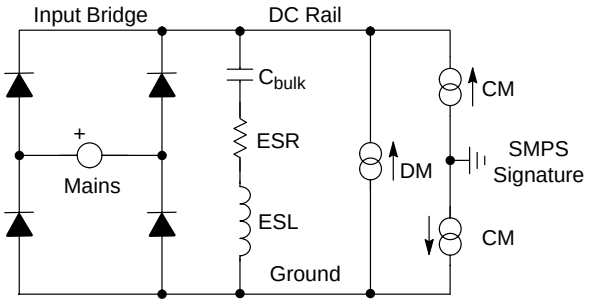

Figure 1b. A more realistic way to represent the EMI generation mechanism.

These technology dependent elements work together to prevent the capacitor from being a true capacitor. At low frequency, the impedance is capacitive (Z goes down when F goes up, C dominates), at medium frequency the impedance is resistive (Z stays flat, ESR dominates) and at higher frequencies, Z goes up because ESL dominates: this is depicted by the well know impedance versus frequency plot as shown by Figure 1c (a 400 V 33 μF snap–in capacitor, Y axis in dBΩ). In SPICE, this is rather easy to model, as portrayed by Figure 1d.

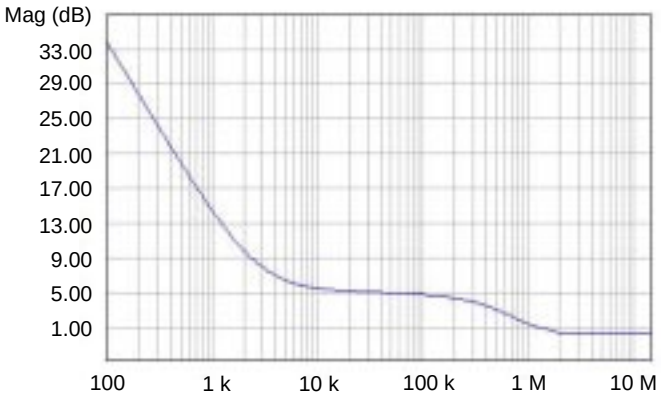

Figure 1c

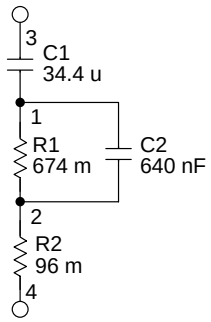

Figure 1d

A typical impedance plot of a 33 μF 400 V capacitor . . . and its equivalent SPICE model showing the resonating elements.

Differential and Common Mode

As you can see on Figure 1b, there are three current generators: one is for the differential mode (DM) currents that flow 180° out of phase on each branch while the remaining two generators depict the common mode (CM) current flowing in phase on both the DC rail and ground. The DM level is caused by the weakness of Cbulk to perform its filtering function over a large frequency range due to its friends ESL and ESR. The CM noise finds one of its roots in capacitive current displacements induced by high dV/dt over a key node: the MOSFET drain. This quickly varying voltage present on this pin pushes currents into capacitive elements exhibited by the transformer (disposed between all terminals), the MOSFET (Coss or an additional snubber) and the various capacitive leaks. Instead of coming back to drain through Cbulk, they continue to transit via the Ground and the DC rail and come back to the drain after exciting the measurement network (a LISN, see its definition below). DM currents usually cause troubles in the low frequency range of interest while CM currents bother the designers in the remaining higher portion of the spectrum. As you can read, it is of importance to be able to identify who is hurting the measurement the most in order to take the adequate solution: CM and DM cures are not the same. Finally, DM disturbances are rather easy to predict, to the opposite of CM currents which depend on various stray paths (copper traces position, stray capacitance etc.) and are extremely difficult to estimate. Furthermore, because of the unsymmetrical nature of stray elements, combinations of currents can lead to an unequilibrated noise distribution over Live and Neutral . . .

Measuring the Noise

Standards have been established to fix a limit below which your SMPS will not disturb the surrounding equipment sharing the same line or outlet (e.g. CISPR22, FCC15 etc.). However, since we deal with circulating currents, the reference impedance used to measure their action takes on

importance: the mains impedance in ON Semiconductor labs is not quite the same as in your building for instance . . . As a matter of fact, international standards have defined a reference impedance on which the measurements will be made. This impedance is guaranteed by a Line Impedance Stabilization Network (LISN) and precisely defined by CISPR16 document. Figure 2 portrays how this device is made. The LISN offers a 50 Ω impedance over the frequency of interest (e.g. 150 kHz–30 MHz for CISPR22) and shields the measurement against unwanted incoming noises. Please note that the high values of some capacitors connected between Live and Earth require the adjunction of an isolating transformer between your mains and the LISN.

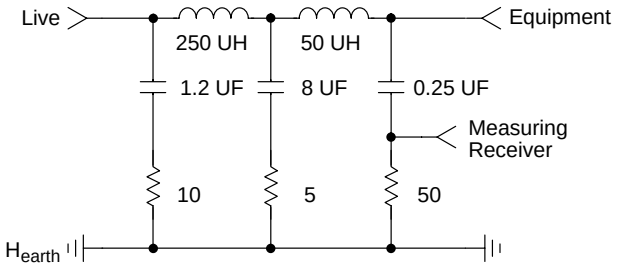

Figure 2. CISPR16 Network (Duplicated for the other line(s))

Fighting Against Conducted EMI

As we said, DM solutions differ from CM solutions. However, some parasitic elements can this time play in our favor . . . DM will usually be combated using the component arrangement of Figure 3a while CM requires Figure 3b arrangement.

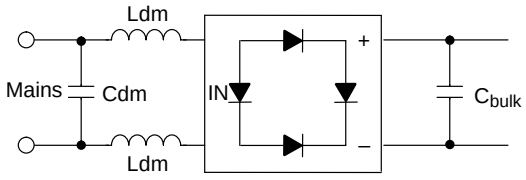

Figure 3a. By connecting two inductors (coupled or not), you attenuate the differential mode noise.

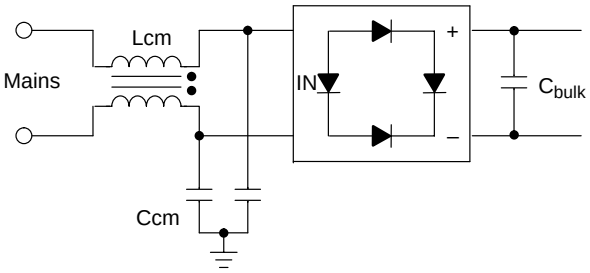

Figure 3b. Two coupled inductor (wounded in opposite directions) route the noise to earth via two Y–type capacitors.

CM inductors are usually of high values (≈ 1 mH to 50 mH) and strive to route the CM noise current through earth via Y–type capacitors. However, since earth leakage current is limited for security reasons, Y capacitors rarely exceed a few nano–farads thus requiring large CM inductors. Due to their winding technique (same directions), CM inductors do not offer any opposition to the DM mode (DM currents cancel the internal field). True DM inductors are either single component or coupled ones (values up to 1 mH). Fortunately, when these CM inductors are crossed by DM currents, the internal field is cancelled: the remaining inductances are the leakage inductances. If these leakage elements are of sufficient values, we can use them for filtering DM noise. Otherwise we need to add an external single coil for DM only (Figure 3c).

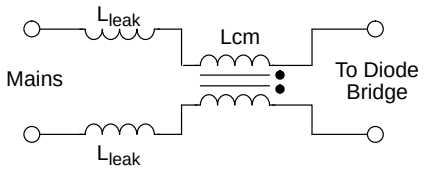

Figure 3c. When crossed by DM current, a CM inductor unveils two “leakage inductances”. Typical value would be 300 μH for a 27 mH type, but it really depends on the way the manufacturer winds the coils.

In some designs, there is no third earth conductor. In that case, you cannot wire two Y capacitors on the filter input. As we said, these Y capacitors are used to route most of the current displaced by the drain voltage back to the originator, a little crossing the LISN network but low enough to stay below the standard limit. The solution consists in providing this path through another Y capacitor but connected between primary and secondary grounds as shown by Figure 3d. Again, this capacitor cannot exceed a given value in order to keep the leakage current within the level imposed by the security standard (250 μA for all class II equipment).

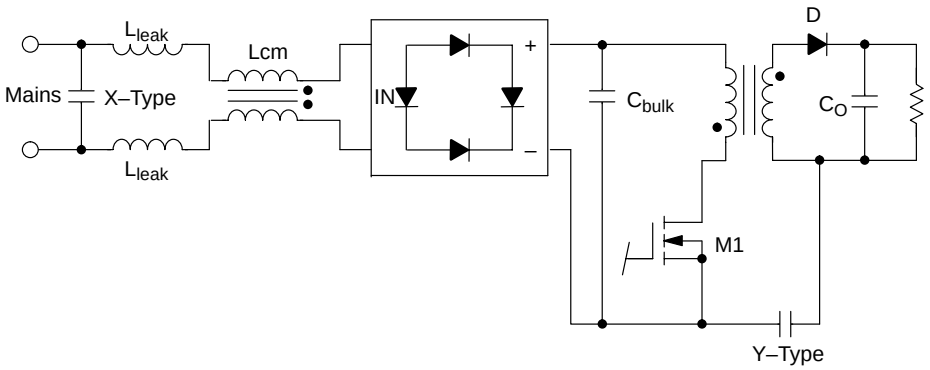

Figure 3d. A typical two–wire implementation when there is no earth conductor.

Evaluating the SMPS Signature

Before calculating any filter, we need to know the enemy: "what harmonic frequency hurts me the most?" On the paper, by hand or with a simulator, we can reasonably estimate the amount of DM noise the SMPS will deliver thanks to a good knowledge of the generation mechanism. CM will require a true measurement because many physical factors influence its content (PCB layout, stray capacitances etc.).

Depending on our topology and its operating mode (Continuous or Discontinuous Conduction Mode, CCM or DCM), we can draw the drain current signature. Figure 4a gives the typical plot for a DCM and a CCM FLYBACK converter.

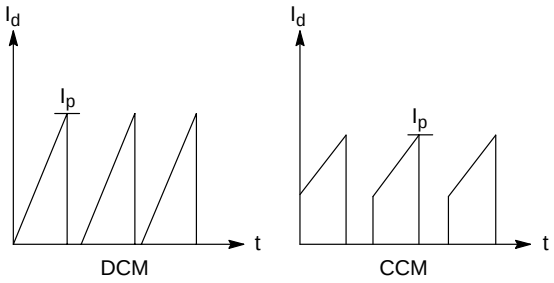

Figure 4a. Typical SMPS signature with two different operating modes.

In both cases, we need to evaluate the harmonic content through Fourier decomposition. In that area, SPICE can really help us through its Fast Fourier Transform (FFT) algorithm. Without entering into the details (see reference [1]), you can tailor the analysis bandwidth by adjusting the duration of your transient simulation:

.TRAN TSTEP TSTOP [TSART] [TMAX] [UIC] [optional]

.TRAN 100NS 801US 400US 50NS UIC
; 5.2MHz sweep range, 2.493kHz analysis BW, 4010 points (1)

.TRAN 24.44NS 500US 400US 12.22NS UIC
; 20.48MHz sweep range, 10kHz analysis BW, 4091 points (2)

.TRAN 489NS 2.1MS 100US 244.5NS UIC
; 1.024MHZ sweep range, 500Hz analysis BW, 4090 points (3)

CISPR22 specifies a 10 kHz analysis bandwidth above 150 kHz up to 30 MHz. This corresponds to the second .TRAN command line (2). But SPICE can even help more by predicting the exact operating point whatever input or output conditions. Figure 4b and 4c show a complete INTUSOFT's IsSpice4 application using the NCP1200 together with a LISN built according to Figure 2. The complete SPICE netlist for the LISN is provided at the end of this document.

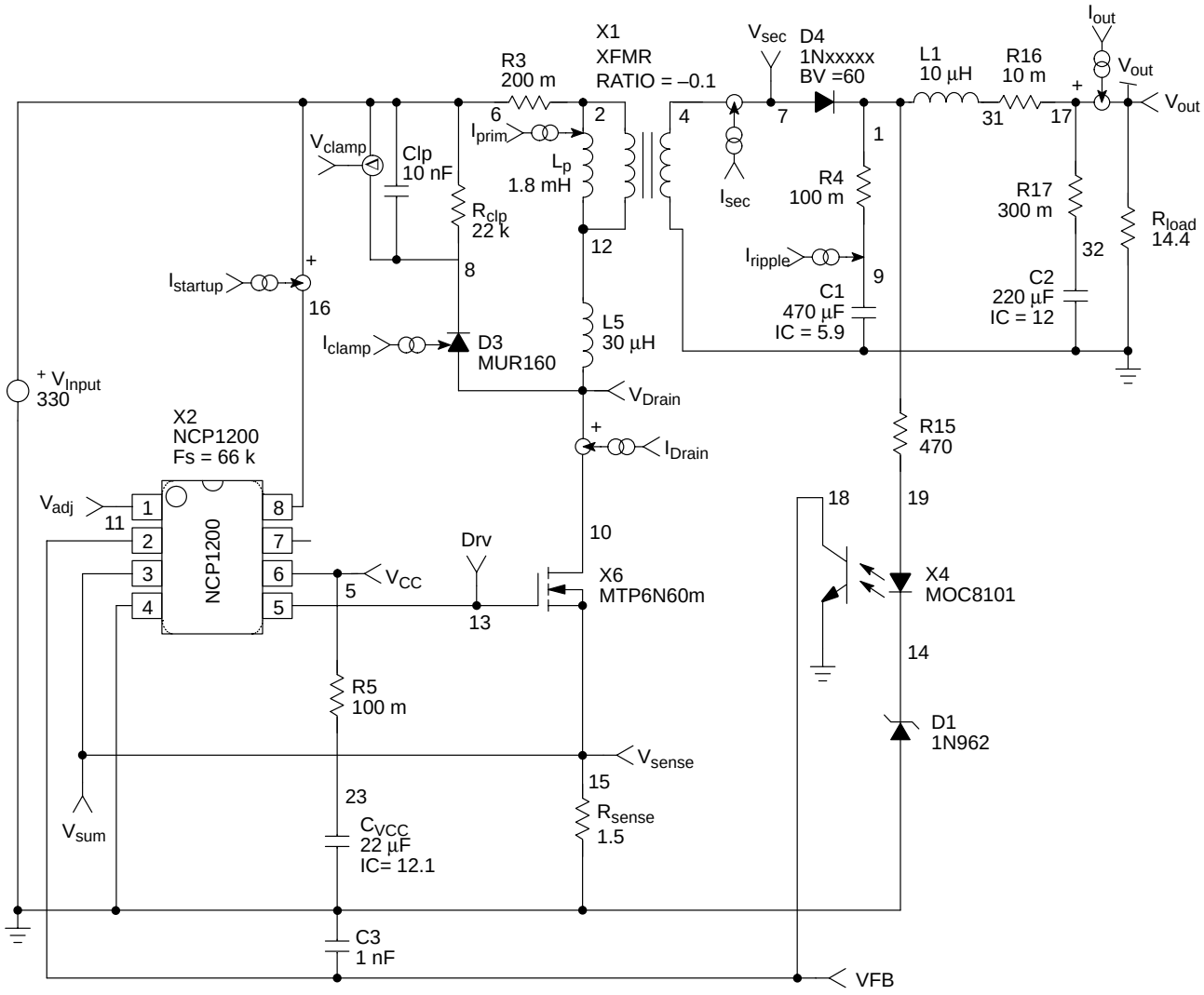

Figure 4b. A complete offline simulation template to unveil the desired operating point . . .

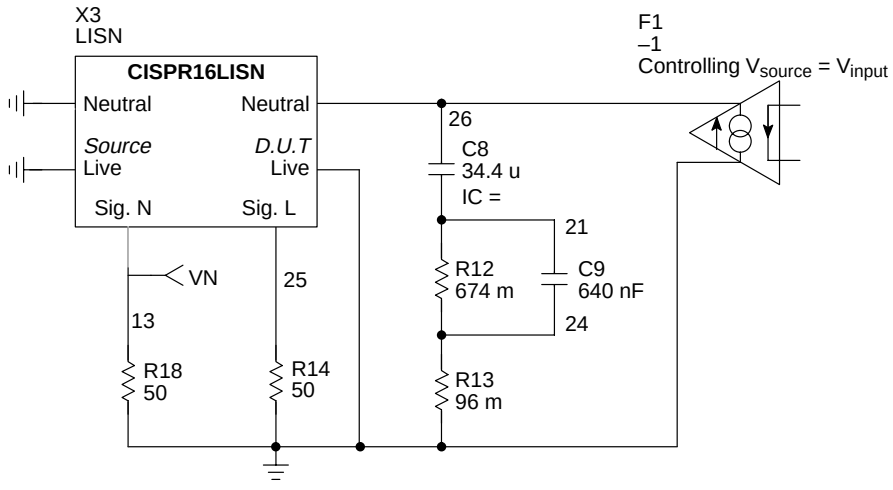

Figure 4c. . . . while the input EMI fixture lets you analyze the SPMS signature.

This application represents a 10 W universal input AC/DC wall adapter operating during given load/line conditions. To unmask the harmonics, F1 current–controlled current source routes the high frequency current pulses through the equivalent model of our 33 µF capacitor and develops the unwanted noise signal. This signal is confronted to the 50 Ω LISN network and a final reading is made on one of the outputs. For simulation reasons, we only use one input, the other one being loaded by a 50 Ω resistor.

Once the simulation is done, the data manipulation interface lets you run the FFT over VN node. After proper formatting, a graph such as Figure 4d is obtained where the vertical axis is displayed in dBµV (0 dBµV = 1 µV, 60 dBµV = 1 mV, etc.). To obtain dBµV, Log compress the Y axis and add 120. We purposely put the CISPR22 class quasi–peak limit to assess the needed amount of correction. Please keep in mind that a quasi–peak detector will give a smaller level compared to a peak detector as we naturally have with SPICE . . .

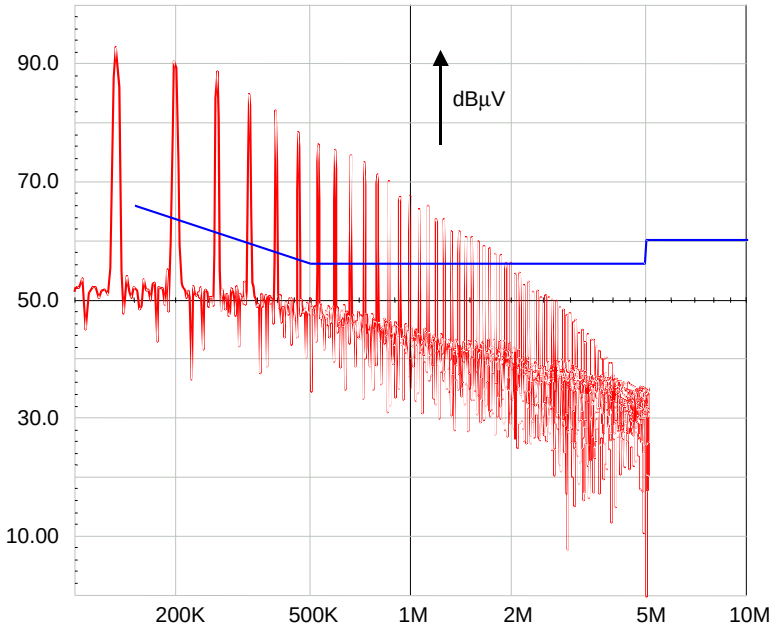

Figure 4d. Further to the simulation, an FFT plot is drawn by the graphical interface.

From this graph, we can clearly identify the value of the highest harmonic: 90 dBµV @ 190 kHz (below 150 kHz is out of the CISPR22 sweep range). To pass the limit, we shall reduce its contribution by more than 35 dB, taking into account a 10 dB safety margin:

1. Position the LC cutoff frequency fc at a given value to obtain the above rejection at 190 kHz : $-35 = -40 \cdot \text{LOG}(190\text{ k}/\text{fc})$ or $\text{fc} = \frac{190\text{ k}}{10^{\frac{35}{40}}} = 25.3\text{ kHz}$.

2. To avoid any resonance, the filter quality coefficient Q should be less than 1. By applying Q definition for a series LC filter, we obtain the following equation: $Q = \frac{\omega o \cdot L}{Rs} < 1$ where Rs is the total series resistance and $\omega o = \frac{1}{\sqrt{L \cdot C}}$. The resistance Rs will normally include all ohmic losses (ESR, inductor series resistance, load etc.) but since the 50 Ω load dominates, we will make Rs = 50 for our calculation.

3. Fix C to an arbitrary 100 nF value (for the first step) and calculate L by: $\frac{Rs}{2 \cdot \pi \cdot fc} = 315\ \mu H$. L should be in the range of 200–400 µH if you want to benefit from CM leakage inductances. If L is too big, select a bigger capacitor 220 nF, 330 nF or 470 nF.

4. Check the DC input impedance presented by the SMPS at the lowest line condition (η = 75%): Pin = Pout/0.75 = 13.3 W. With a 120 VDC input, $Rin = \frac{VinDC^2}{P} = 1082\ \Omega$.

5. Evaluate the LC filter characteristic impedance by: $Zo = \sqrt{\frac{L}{C}} = 56\ \Omega$ and be sure to follow Zmax << Rin to keep the stability. A plot example of the filter output impedance will reveal Zmax (the output impedance peaking) and endure that the above stability criterion is met. It can easily be done by sweeping the LC filter output terminal through a 1A AC source. Observing the terminal voltage will display ohms. In our application, the peaking shows a value of Zmax = $\frac{Zo?}{Rs} \cdot \sqrt{1 + \left(\frac{Rs}{Zo}\right)^2}$ or 38.5 dBΩ with our application values.

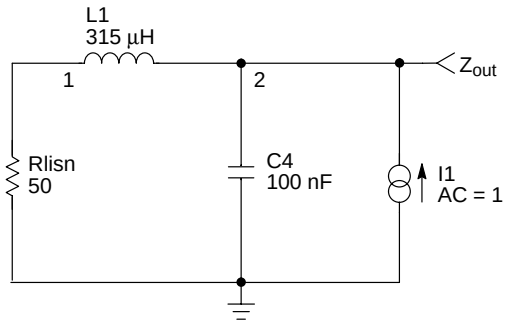

Figure 4e. By fixing the AC current source to 1 A, the voltage probe Zout directly gives ohms

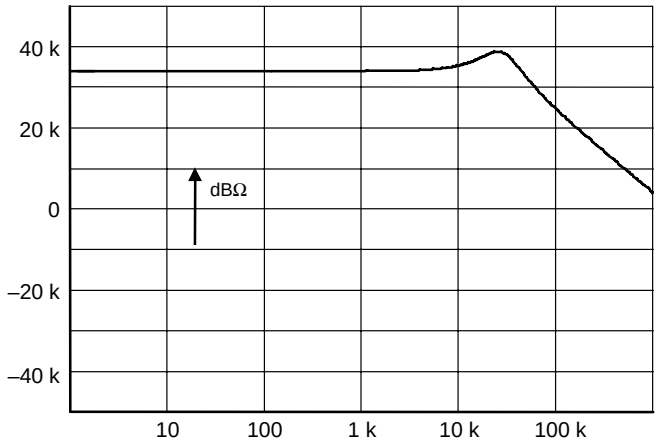

Figure 4f. This voltage plot show an output impedance affected by a low peaking

The exercise can be completed by sweeping the input impedance of the supply through its average model and pasting the results on figure 4e graph: there should be no overlap between the plots. Also the 50Ω impedance is a simplistic mains impedance representation and might obviously change depending on your local network arrangement. Different sweeps shall be carried on the LC filter to ensure a final low peaking. If the peaking is really strong, additional damping elements should be installed to decrease the filter Q.

The Final Filter Stage

We now have the choice to combine a CM filter together with a single inductor for the DM currents. As described in Figure 3d, we can also select a CM filter inductance knowing its leakage inductance and take benefit from it for DM cure. For a DM inductance below 500 µH, a 27 mH CM inductor can be a good choice. However, we need to precisely evaluate the available leakage inductance. With a 1:1 ratio, differential currents cancel the internal field. As a result, why not connecting together the dotted ends of the choke and letting naturally circulate differential currents while measuring the inductance . . . This is what is proposed by Figure 5a.

Figure 5b finally gives you the final impedance plot of the leakage inductor, showing again various stages: resistive in the lower portion, inductive in the medium portion and finally capacitive for higher frequencies. At 100 kHz, we can read 48 dBΩ or a 250 Ω impedance. The final calculation leads to an inductance of 398 µH or twice 199 µH when split into two components. Figure 5c gives its equivalent SPICE model with ohmic losses measured with a 4–wire multimeter.

Below stand measurement results comparing CM inductors provided by two different manufacturers:

Schaffner RN1140–08/2:
Lopen = 23 mH, Lleak = 238 µH or 2 x 119 µH.

Siemens B82723A2102–N1
Lopen = 31 mH, Lleak = 398 µH or 2 x 200 µH.

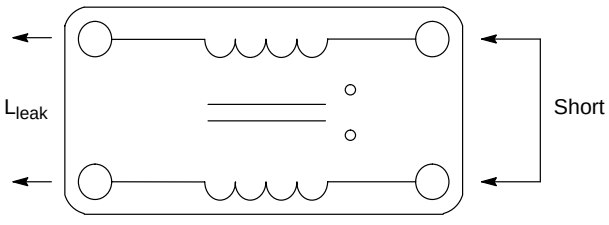

Figure 5a. Shorting the dot–ended windings gives you the value of the total leakage inductance.

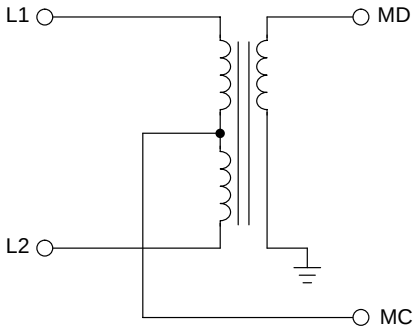

Figure 6a. A transformer to extract DM from CM.

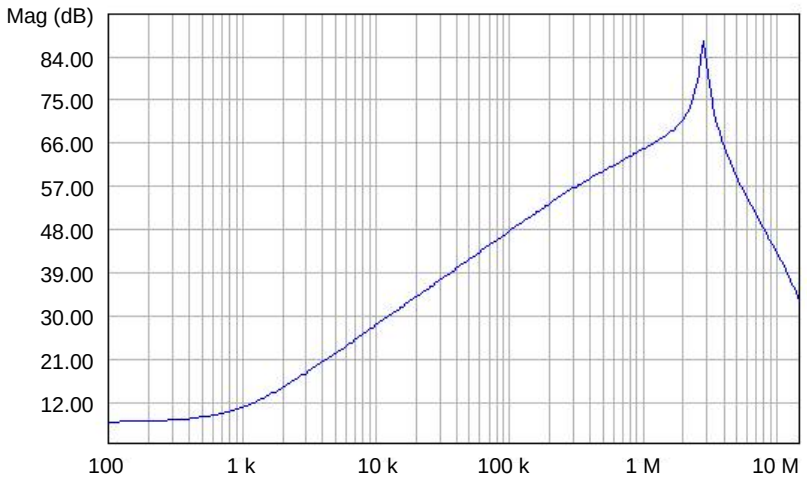

Figure 5b. A leakage inductance also welcomes parasitic elements.

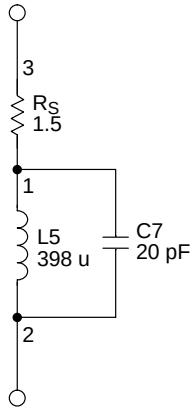

Figure 5c. These elements can be modeled using SPICE.

As you can imagine, combining the 100 nF–X2 capacitor (who also has parasitic elements) together with a Figure 5d–like inductor will deliver a result different from what we expect. Actually, the best would be to assess the final attenuation from the input of the filter (where the diode bridge connects) to the final output of the EMI receiver. SPICE does it in a snap–shot as shown by Figures 5d and 5e:

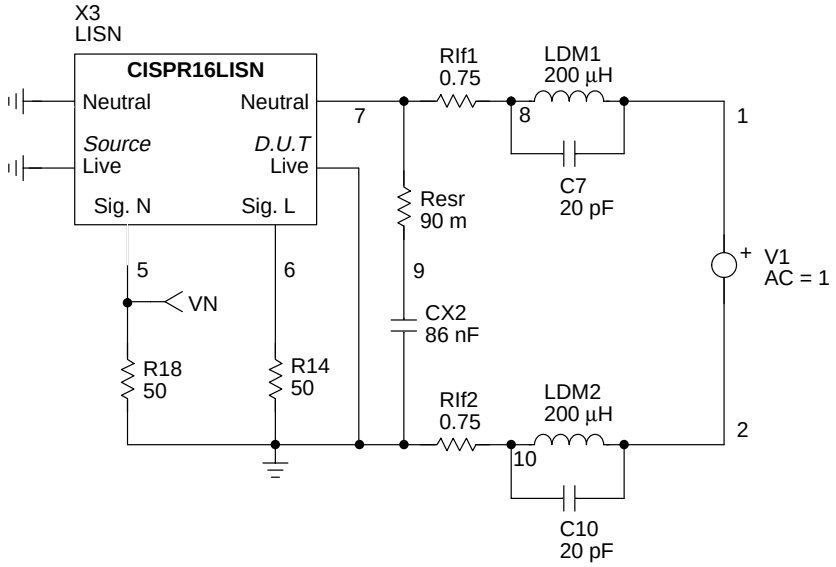

Figure 5d. This sketch lets you evaluate the filter attenuation once loaded by the LISN device.

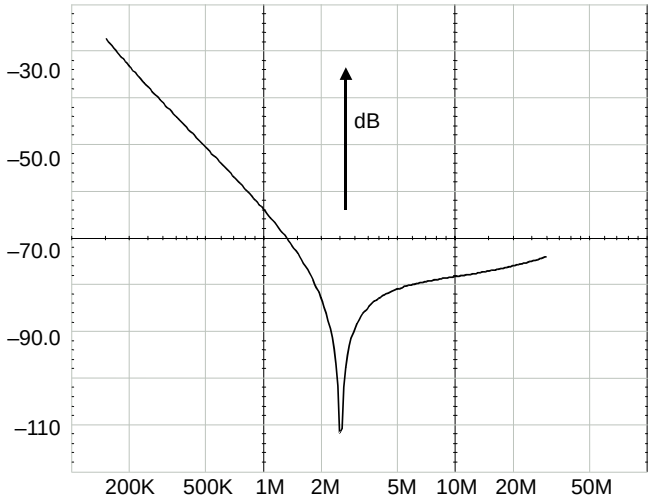

Figure 5e. The resulting final attenuation versus frequency.

As you can observe on Figure 5e, the rejection tends to degrade at higher frequencies due to the presence of parasitic components. But our attenuation at 190 kHz is 33 dB, enough to theoretically pass the DM test.

Let's now plug all these elements in Figure 4b test fixture and run a new test. Figure 5f shows how to install these elements before the LISN while Figure 5g plots the final results:

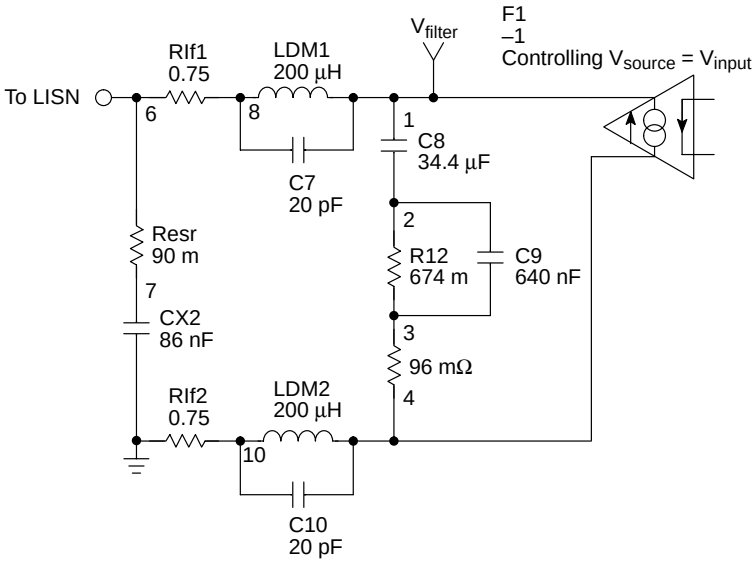

Figure 5f. This sketch shows how the filter finally behaves once loaded by the LISN device.

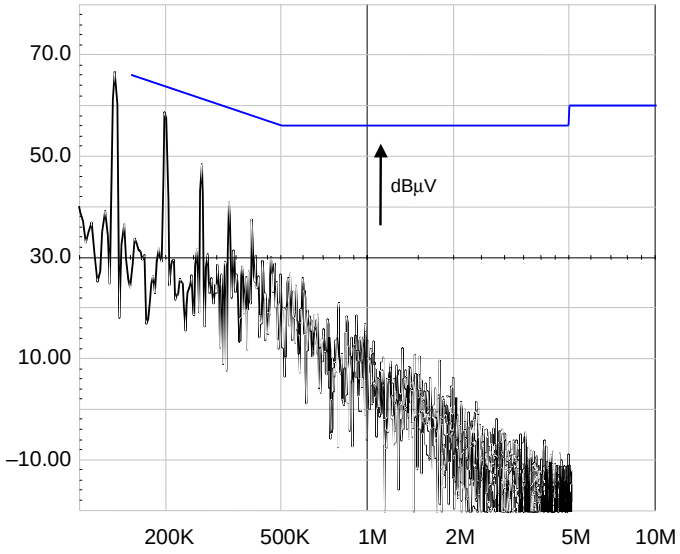

Figure 5g. The resulting spectrum confirming the filter action.

On the paper, we pass the test for DM measurements . . .

Real Measurements Versus Simulated Ones

Using the aforementioned approach, we are able to design a filter in a few iterations providing the computer is fast enough when running SPICE. But this approach is not worthwhile if true measurements on a board reveal large discrepancies. First of all, we must be able to extract differential mode from common mode noise. Unfortunately, standards fix limits regarding the total noise level (CM + DM) available on either L1 (live) or N (neutral), a switch routing either line to the receiver. To allow the study of both noise contents, we have modified a Rhode & Schwarz LISN (ESH–3) to which we added a second separated output. A switch simply loading one of the lines while running the final measurement on the other one. We now have L1 and N separated. If DM currents circulate 180° out of phase on the lines, summing L1 and N signals theoretically gives 0 while you obtain twice the CM level. At the opposite, subtracting the signals cancels CM and gives twice the DM. One limitation however exists: the impedance offered by both lines shall be perfectly equilibrated over the frequency range of interest, otherwise the rejection ratio will change . . . We have used an AEMC (Seyssins, France) DM/CM extractor (reference [2]) to perform our tests (Figure 6a). Figure 6b plots the DM quasi–peak SMPS signature without any EMI filter obtained with a Rhode & Schwarz ESPC EMI receiver. These results should be compared to Figure 4d drawing. The error on the main peak is only 8 dBs while the remaining peaks are not far away. Also quasi–peak measurements deliver levels lower than with a peak detector. Keep in mind that the DM/CM extractor ensures a good rejection up to 1 MHz (60 dB) while it tends to degrade in the higher portion. But the overall result is encouraging.

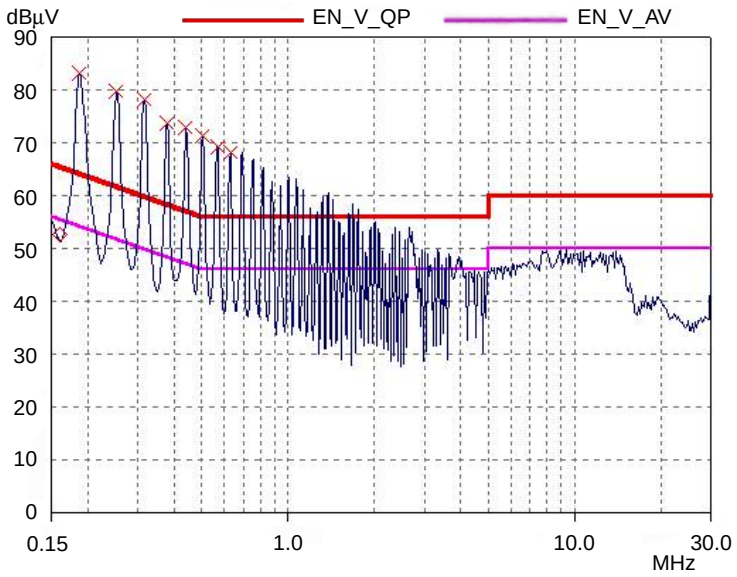

Figure 6b. The DM–only SMPS signature when operated without any EMI filter (quasi–peak detector).

Let's now connect our 27 mH CM inductance with a 100 nF–X2 capacitor over the line, as suggested by Figure 3d. If this capacitor needs to be increased above 100 nF, a discharge path has to be provided to avoid electrical shocks when touching the terminals immediately after unplugging the supply (IEC–950 defines a time constant less or equal to 1s). The final DM measurement is given by Figure 6c and confirms an attenuation of 35 dB at 190 kHz, exactly what we were looking for. The margin we have here is better than what we obtained in simulation, probably because of the quasi–peak internal time constants used during measurements.

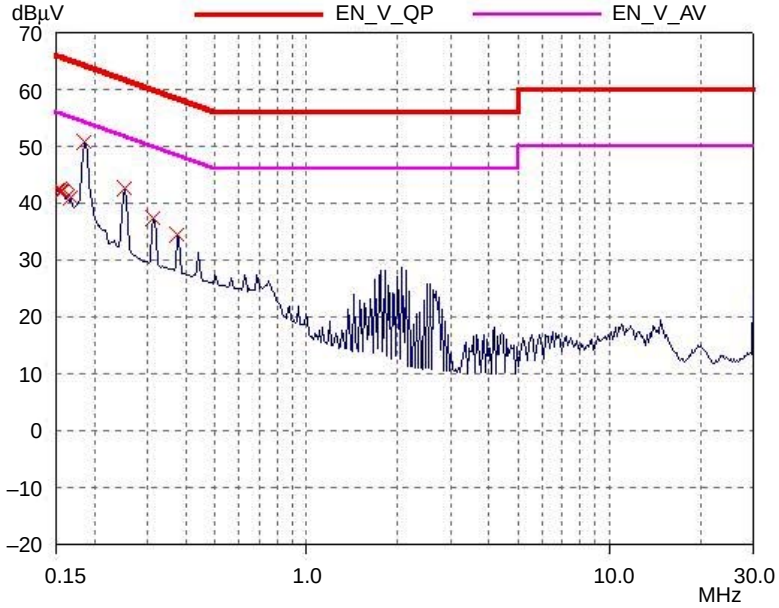

Figure 6c. The final quasi–peak DM–only measurement carried with an EMI receiver.

Total Noise Measurement

We now know that DM levels are within the limits. To attenuate the CM noise, we can wire a Y–type capacitor between the primary and the isolated ground as suggested by Figure 3d. For a two–wire applications, the IEC950 standard limits the maximum leaking current to less than 250 µA at 250 VAC power supply. The maximum capacitor value you can use is thus: Zmin = 250 V/250 µA = 1 MΩ. With a

50 Hz mains frequency, the Y capacitor cannot exceed $\frac{1}{2 \cdot \pi \cdot 50 \cdot 1E6}$ = 3 nF @ 50 Hz or 2.6 nF @ 60 Hz. Start by wiring a 1 nF capacitor or two 2.2 nF in series if you want to reinforce the security in case one of the Y capacitors would fail short. Figure 6d shows the final CM + DM plot in quasi–peak and clearly testifies for the CISPR22 compliance. This measurement was also successfully carried in average at worse operating conditions (100 VAC, 10 W).

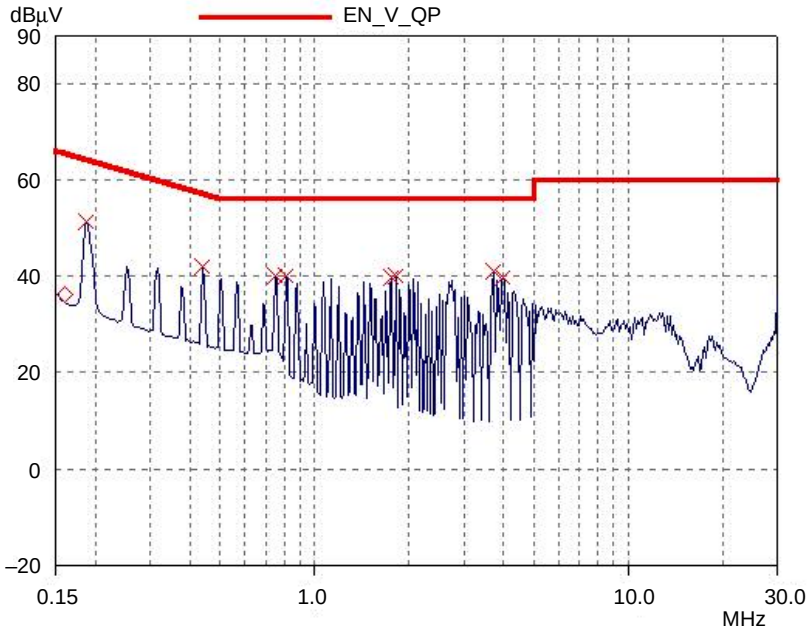

Figure 6d. The final composite QP plot carried over one line while the other is loaded (230 VAC, Pout = 10 W).

If the test would fail in common–mode, an option is to raise the CM inductor. Otherwise, you need to identify how noisy nodes can induce disturbances in adjacent copper traces or through the air. Carefully look at the rising time on the drain, how the output diode eventually rings, and various other unwanted ringing that could be snubbered by an RC network. As an advantage, the NCP1200 offers a controlled turn–on thanks to an asymmetrical output stage. Figure 7a shows how you normally slow–down the MOSFET during turn–on and speed up its discharge for turn–off. Figure 7b depicts how the NCP1200 output stage has been designed to save these two extra components. The driver's impedance at turn–on is about 40 Ω typically while it drops to 12 Ω for the turn–off phase. Figure 6d plot has been captured without any resistor in series with the MOSFET gate.

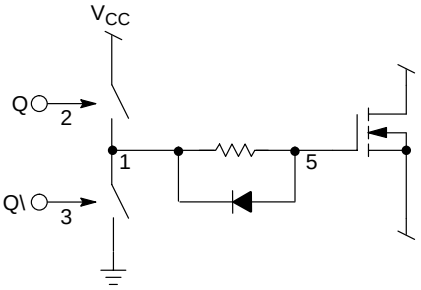

Figure 7a. A standard driver configuration needs external components to slow down the MOSFET without degrading the turn–off.

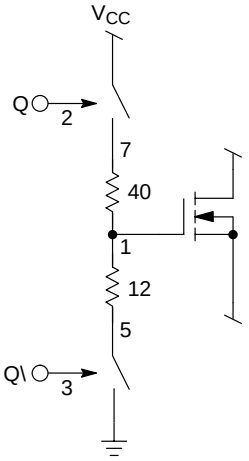

Figure 7b. The NCP1200 already integrates two resistors which avoid adding any other components.

Figure 8 portrays a complete working 10 W application example featuring an EMI filter.

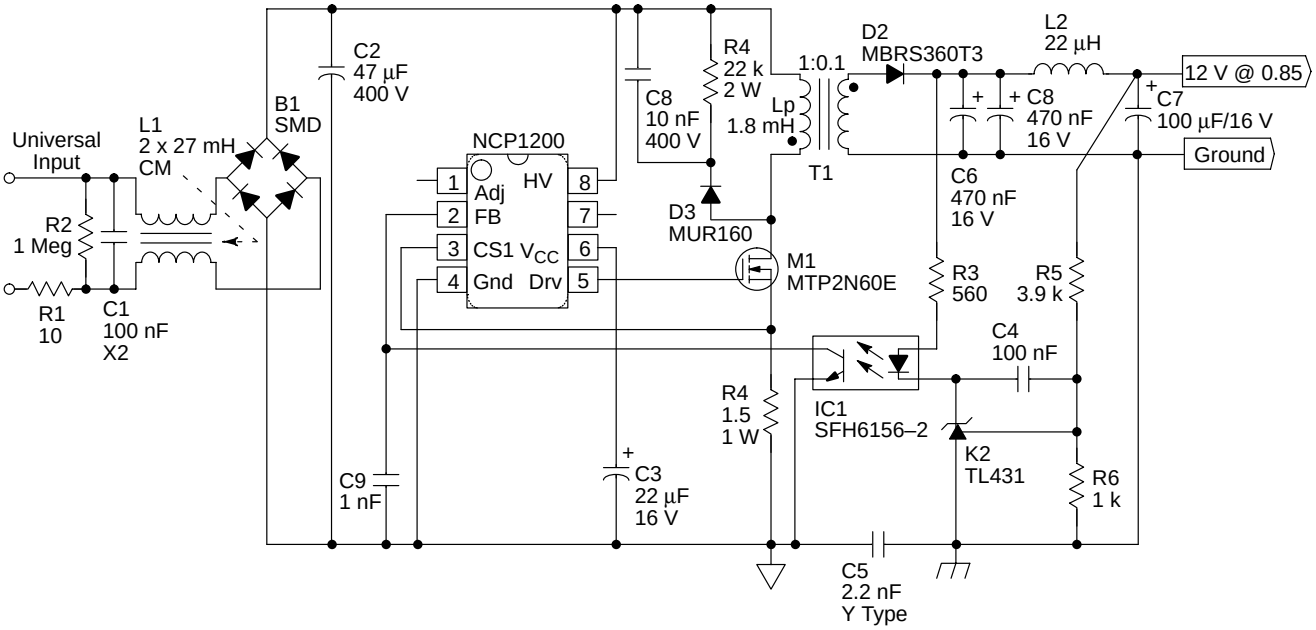

Figure 8. A complete 10 W AC/DC wall adapter featuring an EMI filter.

References

1. C. BASSO, “Spice predicts differential conducted EMI from switching power supplies”, EDN February 3, 1997.

2. AEMC, 86 rue de la Liberté 31180 SEYSSINS France. Tel. 33 (0)4 76 49 76 76, Fax. 33 (0)4 76 21 23 90.

3. T. WILLIAMS, “EMC for product designers”, Butterworth–Heineman, 1992, ISBN 0 7506 1264 9.

Line Impedance Stabilization Network SPICE Netlist:

```
.SUBCKT LISN mainsN mainsL1 measN measL1 L1 N
*
L4 measL1 1 100nH
R9 1 0 1k
C7 1 2 1uF
L5 2 3 1.75mH
R10 3 0 100m
C8 2 L1 1uF
L6 L1 6 50uH
R11 6 7 10m
R12 7 8 3.33
C9 8 0 8uF
C10 7 0 10n
L7 7 10 250uH
R13 10 mainsL1 10m
C11 mainsL1 0 2uF
R3 mainsL1 0 100m
C4 measN 0 10pF
L2 measN 11 100nH
R5 11 0 1k
C5 11 12 1uF
L3 12 13 1.75mH
R6 13 0 100m
C12 12 N 1uF
L8 N 16 50uH
R7 16 17 10m
R8 17 18 3.33
C13 18 0 8uF
C14 17 0 10n
L9 17 20 250uH
R14 20 mainsN 10m
C15 mainsN 0 2uF
R17 mainsN 0 100m
.ENDS
*********
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Notes

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