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High Performance, Precision Analog Capability Enabled by the Treo Platform

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High Performance, Precision Analog Capability Enabled by the Treo Platform

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Introduction

This paper focuses on the analog capabilities which are part of the **onsemi** Treo platform. The PPA triangle concept is being introduced to compare analog key indicators between process technologies. Overall, it will be shown that the **onsemi** Treo platform, based on a 65 nm BCD process technology, allows **onsemi** to be highly competitive in analog, mixed-signal and high-voltage BCD solutions.

The PPA Triangle

Power, performance and area (PPA) are three key indicators that characterize the capability of a wafer process technology:

- *Power* is the power consumed by an integrated circuit. It is determined by the supply voltage and the current consumption.
- *Performance* refers to the bandwidth or operating frequency of a circuit. Performance can also refer to accuracy or resolution, or to on-resistance of high-voltage devices.
- *Area* is the silicon area occupied by the integrated circuit.

Low power consumption, high performance (or smallest resolution, when expressed in mV/LSB) and low silicon area characterize the competitiveness of a circuit designed in a given process technology. These three variables create a fundamental trade-off during circuit design. For instance, when performance is enhanced, it may come at the cost of more power consumption and die size, or when die size is reduced, it may result in a lower performance. Depending on the circuit, different trade-offs exist, resulting in different circuit optimizations.

Power, performance and area characteristics of a process technology and their optimal combination also differ between technology nodes. Circuits designed in a smaller process node typically allow optimization towards a better overall PPA score, meaning more performance for less area and less power consumption.

Traditionally, the PPA figure of merit is expressed by following equation:

$$\text{PPAFOM} = \frac{\text{Performance}}{\text{Area} \times \text{Power}}$$

The overall PPA score is higher as performance increases and area and power consumption decrease.

Another way to represent the scaling effects between technology generations in a visual way, is by means of a triangle (in 2D) or a pyramid (in 3D). In Figure 1, the overall performance is represented on 3 axes.

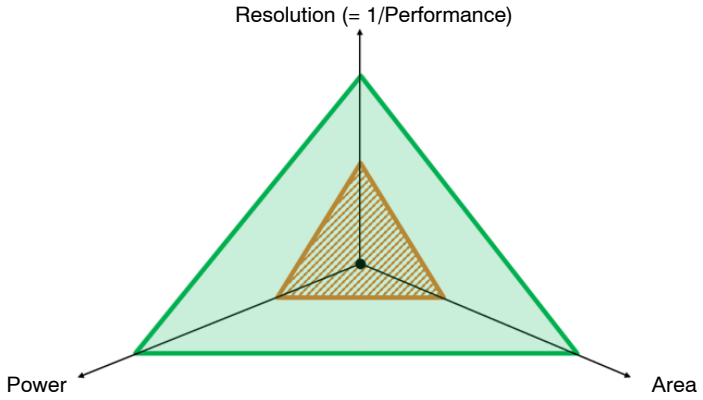

Figure 1. PPA Triangle as Figure of Merit of a Process Technology

One axis represents resolution, where the ideal circuit realizes the smallest possible resolution (zero resolution corresponds to an infinitely accurate system). A second axis represents silicon area, where the ideal circuit provides the function with infinitely small area. The third axis represents power consumption, where the ideal circuit delivers the function with infinitely small power. Realistically, every circuit needs a certain silicon area and power consumption, and realizes a finite resolution larger than zero.

The volume of the pyramid defined by the origin and the PPA triangle, as depicted in the 3D plot in Figure 1, expresses the competitiveness of the process technology. When comparing PPA between circuits and technology nodes, the closer the corners of the PPA triangle are located to the center, the better the PPA score of the circuit is. The ultimate process technology has infinitely small power consumption, silicon area and resolution.

In this representation, the overall performance is determined by the volume of the pyramid:

$$\text{PPA pyramid volume} \sim \frac{\text{Area} \times \text{Power}}{\text{Performance}}$$

The pyramid is a visual way to estimate the quantity of the resources needed to realize a certain performance.

PPA as Metric for BCD65

In this paper, a comparison is made between the **onsemi** Treo platform, a 65 nm BCD process technology (BCD65 – 2.5 V) and a previous process node (180 nm – 3.3 V / 5 V) using PPA as a figure of merit. By comparing technology parameters and characteristics, the impact of the chosen process technology on power, performance and area is clarified and the improvements seen towards BCD65 are discussed. Analog IP already designed in BCD65 or ported from a 180 nm to 65 nm process provides evidence of the actual PPA improvement. Real circuit examples are discussed and compared.

The **onsemi** Treo platform also offers high-voltage devices in the 5 V – 90 V operating range. Low Rsp (specific on-resistance, in $m\Omega * mm^2$) DMOS devices can be integrated together with 65 nm low-voltage analog and digital circuitry on the same die. This combination of low-, medium- and high-voltage capability is highly differentiated for a 65 nm BCD technology.

With PPA as figure of merit, this paper shows that on average at least a 5x integral improvement on analog circuits is reached by moving from 180 nm – 3.3 V / 5 V to 65 nm – 2.5 V. By doing so, **onsemi** is in the position to lead the way in BCD applications and realize an excellent combination of power, performance and area.

The following sections elaborate on each of the three key indicators.

Power Consumption

Process scaling includes scaling of the gate oxide thickness. A thinner gate oxide requires a lower operating supply voltage. For BCD65, the typical analog low voltage supply is 2.5 V, whereas 3.3 V or 5 V is often used in older BCD technology nodes such as 110 nm / 130 nm or 160 nm / 180 nm. This low voltage supply implies a 25% to 50% reduction of a circuit's power consumption (at the same current consumption), which is already an important contributor to the PPA score improvement. As the transistor threshold voltage (V_{TH}) typically also reduces, previous circuit topologies do not necessarily need to change, and reuse of circuit topologies remains generally possible.

At the 65 nm node, the current consumption in analog circuits is also typically lower for a similar performance. Lower bias currents can be applied while keeping the same bandwidth and gain: relative parasitic capacitances strongly reduce, and equal transconductance can be obtained at lower current. This was demonstrated by porting IP from 180 nm – 3.3 V to 65 nm – 2.5 V at equal performance.

Digital circuits operate at a nominal voltage of either 2.5 V (thick gate flow) or 1.2 V (thin gate flow). This was 3.3 V respectively 1.8 V in the 180 nm node. The equation below shows that an important saving in digital power consumption is possible when W, L, t_{ox} and V_{dd} scale down. (Note, t_{ox} scaling has an opposite effect but is overcompensated by scaling sizes and supply voltage). Especially in the 1.2 V process flow, W_{min} and L_{min} scale down considerably. Then, there's also room to increase the operating frequency.

$$Pdiss = f \times C_{gate} \times vdd^2 = f \times W \times L \times \frac{\epsilon_{ox}}{t_{ox}} \times Vdd^2 \qquad \text{(eq. 1)}$$

Silicon Area

A significant area scaling per function (analog, digital, high-voltage power) is seen when moving from the 180 nm node to the 65 nm node.

For analog low voltage circuits, this was demonstrated by porting a set of generic circuits to BCD65 (in the thick gate oxide flow), while keeping similar performance. To keep the comparison valid, the same amount of metal layers and the same set of standard devices were used. The result was roughly a 50% analog low voltage area reduction in BCD65.

Figure 2 shows a 45% scaling factor between 180 nm – 3.3 V and BCD65 – 2.5 V for a comparator circuit.

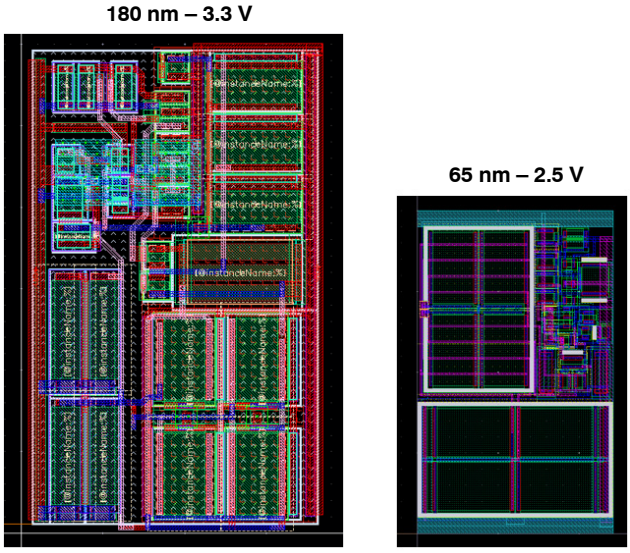

Figure 2. Layout Scaling of a Comparator Circuit Between Process Nodes

This analog (and mixed signal) low voltage shrink at similar accuracy not only provides an improvement in die cost, but also allows the integration of many more functions in a smaller assembly footprint.

These analog and mixed signal shrink factors are made possible because of the following contributors:

- In semiconductor processes, a smaller process node generally results in improved matching of the transistor threshold voltage (Vth). The mismatch coefficient, which is a process dependent parameter, is then lower. According to Pelgom's law, the gate area of matched transistors is then decreasing for the same level of mismatch. Comparison of the threshold voltage mismatch coefficients between a 180 nm – 5 V process and 65 nm BCD – 2.5 V shows a gate area scaling in matched transistor structures of at least a factor two. A limited improvement is seen between 180 nm – 3.3 V and 65 nm – 2.5 V.
- The BCD65 standard poly resistor shows a lower mismatch coefficient compared to both the standard poly and the high-resistance poly resistor of **onsemi**'s 180 nm BCD technology. Along with smaller spacing between units, the area of matched resistor banks is more than 40% smaller.
- Poly-Nwell capacitors have a smaller area for the same absolute value, compared to **onsemi**'s 180 nm BCD technology. The gate oxide capacitance density, which is inversely proportional to the oxide thickness, is 30% higher in BCD65 (in the thick gate flow).
- On top of the shrinking poly area, device density further increases because BCD65 design rules allow smaller spacing between devices. Transistor sources, drains and gate connections take up less area and contacts are almost 6x smaller in area.
- Bipolars are smaller and show excellent matching.
- BCD65 provides a strong scaling in device interconnect and signal routing. Backend design rules allow for a smaller pitch (smaller minimum metal width and spacing) along with (almost 7x) smaller vias. This does not necessarily cause a larger interconnect impedance: the BCD65 metal stack uses damascene copper wires having 35% less resistance compared to aluminum. Routing has typically shorter distances.
- BCD65 offers a tapered metallization, providing narrow, high-density interconnect lines at the lower metal layers, and gradually wider and thicker routing in the higher layer metals for high current capability, supply routing and power. Routing density is furthermore only limited by certain line to line spacing rules at higher voltages.
- Another significant difference is the area taken up by device isolation (BCD65 low voltage uses junction isolation) compared to a 180 nm – 5 V technology.

- Digital libraries provide smaller digital standard cells, resulting in a strong scaling of digital circuitry. This is realizing a 3x digital gate density improvement (comparing the thick gate oxide flows) and a 6x improvement (comparing the thin gate oxide flows). Much more digital content can easily be added in an integrated circuit.
- Electro-static discharge (ESD) protections only show a minor scaling, as dimensions are determined by energy capability requirements.
- The Rsp value of high voltage devices improves significantly in BCD65. The 45 V DMOS device shows a 40% improvement compared to **onsemi**'s previous BCD technology.

The combination of all these contributors results in a significant scaling factor at product level. This was demonstrated by porting a product from the 180 nm BCD node to the **onsemi** Treo platform on the 65 nm BCD node.

Performance

Previous sections elaborated on the reduced power consumption and silicon area in BCD65 at a circuit performance similar to **onsemi**'s previous 180 nm BCD node. Vice versa, within the same power and area budget, circuits developed on the **onsemi** Treo platform perform better in terms of accuracy and bandwidth.

Better matched transistors, resistors and bipolars translate into a higher precision. For the same current consumption, circuits operate at higher gain bandwidth product. The tapered metallization, with narrow traces at the lowest Cu metal layers, as well as shorter distance routing, reduce interconnect parasitics which is also beneficial for circuits at higher bandwidth.

The low-K (low dielectric constant) material in the lower part of the metal stack enables high-speed operation, since parasitic coupling and cross talk noise are lower. Low-K material is in any case required for the continued scaling of process technologies and high-speed operation. The potential for higher clock speed in the digital was already shown in Equation 1, which is boosting the performance.

One can obtain another important bandwidth improvement by using the BCD65 dual gate option for analog design in the 1.2 V thin gate flow. Transistor matching once more improves in the thin gate flow, resulting in highly accurate parameters. Analog design in 1.2 V is particularly interesting for blocks that directly interface the digital, such as A/D and D/A converters, or comparators. Operation at higher frequencies allows analog-to-digital converters (ADC) to clock at higher sampling rate, which allows multiplexing of multiple input channels or reaching a higher over-sampling ratio (OSR), resulting in better resolution.

More functionality and advanced circuits are integrated within the same silicon area.

A strong digital scaling easily enables the addition of digital content including MCU capability. Digital functions can be used to enhance analog performance and implement corrections for analog imperfections.

PPA Integral Improvement in BCD65

Previous sections explained why the Treo 65 nm BCD outperforms 180 nm – 3.3 V / 5 V in terms of power, performance and area. Many qualitative statements on the different contributors were listed. This section shows the actual PPA improvement, based on real circuit examples.

Example 1

The design of an operational amplifier has been ported from **onsemi**'s 180 nm – 3.3 V BCD technology to BCD65. The topology is a widely used 2-stage amplifier known as the Miller op-amp. The ported circuit was designed for equal performance in terms of offset, bandwidth, relative input common mode range, etc… Circuit characterization after manufacturing shows that the function after porting is realized with 40% less current consumption from the 2.5 V supply rail. Note that the original circuit was supplied from a 3.3 V supply rail. The layout of both the original and the ported design are depicted in Figure 3 (where both circuit layouts are shown on the same scale).

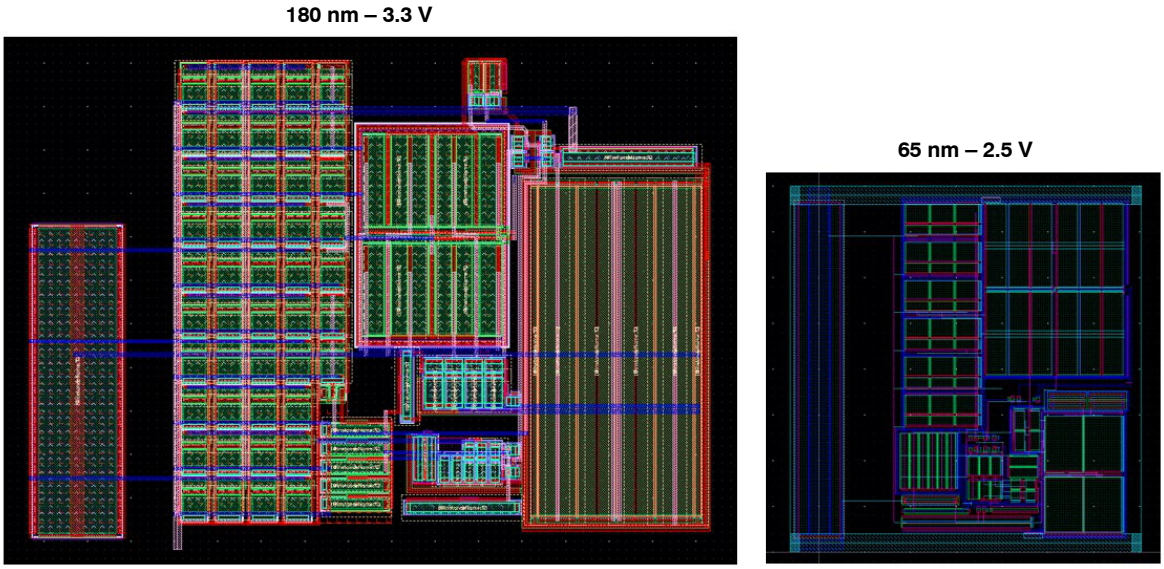

Figure 3. Layout Comparison of an Operational Amplifier

The comparison of key indicators and overall PPA is summarized in the table below:

Table 1. PPA COMPARISON FOR EXAMPLE CIRCUIT 1

Key Indicator	Example 1 Operational Amplifier in BCD65 Compared to 180 nm – 3.3 V
Supply Voltage	Factor 1.32 (= 3.3 V / 2.5 V) lower
Current Consumption	Factor 1.66 lower
Power	Factor 2.20 (1.32 x 1.66) lower
Performance	Equal
Area	43.1% scaling factor, or factor 2.32 lower
Overall PPA	Factor 5.1 improvement

For this operational amplifier design, a factor of 5.1 integral PPA improvement is reached by moving to 65 nm. The PPA triangle, for this circuit depicted in Figure 4, is another way of showing the improvement. The green volume represents the 180 nm – 3.3 V design, the orange volume represents the BCD65 design with equal performance and improved power consumption and silicon area.

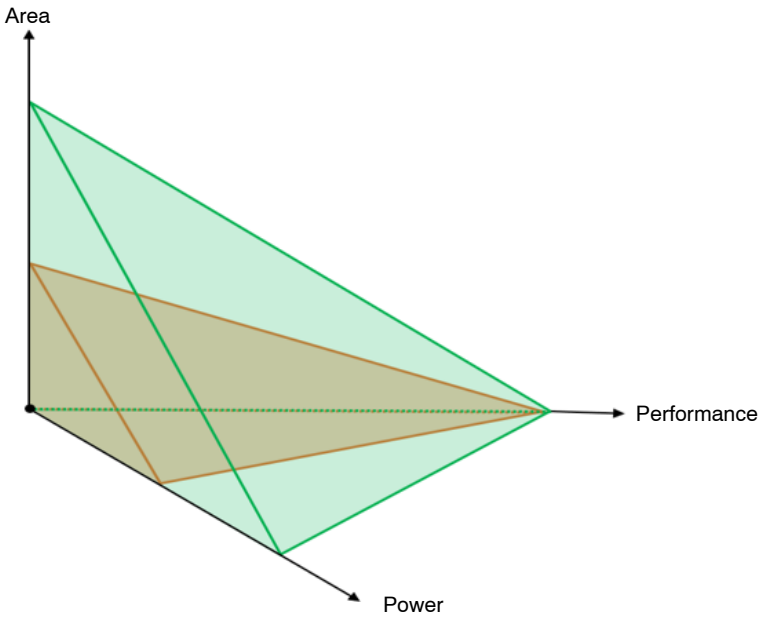

Figure 4. PPA Triangle for Operational Amplifier in 180 nm – 3.3 V (Green) and in 65 nm – 2.5 V (Orange)

Example 2

A comparator design has been ported from **onsemi**'s 180 nm – 5 V BCD technology to BCD65, with equal performance in terms of offset, propagation delay and relative input common mode range. Circuit characterization after manufacturing shows that the function after porting is realized with 31% less current consumption from a 2.5 V supply rail, whereas the original circuit was supplied from 5 V. The layout area of both versions is depicted in Figure 5 (with both circuit layouts shown on the same scale).

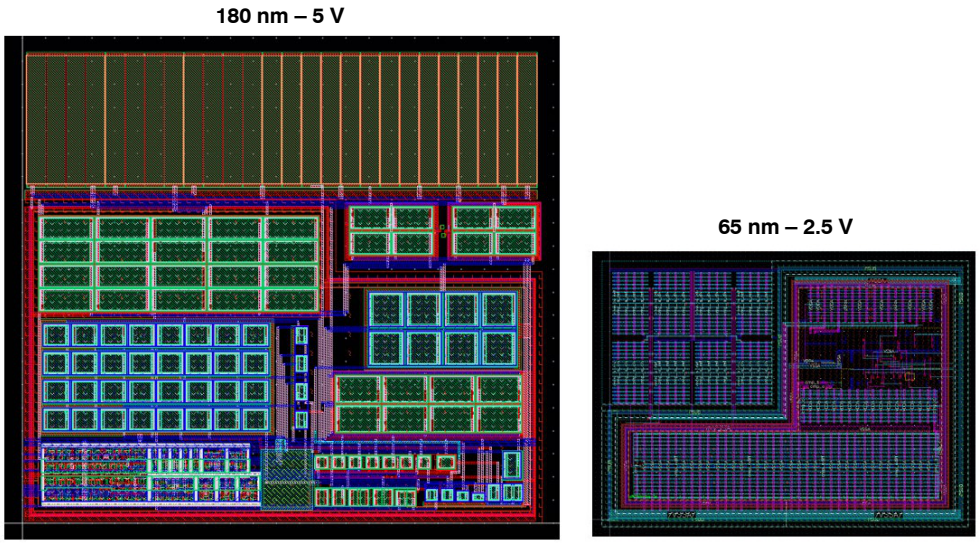

Figure 5. Layout of a Comparator Circuit in 180 nm and 65 nm

Table 2. PPA COMPARISON FOR EXAMPLE CIRCUIT 2

Key Indicator	Example 2 Comparator in BCD65 Compared to 180 nm – 5 V
Supply Voltage	Factor 2 (= 5 V / 2.5 V) lower
Current Consumption	Factor 1.46 lower
Power	Factor 2.92 (2 x 1.46) lower
Performance	Equal
Area	38.5% scaling factor, or factor 2.6 lower
Overall PPA	Factor 7.6 improvement

For this comparator circuit, a factor 7.6 integral PPA improvement is reached by moving to BCD65. The PPA triangle, for this circuit depicted in Figure 6, is another way of showing this improvement. Again, the green volume represents the 180 nm – 5 V design, the orange volume represents the BCD65 design with equal performance and improved power consumption and silicon area.

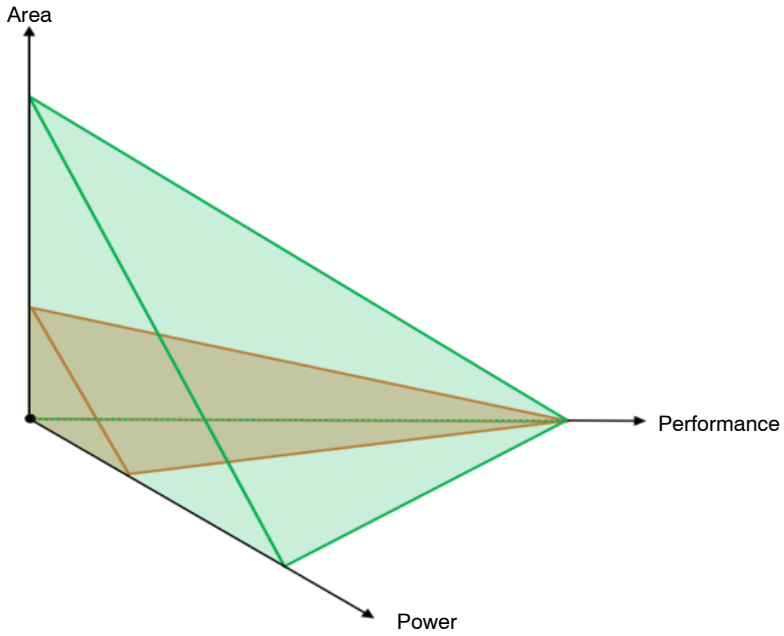

Figure 6. PPA Triangle for a Comparator Circuit Design in 180 nm – 5 V (Green) and in 65 nm – 2.5 V (Orange)

Depending on the circuit type, different integral improvement PPA numbers are reached. Some designs scale harder than others, or some only show a limited scaling in terms of silicon area or current consumption. On average though, a more than 5x integral PPA improvement is reached by moving from 180 nm – 3.3 V to BCD65. An even stronger improvement is obtained by moving from 180 nm – 5 V to BCD65, as the extra supply scaling brings additional benefit.

Conclusion

This paper describes the three key indicators power, performance and area, the trade-off that exists between them, and how PPA can be used as a metric to compare analog capabilities across process technologies. With PPA as figure of merit, it is shown that on average at least a 5x integral improvement is realized by moving from 180 nm – 3.3 V / 5 V BCD to the **onsemi** Treo platform. The add-on of high-voltage devices along with dense analog low-voltage and digital circuits, makes this **onsemi** Treo platform highly competitive for BCD applications.

The PPA improvements in the **onsemi** Treo platform are not just theoretical but are backed by practical evidence from ported and manufactured analog IPs. The process scaling allows for higher integration density, enabling more functions within a smaller footprint, which is crucial for modern high-performance analog and BCD applications.

Overall, the **onsemi** Treo platform positions **onsemi** to lead the way in analog, mixed-signal and high-voltage solutions by bringing to market products which offer superior performance, lower power consumption, and reduced silicon area, making it a highly competitive choice for advanced analog circuit design.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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