NB7NQ621M for Source and Sink Side Application

AND90182/D

INTRODUCTION

This application note gives a setting for meeting HDMI 2.1 TMDS and FRL Compliance when NB7NQ621M HDMI redriver is used on both Source and Sink Side using different I^2C settings.

The application note is to be used along with the NB7NQ621M Datasheet. This application note shows a method of implementation.

Background

Figure 1 shows a typical customer application setup connection. The FPGA is connected to Source TX and to the Sink RX of the NB7NQ621M redriver.

The system will require multiple settings and different operation data rate. NB7NQ621M has suitable I^2C register value at TMDS mode and FRL mode to meet the compliance.

FPGA have capability to dynamically detect the resolution rate as per the configuration of the NB7NQ621M redriver operating mode.
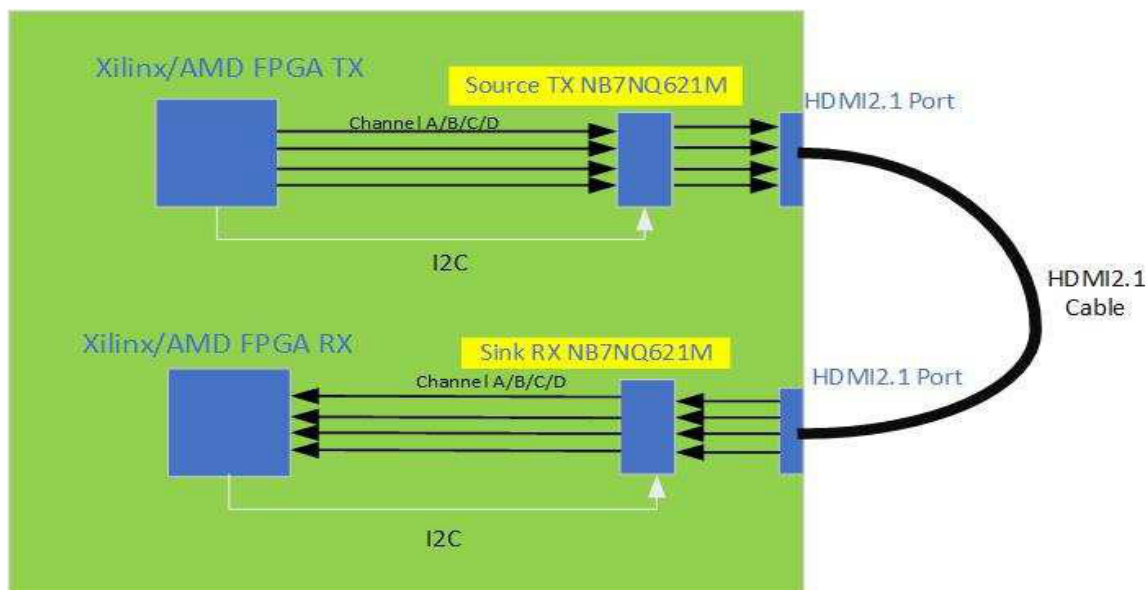

Figure 1. Typical Source Sink System Configuration

December, 2024 – Rev. 1

Publication Order Number:
AND90182/D

A Typical Source and Sink Side Schematic is shown below for reference. Figure 2 shows the Source Side Schematic and Figure 3 shows the Sink Side Schematic around the NB7NQ621M redriver.
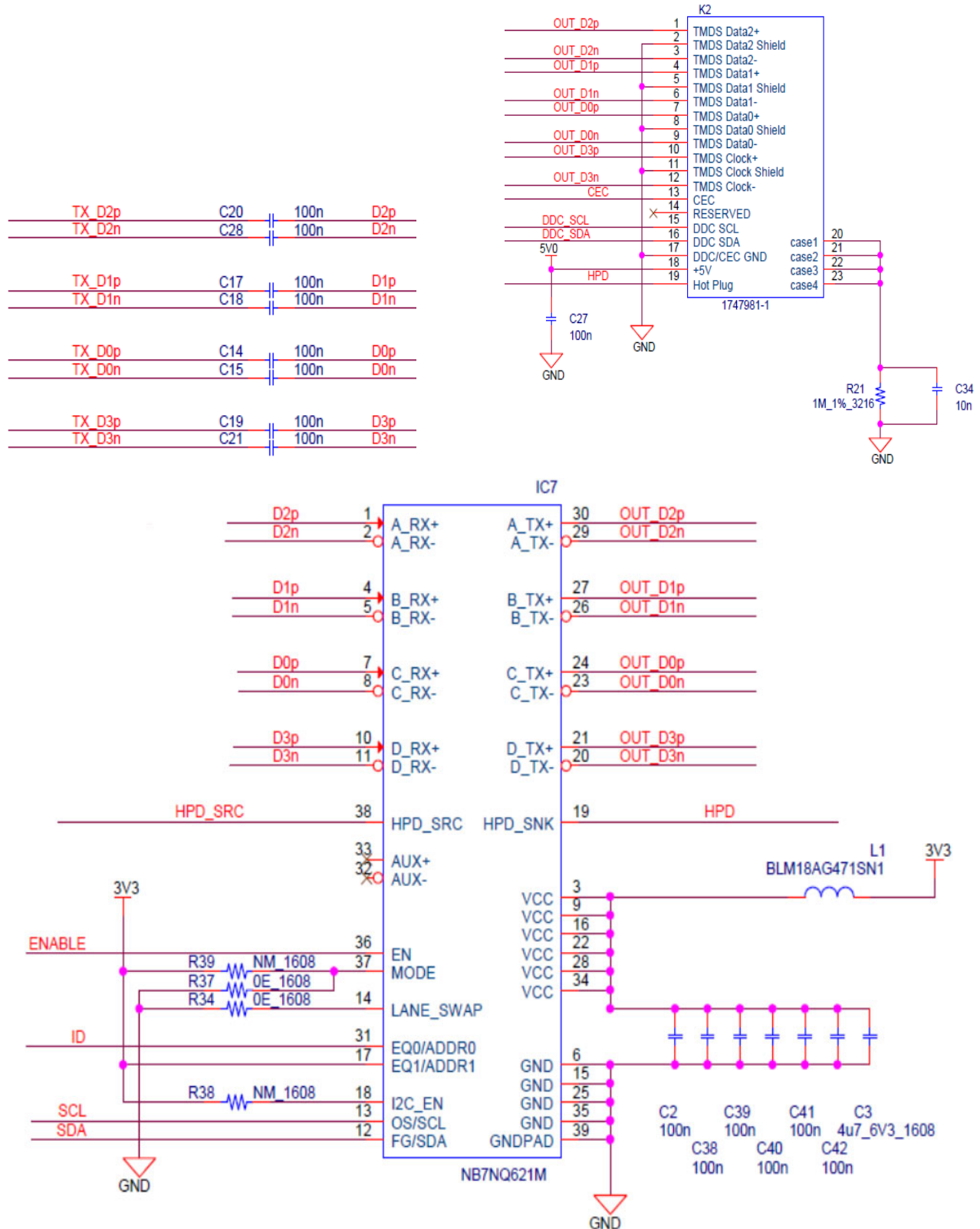
Source Side Schematic

Figure 2. Source Side Circuit

Sink Side Schematic
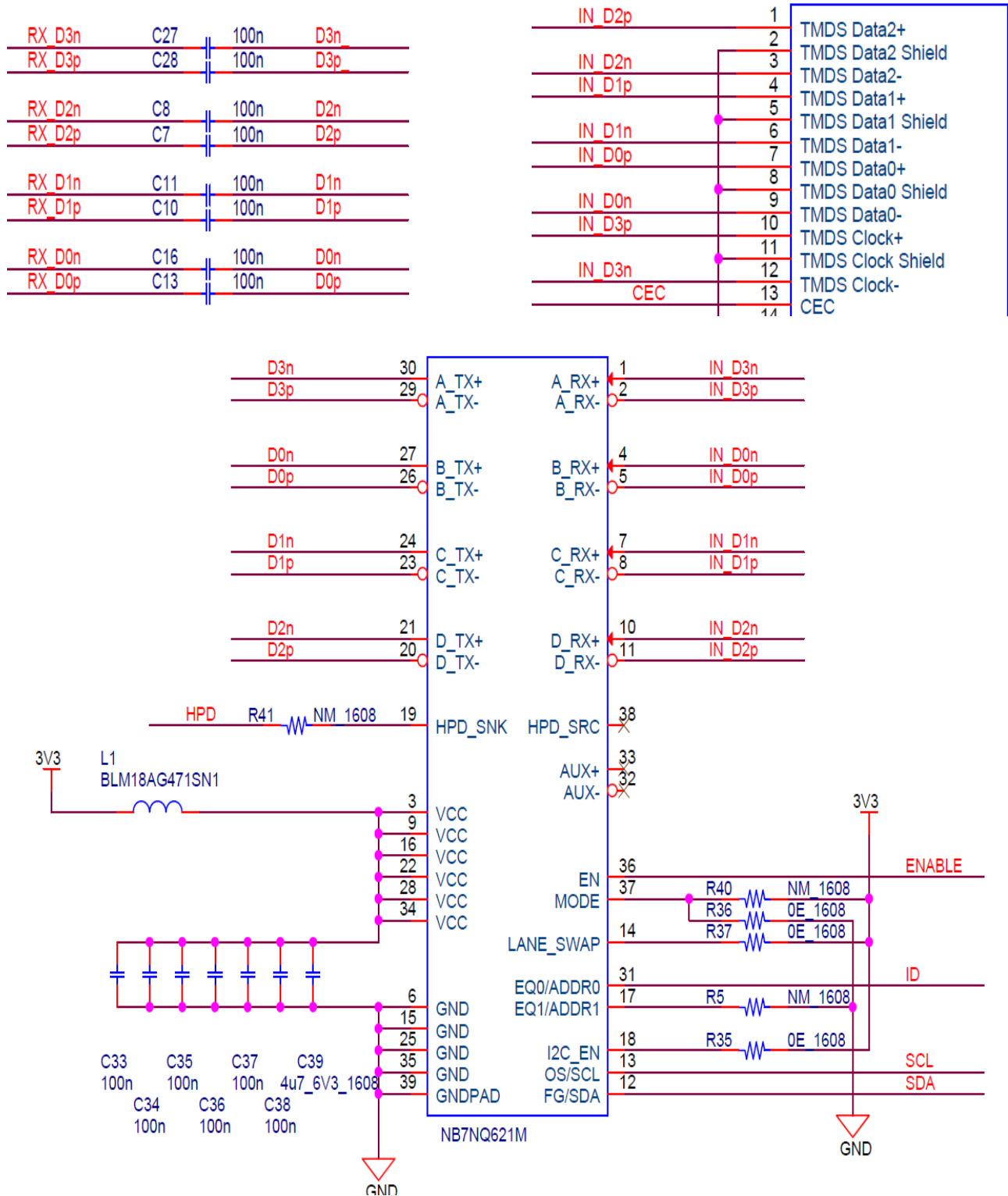

Figure 3. Sink Side Circuit

Given below Tables 1 to 4 showing the I^{2}C setting meeting the Compliance for the Source side TX Source and Table 5 to 7 showing I^{2}C settings for RX Sink Side meeting the Compliance for different Modes.

Table 1. NB7NQ621M I^{2}C SETTING FOR SOURCE TX HDMI 1.4 TMDS UNDER 1.65 Gbps DATA RATE

Register	Setting	Remarks
0x0A	04	Global control, Line to Line Hi−Z, Mode 0, Short circuit block disable
0x0B	0F	
0x0C	00	
0x0D	31	CLK FG = 4.5 dB, OS = 1200 mV
0x0E	03	CLK Slew Rate fast, EQ level 3
0x0F	31	Data FG = 4.5 dB, OS = 1200 mV
0x10	03	Data Slew Rate fast, EQ level 3
0x11	0F	
0x12	AA	
0x13	30	
0x14	0F	
0x15	00	
0x16	02	
0x17	63	
0x18	00	
0x19	00	
0x1A	03	
0x1B	00	
0x1C	00	
0x1D	03	
0x1E	00	

Table 2. NB7NQ621M I2C SETTING FOR SOURCE TX HDMI 1.4 TMDS 1.65 Gbps TO 3.4 Gbps DATA RATE

Register	Setting	Remarks
0x0A	0C	Global control, Line to Line 300 Ohms, Mode 1, Short circuit block disable
0x0B	0F	
0x0C	00	
0x0D	31	CLK FG = 4.5 dB, OS = 1200 mV
0x0E	03	CLK Slew Rate fast, EQ level 3
0x0F	31	Data FG = 4.5 dB, OS = 1200 mV
0x10	03	Data Slew Rate fast, EQ level 3
0x11	0F	
0x12	AA	
0x13	30	
0x14	0F	
0x15	00	
0x16	02	
0x17	63	
0x18	00	
0x19	00	
0x1A	03	
0x1B	00	
0x1C	00	
0x1D	03	
0x1E	00	

Table 3. NB7NQ621M I2C SETTING FOR SOURCE TX HDMI 2.1 TMDS 3.4 Gbps TO 6 Gbps DATA RATE

Register	Setting	Remarks
0x0A	1C	Global control, Line to Line 100 Ohms, Mode 3, Short circuit block disable
0x0B	0F	
0x0C	00	
0x0D	31	CLK FG = 4.5 dB, OS = 1200 mV
0x0E	03	CLK Slew Rate fast, EQ level 3
0x0F	31	Data FG = 4.5 dB, OS = 1200 mV
0x10	03	Data Slew Rate fast, EQ level 3
0x11	0F	
0x12	AA	
0x13	02	
0x14	0F	
0x15	00	
0x16	02	
0x17	63	
0x18	00	
0x19	00	
0x1A	03	
0x1B	00	
0x1C	00	
0x1D	03	
0x1E	00	

Table 4. NB7NQ621M I²C SETTING FOR SOURCE TX HDMI 2.1 FRL 12 Gbps DATA RATE

Register	Setting	Remarks
0x0A	24	Global control, FRL DC Coupling, Mode 4, Short circuit block disable
0x0B	0D	Disable HPD Automatic power down function
0x0C	00	
0x0D	31	CLK FG = 4.5 dB, OS = 1200 mV
0x0E	03	CLK Slew Rate fast, EQ level 3
0x0F	31	Data FG = 4.5 dB, OS = 1200 mV
0x10	03	Data Slew Rate fast, EQ level 3
0x11	0F	
0x12	AA	
0x13	00	
0x14	03	
0x15	00	
0x16	00	
0x17	03	
0x18	00	
0x19	00	
0x1A	03	
0x1B	00	
0x1C	00	
0x1D	03	
0x1E	00	

Table 5. NB7NQ621M I²C SETTING FOR SINK RX HDMI 1.4 TMDS UNDER 3.4 Gbps DATA RATE

Register	Setting	Remarks
0x0A	1C	Global control, Line to Line 100 Ohms, Mode 3, Short circuit block disable
0x0B	0D	Disable HPD Automatic power down function
0x0C	00	
0x0D	00	CLK FG = 0 dB, OS = 1000 mV
0x0E	03	CLK Slew Rate fast, EQ level 3
0x0F	21	Data FG = 1.5 dB, OS = 1200 mV
0x10	2A	Data Slew Rate fast, EQ level 10
0x11	0F	
0x12	00	
0x13	00	
0x14	03	
0x15	00	
0x16	00	
0x17	03	
0x18	00	
0x19	00	
0x1A	03	
0x1B	00	
0x1C	00	
0x1D	03	
0x1E	00	

Table 6. NB7NQ621M I²C SETTING FOR SINK RX HDMI 2.1 TMDS 3.4 Gbps TO 6 Gbps DATA RATE

Register	Setting	Remarks
0x0A	1C	Global control, Line to Line 100 Ohms, Mode 3, Short circuit block disable
0x0B	0D	Disable HPD Automatic power down function
0x0C	00	
0x0D	00	CLK FG = 0 dB, OS = 1000 mV
0x0E	03	CLK Slew Rate fast, EQ level 3
0x0F	21	Data FG = 1.5 dB, OS = 1200 mV
0x10	2A	Data Slew Rate fast, EQ level 10
0x11	0F	
0x12	00	
0x13	00	
0x14	03	
0x15	00	
0x16	00	
0x17	03	
0x18	00	
0x19	00	
0x1A	03	
0x1B	00	
0x1C	00	
0x1D	03	
0x1E	00	

Table 7. NB7NQ621M I²C SETTING FOR SINK RX HDMI 2.1 FRL 12 Gbps DATA RATE

Register	Setting	Remarks
0x0A	24	Global control, FRL DC Coupling, Mode 4, Short circuit block disable
0x0B	0D	Disable HPD Automatic power down function
0x0C	00	
0x0D	21	CLK FG = 1.5 dB, OS = 1200 mV
0x0E	01	CLK Slew Rate fast, EQ level 1
0x0F	21	Data FG = 1.5 dB, OS = 1200 mV
0x10	01	Data Slew Rate fast, EQ level 1
0x11	0F	
0x12	33	
0x13	21	
0x14	00	
0x15	00	
0x16	21	
0x17	00	
0x18	00	
0x19	21	
0x1A	00	
0x1B	00	
0x1C	20	
0x1D	07	
0x1E	00	

Additional Guidelines

In addition to the above settings, below guidelines also need to be followed for passing compliance:

- For passing HFR 2−1, HFR 2−2 and HFR 2−3 Sink HDMI 2.1 Intrapair skew and Inter pair skew, the data path of layout between the intra pair and inter pair skew must under 2 mil. Also, the component pad must be etched at reference plan. An example Layout routing is shown in Figure 5 below.
- The HDMI connector selected should be of the HDMI category 3 certification connector and also must be of the SMT type.

- There is no need in the system for tunning the FPGA PHY of firmware and software setting. We just need tunning the EQ, Flat gain and output swing setting of NB7NQ621M redriver depending on the channel signal quality.
- For the eye diagram pre−check, user can make use of the chipset IBERT IP tool for Eye Diagram Analyzer. Below Figure 4 photo shows an example tool screen If this is done, then there will be no need for use of Scope or BERT test before going to the certification test.
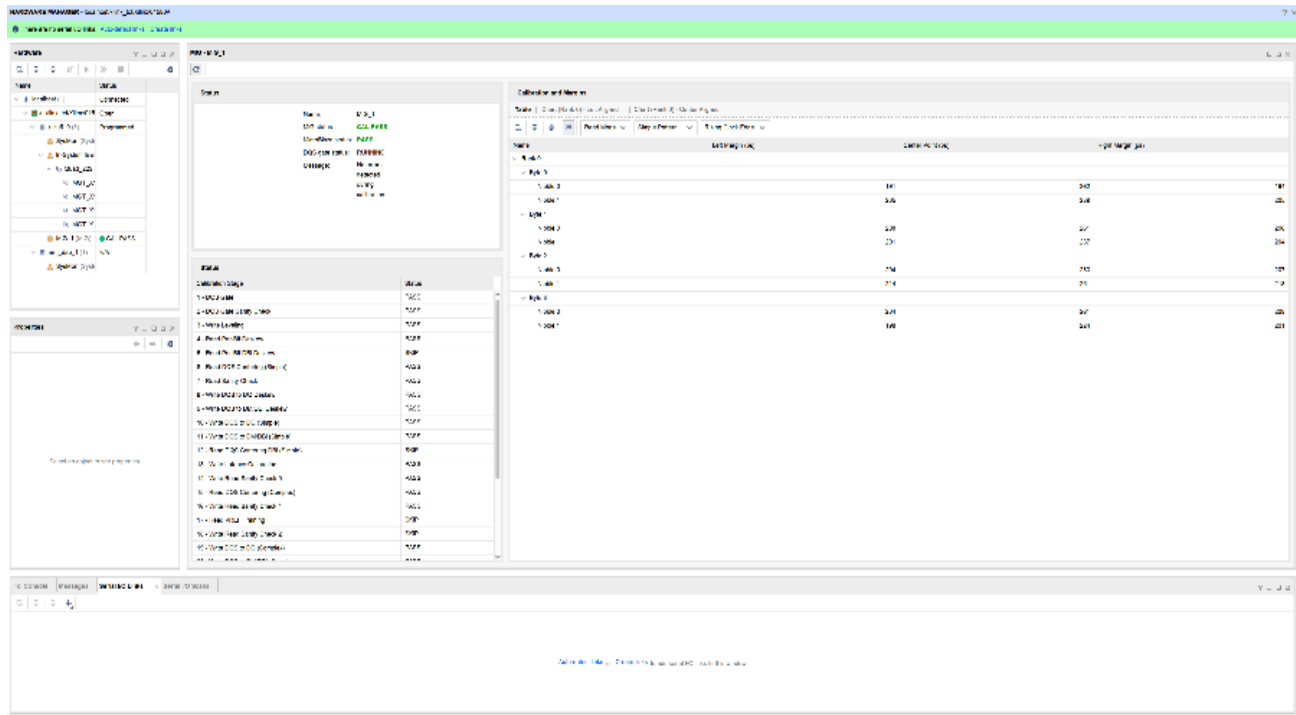
Figure 4. Sample IBERT IP Tool
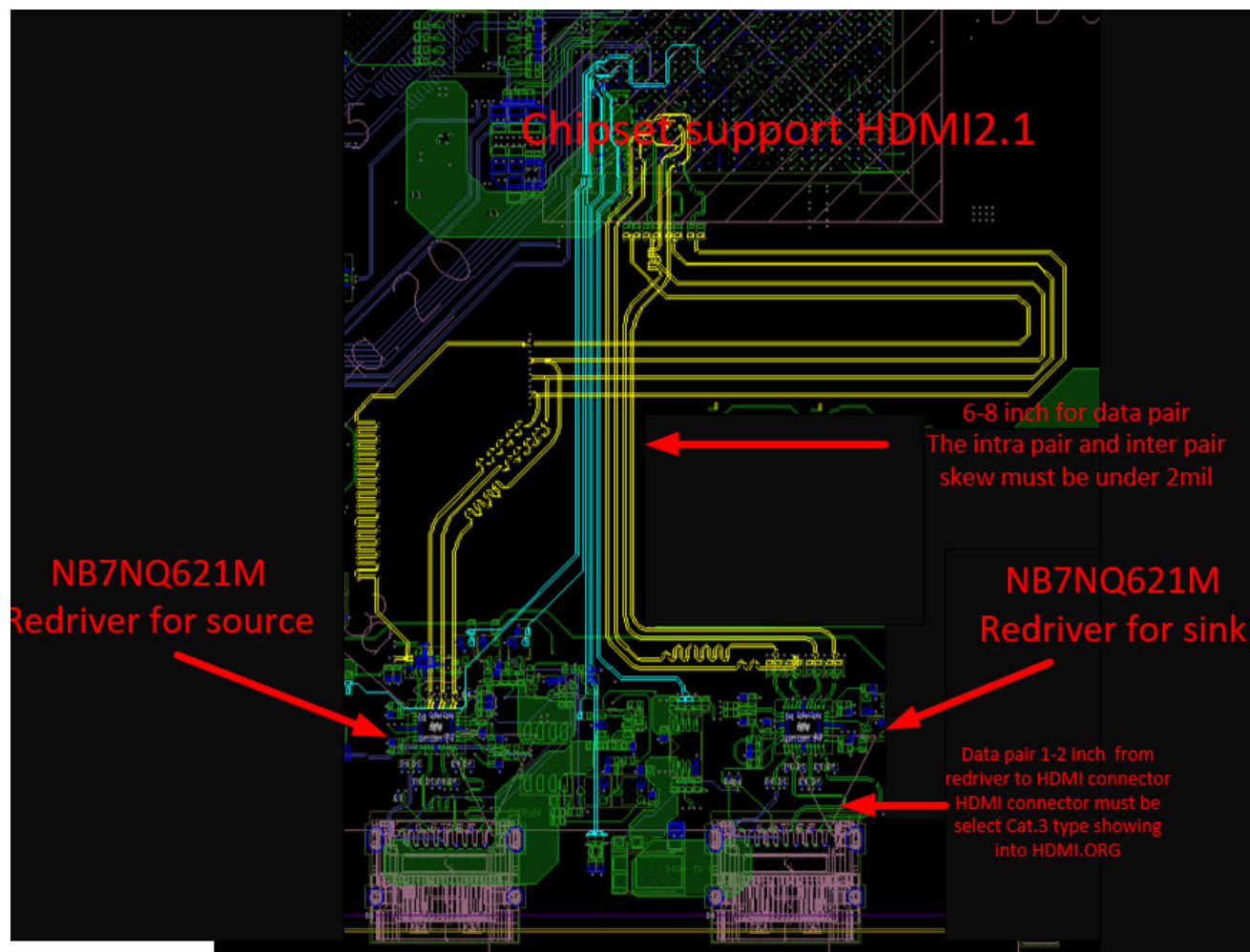
Figure 5. Example of Layout Routing

Given below are the brief Summary of the Compliance results from one of the Systems using NB7NQ621M tested at a certified Lab. Table 8 shows Source Side Test results and Table 9 Shows the Sink Side Test Results.

Table 8. SOURCE SIDE TEST RESULT SUMMARY

Test Item		Result
HDMI 2.1 FRL Electrical	Test ID HFR 1−1: DC Common Mode	Pass
	Test ID HFR 1−2: Vse_max, Vse_min	Pass
	Test ID HFR 1−3: TRISE, TFALL	Pass
	Test ID HFR 1−4: Inter−Pair Skew	Pass
	Test ID HFR 1−5: TMDS / FRL Rates	Pass
	Test ID HFR 1−6: Data Jitter (Rj)	Pass
	Test ID HFR 1−7: Data Eye Diagram	Pass
	Test ID HFR 1−8: AC Common Mode Noise	Pass
	Test ID HFR 1−9: FFE	Pass
HDMI 2.1 TMDS Electrical	Test ID HF 1−1: VL and Vswing	Pass
	Test ID HF 1−2: TRISE, TFALL	Pass
	Test ID HF 1−3: Inter−Pair Skew	Pass
	Test ID HF 1−4: Intra−Pair Skew	Pass
	Test ID HF 1−5: Differential Voltage	Pass
	Test ID HF 1−6: Clock Duty Cycle and Clock Rate	Pass
	Test ID HF 1−7: Clock Jitter	Pass
	Test ID HF 1−8: Data Eye Diagram	Pass
	Test ID HF 1−9: Differential impedance test	Pass
HDMI 1.4 TMDS Electrical	7−2 Low Level Output Voltage (VL)	Pass
	7−4 Rise/Fall Time	Pass
	7−5 Overshoot/Undershoot	Pass
	7−6 Inter−pair Skew	Pass
	7−7 Intra−pair Skew	Pass
	7−8 Clock Duty Cycle	Pass
	7−9 Clock Jitter	Pass
	7−10 Data Eye Diagram	Pass

Given below are some suggestion and notes that will help to pass Compliance:
1. Set the redriver slew rate setting to slew1 or slew2 for passing HDMI 1.4 7−4 Rise/Fall Time test.
2. Set the redriver output swing = 1000 mV for pass HDMI 1.4 7−2 low level output voltage (VL) test.
3. Set the redriver line to line impedance to 100 Ohm for pass the HDMI 2.1 HF 1−9 differential impedance test.
4. Set the redriver EQ level under level 3 for passing HDMI 2.1 FRL HFR1−7 eye diagram test.
5. Make sure the data pair of length pair to pair mismatch is under 2 mil and select the HDMI category 3 certification connector for passing the HDMI 2.1 FRL HFR 1−4 Inter−Pair Skew.

Table 9. SINK SIDE TEST RESULT SUMMARY

	Test Item	Result
HDMI 2.1 FRL Electrical	Test ID HFR 2−1: Max Differential Swing Tolerance	Pass
	Test ID HFR 2−2: Intra−Pair Skew	Pass
	Test ID HFR 2−3: Inter−Pair Skew	Pass
	Test ID HFR 2−4: Minimum Link Rate Tolerance	Pass
	Test ID HFR 2−5: Jitter Tolerance	Pass
HDMI 2.1 TMDS Electrical	Test ID HF 2−1: Min/Max Differential Swing Tolerance	Pass
	Test ID HF 2−2: Intra−Pair Skew	Pass
	Test ID HF 2−3: Jitter Tolerance	Pass
HDMI 1.4 TMDS Electrical	8−4 Termination Voltage	Pass
	8−5 Min/Max Differential Swing Tolerance	Pass
	8−6 Intra−pair Skew	Pass
	8−7 Jitter Tolerance	Pass
	8−8 Differential Impedance	Pass
	8−21 Audio Clock Regeneration	Pass
	8−22 Audio Sample Packet Jitter	Pass
	8−23 Audio Formats	Pass
	8−24 DVI Interoperability	Pass
	8−25 Deep Color	Pass
	8−28 One Bit Audio	Pass
	8−29 3D Video	Pass
	8−30 4K x 2K Video	Pass
	8−31 Extended Colors and Contents	Pass

Given below are some suggestion and notes that will help to pass Compliance:
1. Make sure the data pair of length pair to pair mismatch is under 2mil and select the HDMI category 3 certification connector for pass the HDMI 2.1 and FRL HFR 2−2: Intra−Pair Skew and HFR 2−3: Inter−Pair Skew.
2. Set the redriver of EQ level under level 3 and Flat gain under 1.5 db to pass the HDMI 2.1 FRL HFR 2−5: Jitter Tolerance test.
3. Set the FRL DC Coupling mode, Mode 4 for pass the HDMI 1.4 8−8 Differential Impedance.

Given below Eye−Diagram for HDMI1.4 7−10 TP2 EQ worse cable model eye diagram on one of the Lanes:
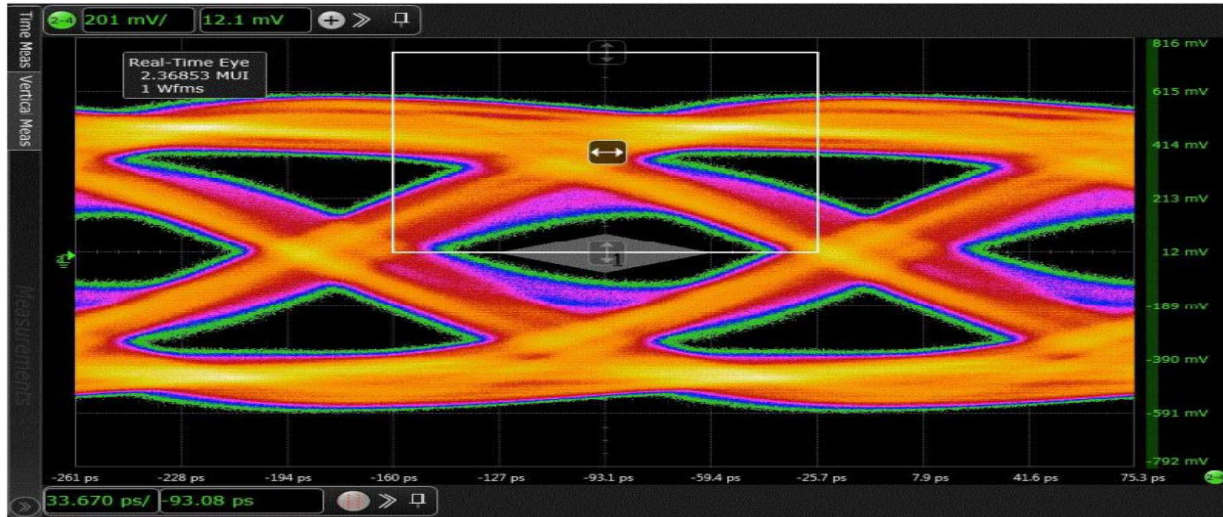
Figure 6. Eye−Diagram for HDMI 1.4 HF 7 − 10

Given below Eye−Diagram for HDMI 2.1 TMDS HF 1−8 TP2 EQ worse cable model eye diagram on one of the Lanes:
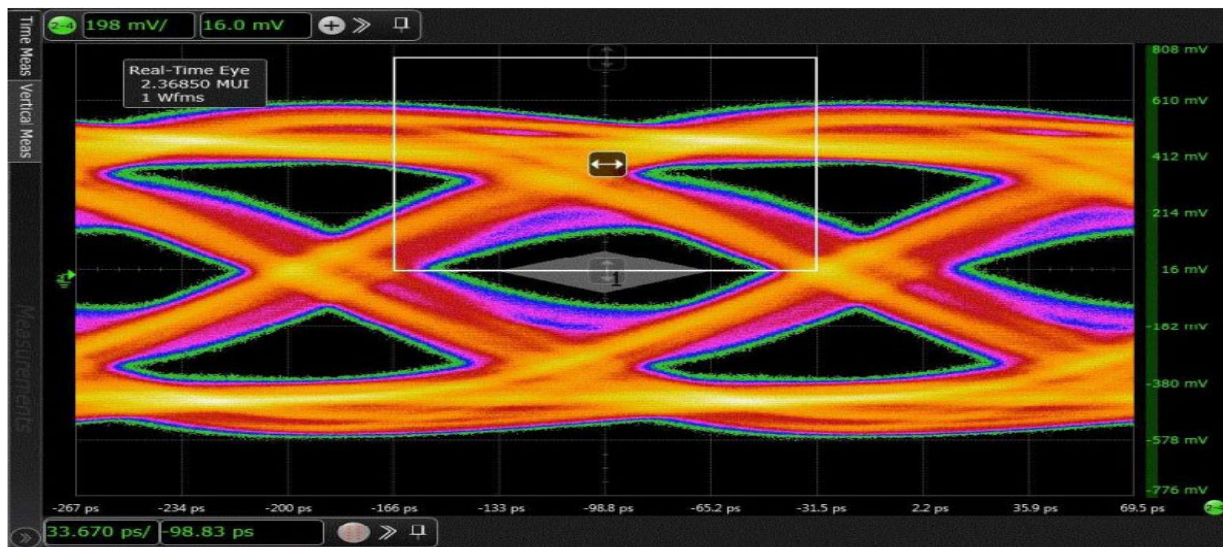
Figure 7. Eye−Diagram for HDMI 2.1 TMDS HF 1 − 8

Given below Eye−Diagram for HDMI 2.1 FRL HFR 1−8 eye diagram TP3 EQ worse cable model 12 Gbps on one of the Lanes:
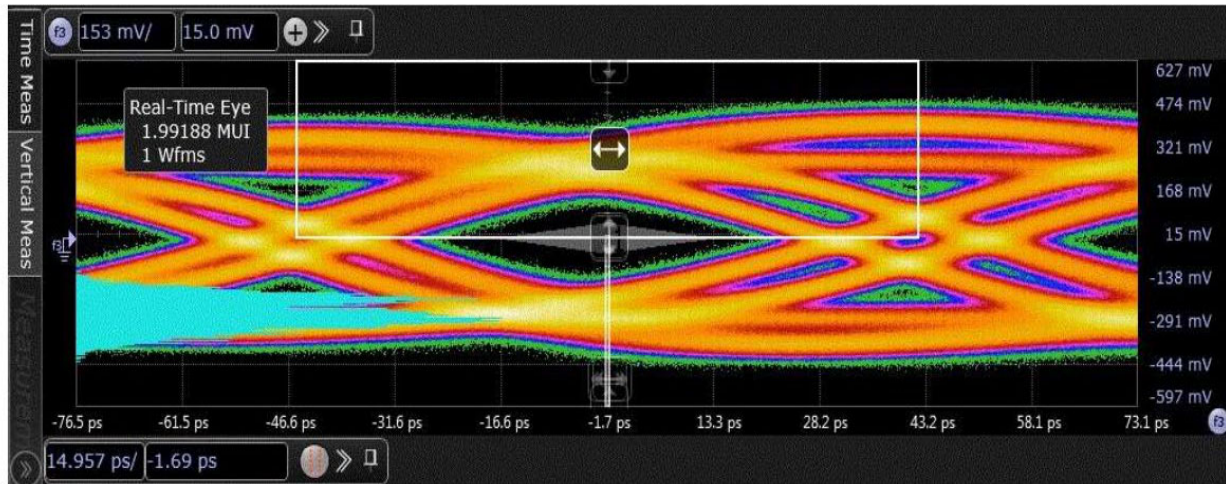
Figure 8. Eye−Diagram for HDMI 2.1 TMDS HF 1 − 8 12 Gbps

Conclusion

We can conclude that with NB7NQ621M device, it is possible to meet compliance requirement of HDMI 2.1 TMDS and FRL Mode for both the Source and Sink Side applications using the multiple I^2C setting options available.

The above application note provides the details of the required redriver settings and suggestion to meet Compliance.

onsemi is licensed by the Philips Corporation to carry the I^2C bus protocol.

PUBLICATION ORDERING INFORMATION

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