Data Sheet | November 10, 2006 | FN9283.1

Wide VIN, 7V to 25V, Single-Phase PWM Controller with Integrated MOSFET Drivers

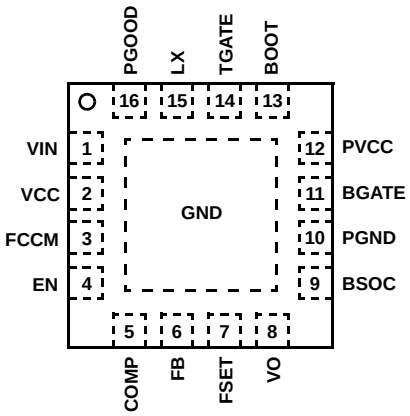
The ISL8106 is a Single-Phase Synchronous-Buck PWM Controller with a input voltage range of +7.0V to +25.0V featuring Intersil's Robust Ripple Regulator (R^3) technology that delivers exceptional dynamic response to input voltage and output load transients. Integrated MOSFET drivers, 5V LDO, and bootstrap diode result in fewer components and smaller implementation area for power supply systems.

The ISL8106 features a 1.5ms digital soft-start and can be started into a pre-biased output voltage. A resistor divider is used to program the output voltage setpoint. The ISL8106 can be configured to operate in forced-continuous-conduction-mode (FCCM) or in diode-emulation-mode (DEM), which improves light-load efficiency. In FCCM the controller always operates as a synchronous rectifier, switching the bottom-side MOSFET regardless of the output load. With DEM enabled, the bottom-side MOSFET is disabled preventing negative current flow from the output inductor during low load operation. This makes the ISL8106 an excellent choice for all “green” applications. An audio filter prevents the PWM switching frequency from entering the audible spectrum due to extremely light load while in DEM.

A PGOOD pin featuring a unique fault-identification capability significantly reduces system trouble-shooting time and effort. The pull-down resistance of the PGOOD pin is 30Ω for an overcurrent fault, 60Ω for an overvoltage fault, or 90Ω for either an undervoltage fault or during soft-start. Overcurrent protection is accomplished by measuring the voltage drop across the $r_{DS(ON)}$ of the bottom-side MOSFET. A single resistor programs the overcurrent and short-circuit points. Overvoltage and undervoltage protection is monitored at the FB voltage feedback pin.

Pinout

16 LD QFN (4mm x 4mm)
TOP VIEW



Features

- Wide input voltage range: +7.0V to +25.0V
- High performance R^3 technology delivers extremely fast transient response
- +0.6V Internal Reference
  - ±0.6% tolerance over the commercial temperature Range (0°C to +70°C)
  - ±1.0% tolerance over the industrial temperature range (-40°C to +85°C)
- Output voltage range: +0.6V to V_{CC}-0.3V
- Selectable forced continuous conduction mode or diode emulation mode
- Integrated MOSFET drivers with shoot-through protection
- External type-two loop compensation
- Internal 5V low-dropout regulator with Integrated boot-strap diode
- Programmable PWM frequency: 200kHz to 600kHz
- PWM minimum frequency above audible spectrum
- Internal digital soft-start with prebiased startup capability
- Power good monitor with fault identification by PGOOD pull down resistance
- Lossless, programmable overcurrent protection
  - Uses bottom-side MOSFET's $r_{DS(ON)}$
- Undervoltage protection, soft crowbar overvoltage protection and over-temperature protection
- Pb-free plus anneal available (RoHS compliant)

Applications

- Telecom/datacom applications
- Industrial applications
- Distributed DC/DC power architecture
- Point-of-load modules

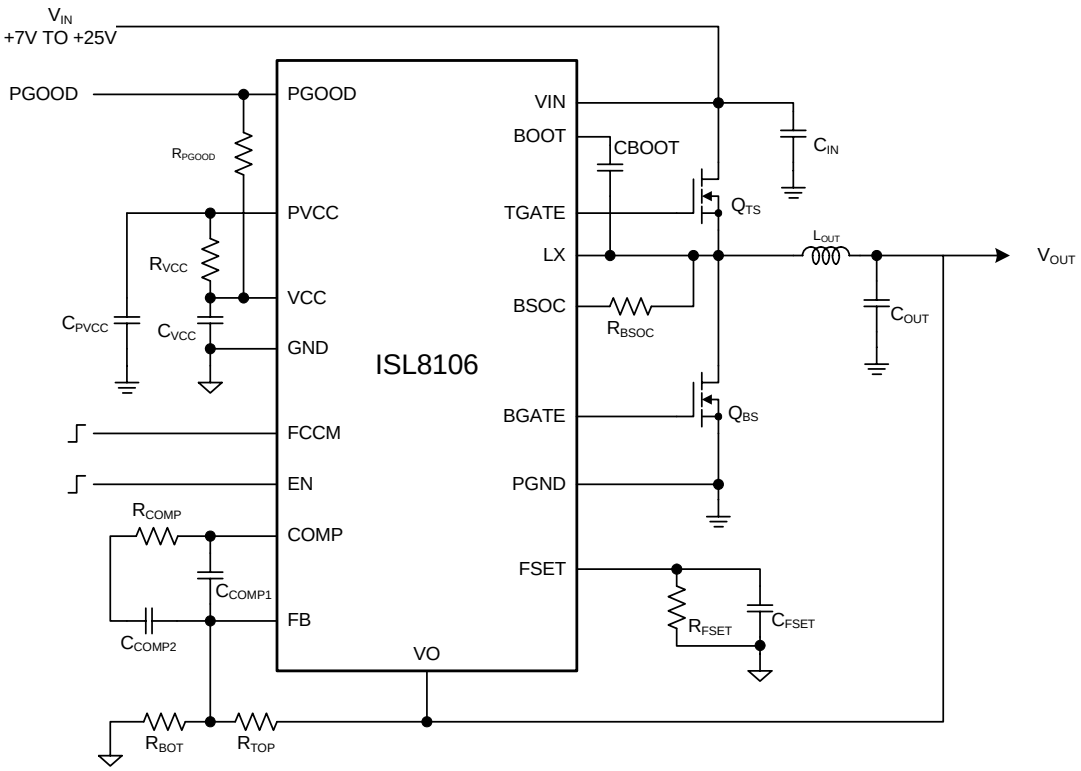
Ordering Information

PART NUMBER	PART MARKING	TEMP (°C)	PACKAGE	PKG. DWG. #
ISL8106CRZ*	8106CRZ	0 to +70	16 Ld 4x4 QFN	L16.4x4
ISL8106IRZ*	8106IRZ	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL8106EVAL1Z	Evaluation Board			

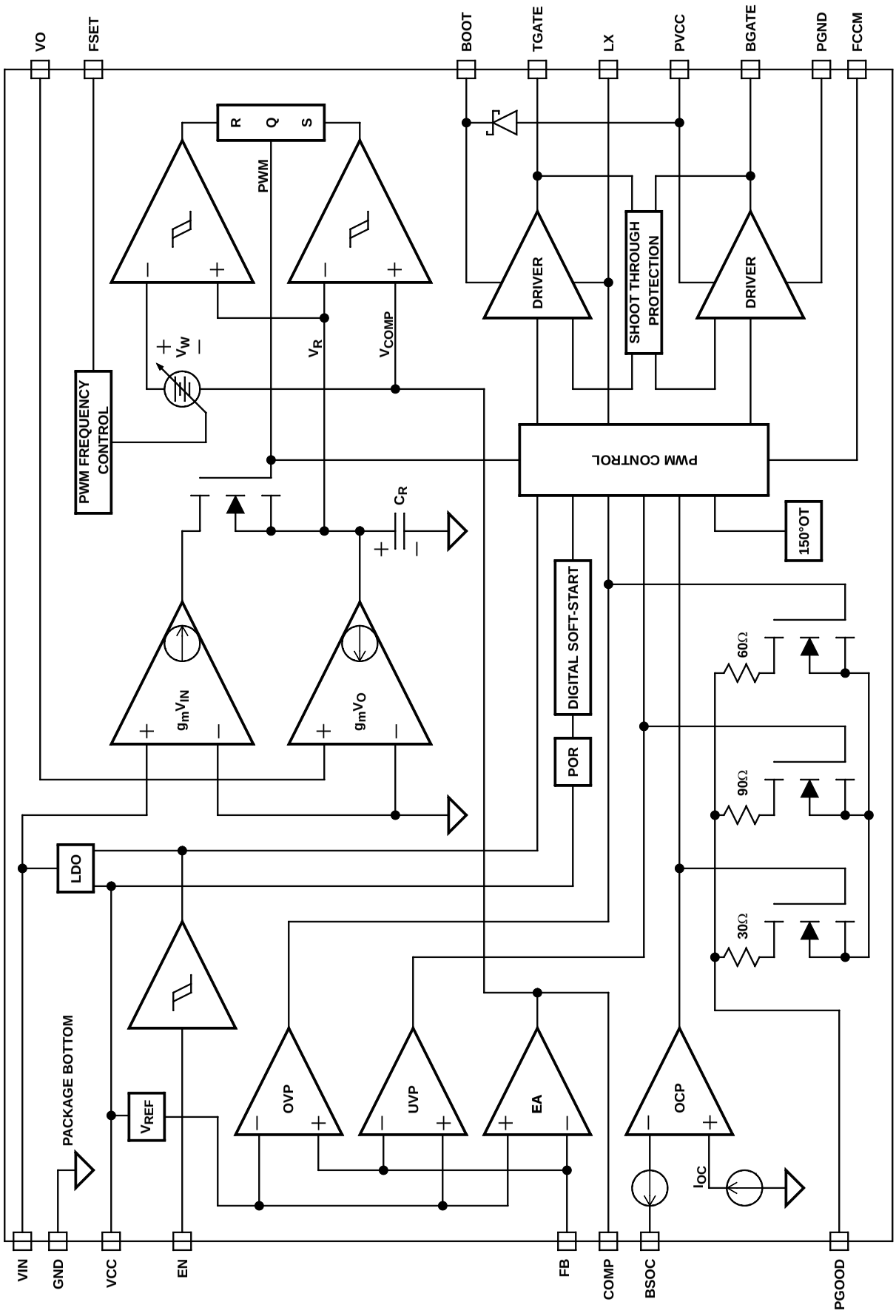
*Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application



Block Diagram



Absolute Voltage Ratings

BSOC, VIN to GND . . . . . -0.3V to +28V
VCC, PGOOD to GND . . . . . -0.3V to +7.0V
PVCC to PGND. . . . . -0.3V to +7.0V
GND to PGND. . . . . -0.3V to +0.3V
EN, FCCM. . . . . -0.3V to GND, VCC +3.3V
LX to GND. . . . . (DC) -0.3V to +28V
. . . . . (<100ns Pulse Width, 10µJ) -5.0V
BOOT to GND, or PGND . . . . . -0.3V to +33V
BOOT to LX . . . . . -0.3V to +7V
TGATE . . . . . (DC) -0.3V to LX, BOOT +0.3V
. . . . . (<200ns Pulse Width, 20µJ) -4.0V
BGATE . . . . . (DC) -0.3V to PGND, PVCC +0.3V
. . . . . (<100ns Pulse Width, 4µJ) -2.0V
ESD Classification . . . . . Level 1 (HBM = 2kV)

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	48	11.5

Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range
ISL8106CRZ. . . . . 0°C to +70°C
ISL8106IRZ . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature . . . . . (soldering, 10s) +300°C

Recommended Operating Conditions

Ambient Temperature Range (ISL8106C) . . . . . 0°C to +70°C
Ambient Temperature Range (ISL8106I) . . . . . -40°C to +85°C
Supply Voltage (VIN to GND) . . . . . 7V to 25V

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. Parameters are Guaranteed by Design.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted specifications in **bold** are valid for process, temperature, and line operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN						
VIN Voltage Range	V_{IN}		7.0		25.0	V
VIN Input Bias Current	I_{VIN}	EN and FCCM = 5V, FB = 0.65V, VIN = 7V to 25V		2.2	3.0	mA
VIN Shutdown Current	I_{SHDN}	EN = GND, VIN = 25V		0.1	1.0	µA
VCC LDO						
VCC Output Voltage Range	V_{CC}	VIN = 7V to 25V, I_{LDO} = 0mA to 80mA	4.75	5.00	5.25	V
VCC POR THRESHOLD						
Rising VCC POR Threshold Voltage	V_{CCTHR}	ISL8106CRZ	4.35	4.45	4.55	V
		ISL8106IRZ	4.33	4.45	4.55	V
Falling VCC POR Threshold Voltage	V_{CCTHF}	ISL8106CRZ	4.10	4.20	4.30	V
		ISL8106IRZ	4.08	4.20	4.30	V
CONTROL INPUTS						
EN High Threshold Voltage	V_{ENTHR}		2.0			V
EN Low Threshold Voltage	V_{ENTHF}				0.5	V
FCCM High Threshold Voltage	$V_{FCCMTHR}$		2.0			V
FCCM Low Threshold Voltage	$V_{FCCMTHF}$				1.0	V
EN Leakage Current	I_{ENL}	EN = 0V		<0.1	1.0	µA
	I_{ENH}	EN = 5.0V		20		µA
FCCM Leakage Current	I_{FCCML}	FCCM = 0V		<0.1	1.0	µA
	I_{FCCMH}	FCCM = 5.0V		2.0		µA
REFERENCE						
Reference Voltage	V_{REF}			0.6		V
Voltage Regulation Accuracy	V_{REG}	ISL8106CRZ	-0.6		+0.6	%
		ISL8106IRZ	-1.0		+1.0	%

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted specifications in **bold** are valid for process, temperature, and line operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM						
Frequency Range	F_{OSC}	FCCM = 5V	200		600	kHz
	F_{AUDIO}	FCCM = GND; ISL8106CRZ	21	28		kHz
		FCCM = GND; ISL8106IRZ	20	28		kHz
Frequency-Set Accuracy		F_{OSC} = 300kHz; ISL8106CRZ	-10		+10	%
		F_{OSC} = 300kHz; ISL8106IRZ	-12		+12	%
VO Range	V_{VO}		0.60		3.30	V
VO Input Leakage Current	I_{VO}	VO = 0.60V VO = 3.30V		1.3 7.0		µA µA
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}	FB = 0.60V		± 20		nA
COMP Source Current	$I_{COMPSRC}$	FB = 0.40V, COMP = 3.20V		2.5		mA
COMP Sink Current	$I_{COMPSNK}$	FB = 0.80V, COMP = 0.30V		0.3		mA
COMP High Clamp Voltage	V_{COMPHC}	FB = 0.40V, Sink 50µA	3.10	3.40	3.65	V
COMP Low Clamp Voltage	V_{COMPLC}	FB = 0.80V, Source 50µA	0.09	0.15	0.21	V
GATE DRIVER						
TGATE Pull-Up Resistance	$R_{TGATEPU}$	200mA Source Current (Note 3)		1.0	1.5	Ω
TGATE Source Current	$I_{TGATESRC}$	V_{TGATE} to LX = 2.5V		2.0		A
TGATE Sink Resistance	$R_{TGATEPD}$	250mA Sink Current (Note 3)		1.0	1.5	Ω
TGATE Sink Current	$I_{TGATESNK}$	V_{TGATE} to LX = 2.5V		2.0		A
BGATE Pull-Up Resistance	$R_{BGATEPU}$	250mA Source Current (Note 3)		1.0	1.5	Ω
BGATE Source Current	$I_{BGATESRC}$	V_{BGATE} to PGND = 2.5V		2.0		A
BGATE Sink Resistance	$R_{BGATEPD}$	250mA Sink Current (Note 3)		0.5	0.9	Ω
BGATE Sink Current	$I_{BGATESNK}$	V_{BGATE} to PGND = 2.5V		4.0		A
Delay From TGATE Falling to BGATE Rising	$t_{TGATEFBGATER}$	TGATE falling to BGATE rising		21		ns
Delay From BGATE Falling to TGATE Rising	$t_{BGATEFTGATER}$	BGATE falling to TGATE rising		14		ns
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 2mA		0.58		V
Reverse Leakage	I_R	V_R = 25V		0.2		µA
POWER GOOD						
PGOOD Pull Down Impedance	PGR_{SS}	PGOOD = 5mA Sink; ISL8106CRZ	75	95	115	Ω
	PGR_{UV}					
	PGR_{SS}	PGOOD = 5mA Sink; ISL8106IRZ	67	95	118	Ω
	PGR_{UV}					
	PGR_{OV}	PGOOD = 5mA Sink; ISL8106CRZ	50	63	78	Ω
		PGOOD = 5mA Sink; ISL8106IRZ	45	63	81	Ω
	PGR_{OC}	PGOOD = 5mA Sink; ISL8016CRZ	25	32	40	Ω
		PGOOD = 5mA Sink; ISL8106IRZ	22	32	43	Ω
PGOOD Leakage Current	I_{PGOOD}	PGOOD = 5V		<0.1	1.0	µA
PGOOD Maximum Sink Current				5.0		mA

Electrical Specifications Recommended Operating Conditions, unless otherwise noted specifications in **bold** are valid for process, temperature, and line operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD Soft-Start Delay	T_{SS}	EN High to PGOOD High; ISL8106CRZ	2.20	2.75	3.30	ms
		EN High to PGOOD High; ISL8106IRZ	2.20	2.75	3.50	ms
PROTECTION						
BSOC OCP Threshold Current	I_{OC}	ISL8106CRZ	-33	-26	-19	µA
		ISL8106IRZ	-33	-26	-17	µA
BSOC Short-Circuit Threshold Current	I_{SC}			-50		µA
UVP Threshold Voltage	V_{UV}		81	84	87	%
OVP Rising Threshold Voltage	V_{OVR}		113	116	119	%
OVP Falling Threshold Voltage	V_{OVF}			103		%
OTP Rising Threshold Temperature	T_{OTR}	(Note 3)		150		°C
OTP Temperature Hysteresis	T_{OTHYS}	(Note 3)		25		°C

Functional Pin Descriptions

GND (Bottom terminal pad)

Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin, not the PGND pin. Connect the GND pad of the ISL8106 to the signal ground layer of the pcb using at least five vias, for a robust thermal and electrical conduction path.

The best tie-point between the signal ground and the power ground is at the negative side of the output capacitors that is not in the return path of the inductor ripple current flowing through the output capacitors.

VIN (Pin 1)

The VIN pin measures the converter input voltage with respect to the GND pin. VIN is a required input to the R^3 PWM modulator. The VIN pin is also the input source for the integrated +5V LDO regulator.

VCC (Pin 2)

The VCC pin is the output of the integrated +5V LDO regulator, which provides the bias voltage for the IC. The VCC pin delivers regulated +5V whenever the EN pin is pulled above V_{ENTHR}. For best performance, the LDO requires at least a 1µF MLCC decouple capacitor to the GND pin.

FCCM (Pin 3)

The FCCM pin configures the controller to operate in forced-continuous-conduction-mode (FCCM) or diode-emulation-mode (DEM). DEM is disabled when the FCCM pin is pulled above the rising threshold voltage $V_{FCCMTHR}$, and DEM is enabled when the FCCM pin is pulled below the falling threshold voltage $V_{FCCMTHF}$.

EN (Pin 4)

The EN pin is the on/off switch of the IC. When the EN pin is pulled above the rising threshold voltage V_{ENTHR}, V_{CC} will ramp up and begin regulation. The soft-start sequence begins once V_{CC} ramps above the power-on reset (POR) rising threshold voltage V_{CCTHR}. When the EN pin is pulled below the falling threshold voltage V_{ENTHF}, PWM immediately stops and V_{CC} decays below the POR falling threshold voltage V_{CCTHF}, at which time the IC turns off.

COMP (Pin 5)

The COMP pin is the output of the control-loop error amplifier. Loop compensation components connect from the COMP pin to the FB pin.

FB (Pin 6)

The FB pin is the inverting input of the control loop error amplifier. The converter will regulate to 600mV at the FB pin with respect to the GND pin. Scale the desired output voltage to 600mV with a voltage divider network made from resistors R_{TOP} and R_{BOTTOM}. Loop compensation components connect from the FB pin to the COMP pin.

FSET (Pin 7)

The FSET pin programs the PWM switching frequency of the converter. Connect a resistor R_{FSET} and a 10nF capacitor C_{FSET} from the FSET pin to the GND pin.

VO (Pin 8)

The VO pin makes a direct measurement of the converter output voltage used exclusively by the R^3 PWM modulator. The VO pin should be connected to the top of feedback resistor R_{TOP} at the converter output. Refer to Typical Application Schematic.

BSOC (Pin 9)

The BSOC pin is the input to the overcurrent protection (OCP) and short-circuit protection (SCP) circuits. Connect a resistor R_{BSOC} between the BSOC pin and the LX pin. Select the value of R_{BSOC} that will force the BSOC pin to source the I_{BSOC} threshold current I_{OC} when the peak inductor current reaches the desired OCP setpoint. The SCP threshold current I_{SC} is fixed at twice the OCP threshold current I_{OC}.

PGND (Pin 10)

The PGND pin should be connected to the source of the bottom-side MOSFET, preferably with an isolated path that is in parallel with the trace connecting the BGATE pin to the gate of the MOSFET. The PGND pin is an isolated path used exclusively to conduct the turn-off transient current that flows out the PGND pin, through the gate-source capacitance of the bottom-side MOSFET, into the BGATE pin, and back to the PGND pin through the pull-down resistance of the BGATE driver. The adaptive shoot-through protection circuit, measures the bottom-side MOSFET gate voltage with respect to the PGND pin, not the GND pin.

BGATE (Pin 11)

The BGATE pin is the output of the bottom-side MOSFET gate driver. Connect to the gate of the bottom-side MOSFET.

The signal going through this trace is both high dv/dt and high di/dt, with high peak charging and discharging current. Route this trace in parallel with the trace from the PGND pin. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in parallel with these traces on any layer.

PVCC (Pin 12)

The PVCC pin is the input voltage for the bottom-side MOSFET gate driver BGATE. Connect a +5V power source to the PVCC pin with respect to the GND pin, a 1µF MLCC bypass capacitor needs to be connected from the PVCC pin to the PGND pin, not the GND pin. The VCC output may be used for the PVCC input voltage source. Connect the VCC pin to the PVCC pin through a low-pass filter consisting of a resistor and the PVCC bypass capacitor. Refer to Typical Application Schematic.

BOOT (Pin 13)

The BOOT pin stores the input voltage for the top-side MOSFET gate driver. Connect an MLCC capacitor across the BOOT and LX pins. The boot capacitor is charged through an internal boot diode connected from the PVCC pin to the BOOT pin, each time the LX pin drops below PVCC minus the voltage dropped across the internal boot diode.

TGATE (Pin 14)

The TGATE pin is the output of the top-side MOSFET gate driver. Connect to the gate of the top-side MOSFET.

The signal going through this trace is both high dv/dt and high di/dt, with high peak charging and discharging current. Route this trace in parallel with the trace from the LX pin. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in parallel with these traces on any layer.

LX (Pin 15)

The LX pin is the return current path for the TGATE MOSFET driver. The LX pin also measures the polarity of the bottom-side MOSFET drain voltage for the diode emulation function.

Connect the LX pin to the node consisting of the top-side MOSFET source, the bottom-side MOSFET drain, and the output inductor. Refer to Typical Application Schematic. This trace should be short, and positioned away from other weak signal traces. The parasitic capacitance and parasitic inductance of the LX node should be kept very low to minimize ringing. If ringing is excessive, it could easily affect current sample information. It would be best to limit the size of the LX node copper in strict accordance with the current and thermal management of the application.

PGOOD (Pin 16)

The PGOOD pin is an open-drain output that is high impedance when the converter is in regulation, or when the EN pin is pulled below the falling threshold voltage V_{ENTHF}. The PGOOD pin has three distinct pull-down impedances that correspond to an OVP fault, OCP/SCP, or UVP and soft-start. Connect the PGOOD pin to +5V through a pull-up resistor.

Functional Description

POR and Soft-Start

The power-on reset (POR) circuit monitors V_{CC} for the V_{CCR} (rising) and V_{CCF} (falling) voltage thresholds. The purpose of soft-start is to limit the inrush current through the output capacitors when the converter first turns on. The PWM soft-start sequence initializes once V_{CC} rises above the V_{CCR} threshold, beginning from below the V_{CCF} threshold.

The ISL8106 uses a digital soft-start circuit to ramp the output voltage of the converter to the programmed regulation setpoint in approximately 1.5ms. The converter regulates to 600mV at the FB pin with respect to the GND pin. During soft-start a digitally derived voltage reference forces the converter to regulate from 0V to 600mV at the FB pin. When the EN pin is pulled above the rising EN threshold voltage V_{ENTHR} the PGOOD Soft-Start Delay T_{SS} begins and the output voltage begins to rise. The output voltage enters regulation in approximately 1.5ms and the PGOOD pin goes to high impedance once T_{SS} has elapsed.

When the EN pin is pulled below the V_{ENF} threshold, the LDO stops regulating and PWM immediately stops, regardless of the falling V_{CC} voltage. The soft-start sequence can be reinitialized and fault latches reset, once V_{CC} falls below the V_{CCF} threshold.

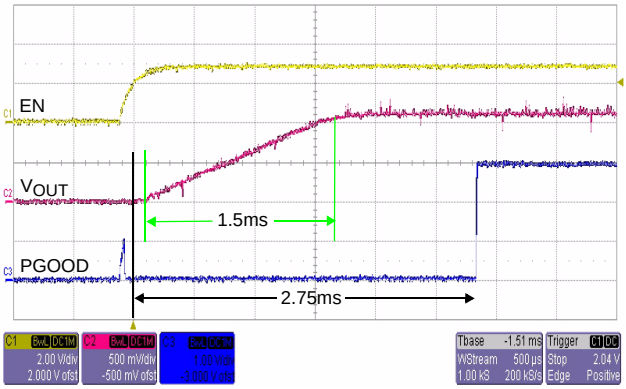


FIGURE 1. SOFT-START SEQUENCE

PGOOD

The PGOOD pin connects to three open drain MOSFETS each of which has a different $r_{DS(ON)}$. The PGOOD pin is an undefined impedance if V_{CC} has not reached the rising POR threshold V_{CCR}, or if V_{CC} is below the falling POR threshold V_{CCF}. The ISL8106 features a unique fault-identification capability that can drastically reduce trouble-shooting time and effort. The pull-down resistance of the PGOOD pin

corresponds to the fault status of the controller. During soft-start or if an undervoltage fault occurs, the PGOOD pulldown resistance is 95Ω, or 30Ω for an overcurrent fault, or 60Ω for an overvoltage fault.

TABLE 1. PGOOD PULL-DOWN RESISTANCE

CONDITION	PGOOD RESISTANCE
IC Off	Open
Soft-Start	95Ω
Undervoltage Fault	95Ω
Overvoltage Fault	60Ω
Overcurrent Fault	30Ω

LDO

Voltage applied to the VIN pin with respect to the GND pin is regulated to +5VDC by an internal low-dropout voltage regulator (LDO). The output of the LDO is called V_{CC}, which is the bias voltage used by the IC internal circuitry. The LDO output is routed to the VCC pin and requires a ceramic capacitor connected to the GND pin to stabilize the LDO and to decouple load transients.

When the EN pin rises above the V_{ENR} threshold, V_{CC} will turn on and rise to its regulation voltage. The LDO regulates V_{CC} by pulling up towards the voltage at the VIN pin; the LDO has no pull-down capability.

Pulse Width Modulator

The ISL8106 is a hybrid of fixed frequency PWM control, and variable frequency hysteretic control. Intersil's R^3 technology can simultaneously affect the PWM switching frequency and PWM duty cycle in response to input voltage and output load transients. The term "Ripple" in the name "Robust-Ripple-Regulator" refers to the converter output inductor ripple current, not the converter output ripple voltage. The output voltage is regulated to 600mV at the FB pin with respect to the GND pin. The FB pin is the inverting input of the error amplifier. The frequency response of the feedback control loop is tuned with a type-two compensation network connected across the FB pin and COMP pin.

The R^3 modulator synthesizes an AC signal V_R, which is an ideal representation of the output inductor ripple current. The duty-cycle of V_R is derived from the voltage measured at the VIN pin and VO pin with respect to the GND pin. Transconductance amplifiers convert the VIN and VO voltages into currents that charge and discharge the ripple capacitor C_R. The positive slope of V_R can be written as:

$$V_{RPOS} = (gm)\cdot(V_{IN} - V_O) \quad \text{(EQ. 1)}$$

The negative slope of V_R can be written as:

$$V_{RNEG} = gm\cdot V_O \quad \text{(EQ. 2)}$$

A voltage V_W is referenced with respect to the error amplifier output voltage V_{COMP}, creating a window-voltage envelope into which voltage V_R is compared. The V_R, V_{COMP}, and V_W signals feed into a hysteretic window comparator in which V_{COMP} is the lower threshold voltage and V_W is the higher threshold voltage. PWM pulses are generated as V_R traverses the V_W and V_{COMP} thresholds. The charging and discharging rates of capacitor C_R determine the PWM switching frequency for a given amplitude of V_W with respect to V_{COMP}. The R^3 regulator simultaneously affects switching frequency and duty cycle because it modulates both edges of the PWM pulses.

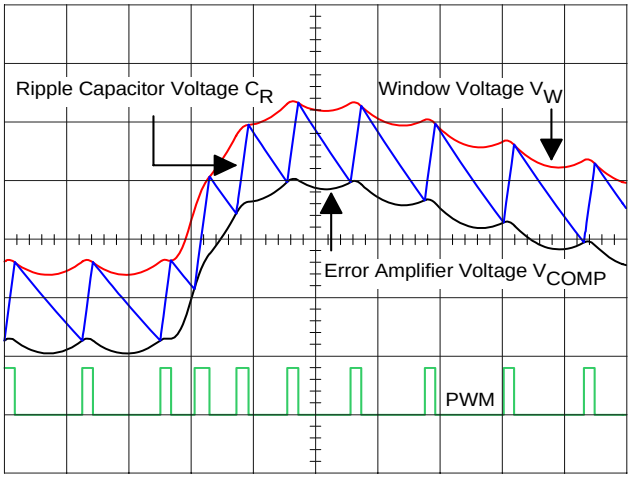


FIGURE 2. MODULATOR WAVEFORMS DURING LOAD TRANSIENT

MOSFET Gate-Drivers

The ISL8106 has internal gate-drivers for the top-side and bottom-side N-Channel MOSFETs. The bottom-side gate-driver is optimized for low duty-cycle applications where the bottom-side MOSFET conduction losses are dominant, requiring a low $r_{DS(on)}$ MOSFET. The BGATE pulldown resistance is small in order to clamp the gate of the MOSFET below the $V_{GS(th)}$ at turnoff. The current transient through the gate at turnoff can be considerable because the switching charge of a low $r_{DS(on)}$ MOSFET can be large. Both drivers incorporate bottom-side MOSFETS from conducting simultaneously and shorting the input supply. During turn-off of the bottom-side MOSFET, the BGATE to PGND voltage is monitored until it reaches a 1V threshold, at which time the TGATE driver is allowed to switch. During turn-off of the top-side MOSFET, the TGATE to LX voltage is monitored until it reaches a 1V threshold, at which time the BGATE driver is allowed to switch.

The input power for the BGATE driver circuit is sourced directly from the PVCC pin. The input power for the TGATE driver circuit is sourced from a “boot” capacitor connected from the BOOT pin to the LX pin. The boot capacitor is charged from a 5V bias supply through a internal Schottky diode each time the bottom-side MOSFET turns on.

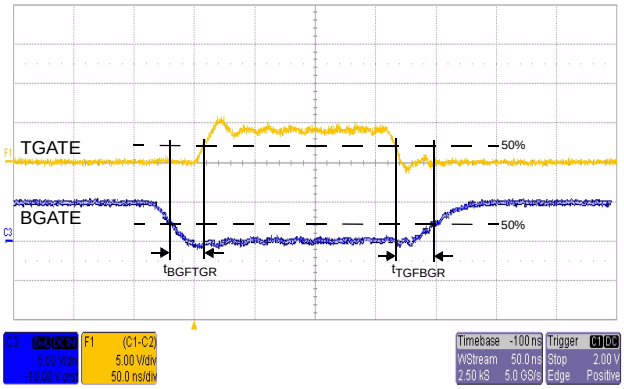


FIGURE 3. GATE DRIVE TIMING DIAGRAM

Diode Emulation

Positive inductor current can flow *from* the source of the top-side MOSFET or *from* the drain of the bottom-side MOSFET. Negative inductor current flows *into* the drain of the bottom-side MOSFET. When the bottom-side MOSFET conducts positive inductor current, the LX voltage will be negative with respect to the GND pin. Conversely, when the bottom-side MOSFET conducts negative inductor current, the LX voltage will be positive with respect to the GND pin. Negative inductor current occurs when the output load current is less than ½ the inductor ripple current.

The ISL8106 can be configured to operate in forced-continuous-conduction-mode (FCCM) or in diode-emulation-mode (DEM), which can improve light-load efficiency. In FCCM, the controller always operates as a synchronous rectifier, switching the bottom-side MOSFET regardless of the polarity of the output inductor current. In DEM, the bottom-side MOSFET is disabled during negative current flow from the output inductor. DEM is permitted when the FCCM pin is pulled low, and disabled when pulled high.

When DEM is permitted, the converter will automatically select FCCM or DEM according to load conditions. If positive LX pin voltage is measured for eight consecutive PWM pulses, then the converter will enter diode-emulation mode on the next PWM cycle. If a negative LX pin voltage is measured, the converter will exit DEM on the following PWM pulse. An audio filter is incorporated into the PWM generation circuitry that prevents the switching frequency from entering the audible spectrum at low load conditions.

Overcurrent and Short-Circuit Protection

When an OCP or SCP fault is detected, the ISL8106 overcurrent and short-circuit protection circuit will pull the PGOOD pin low and latch off the converter. The fault will remain latched until the EN pin is pulled below V_{ENF} or if the voltage at the VIN pin is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold. Selecting the appropriate value of resistor R_{BSOC} that is connected from the BSOC pin to the drain terminal of the bottom-side MOSFET to programs the OCP threshold.

The OCP circuit measures positive-flowing, peak-current through the output inductor, not the DC current flowing from the converter to the load. The bottom-side MOSFET drain current is assumed to be equal to the positive output inductor current when the top-side MOSFET is turn off. Current briefly conducts through the bottom-side MOSFET body diode until the BGATE driver goes high. The peak inductor current develops a voltage across the $r_{DS(ON)}$ of the bottom-side MOSFET just as if it were a discrete current-sense resistor. An OCP fault will occur when the BSOC pin has measured more than the OCP threshold current I_{OC}, on consecutive PWM pulses, for a period exceeding 20µs. It does not matter how many PWM pulses are measured during the 20µs period. If a measurement falls below I_{OC} before 20µs has elapsed, then the timer is reset to zero. An SCP fault will occur when the BSOC pin has measured more than the short-circuit threshold current I_{SC}, in less than 10µs, on consecutive PWM pulses. The relationship between I_D and I_{BSOC} can be written as:

$$I_{BSOC} \cdot R_{BSOC} = I_D \cdot r_{DS(ON)} \quad \text{(EQ. 3)}$$

The value of R_{BSOC} can then be written as:

$$R_{BSOC} = \frac{\left[I_{FL} + \frac{I_{PP}}{2}\right] \cdot OC_{SP} \cdot r_{DS(ON)}}{I_{OC}} \quad \text{(EQ. 4)}$$

Where:

- R_{BSOC} (Ω) is the resistor used to program the over-current setpoint
- I_{BSOC} is the current sense current that is sourced from the BSOC pin
- I_{OC} is the I_{BSOC} threshold current value sourced from the BSOC pin that will activate the OCP circuit
- I_{FL} is the maximum continuous DC load current
- I_{PP} is the inductor peak-to-peak ripple current
- OC_{SP} is the desired overcurrent setpoint expressed as a multiplier relative to I_{FL}

Overvoltage

When an OVP fault is detected, the ISL8106 overvoltage protection circuit will pull the PGOOD pin low and latch off the converter. The fault will remain latched until the EN pin is pulled below V_{ENF} or if the voltage at the VIN pin is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold.

When the voltage at the FB pin (relative to the GND pin) has exceeded the rising overvoltage threshold V_{OVR}, the converter will latch off; however, the BGATE driver output will stay high, forcing the bottom-side MOSFET to pull down the output voltage of the converter. The bottom-side MOSFET will continue to pull down the output voltage until the voltage at the FB pin relative to the GND pin, has decayed below the falling overvoltage threshold $V_{OVF,}$ at which time the BGATE driver output is driven low, forcing the bottom-side MOSFET off. The BGATE driver output will continue to switch on at V_{OVR} and switch off at V_{OVF} until the EN pin is pulled below V_{ENF} or if the voltage at the VIN is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold.

UnderVoltage

When an UVP fault is detected, the ISL8106 undervoltage protection circuit will pull the PGOOD pin low and latch off the converter. The UVP fault occurs when the voltage at the FB pin relative to the GND pin, has fallen below the under-voltage threshold $V_{UV.}$ The fault will remain latched until the EN pin is pulled below V_{ENF} or if the voltage at the VIN is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold.

Over-Temperature

When an OTP fault is detected, the ISL8106 over-temperature protection circuit suspends PWM, but will not affect the PGOOD pin, or latch off the converter. The over-temperature protection circuit measures the temperature of the silicon and activates when the rising threshold temperature T_{OTR} has been exceeded. The PWM remains suspended until the silicon temperature falls below the temperature hysteresis T_{OTHYS} at which time normal operation is resumed. All other protection circuits will function normally during OTP however, since PWM is inhibited, it is likely that the converter will immediately experience an undervoltage fault, latch off, and pull PGOOD low. If the EN pin is pulled below V_{ENF} or if the voltage at the VIN is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold, normal operation will resume however, the temperature hysteresis T_{OTHYS} is reset.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

A multi-layer printed circuit board is recommended. Figure 4 shows the critical components of the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage

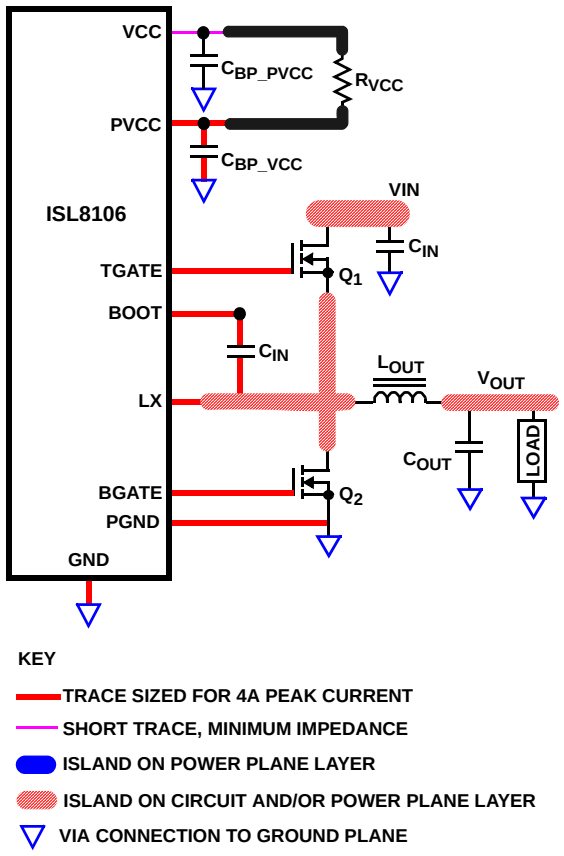


FIGURE 4. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

levels. Keep the metal runs from the LX terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the LX nodes. Use the remaining printed circuit layers for small signal wiring.

Locate the ISL8106 within 2 to 3 inches of the MOSFETs, Q1 and Q2 (1 inch or less for 500kHz or higher operation). The circuit traces for the MOSFETs' gate and source connections from the ISL8106 must be sized to handle up to 4A peak current. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT pin and the phase node.

Programming the Output Voltage

When the converter is in regulation there will be 600mV from the FB pin to the GND pin. Connect a two-resistor voltage divider across the VO pin and the GND pin with the output node connected to the FB pin. Scale the voltage-divider network such that the FB pin is 600mV with respect to the GND pin when the converter is regulating at the desired output voltage.

Programming the output voltage can be written as:

$$V_{REF} = V_{OUT} \cdot \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \quad \text{(EQ. 5)}$$

Where:

- V_{OUT} is the desired output voltage of the converter.
- V_{REF} is the voltage that the converter regulates to at the FB pin.
- R_{TOP} is the voltage-programming resistor that connects from the FB pin to the VO pin. It is usually chosen to set the gain of the control-loop error amplifier. It follows that R_{BOTTOM} will be calculated based upon the already selected value of R_{TOP}.
- R_{BOTTOM} is the voltage-programming resistor that connects from the FB pin to the GND pin.

Calculating the value of R_{BOTTOM} can now be written as:

$$R_{BOTTOM} = \frac{V_{REF} \cdot R_{TOP}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 6)}$$

Programming the PWM Switching Frequency

The PWM switching frequency F_{OSC} is programmed by the resistor R_{FSET} that is connected from the FSET pin to the GND pin. Programming the approximate PWM switching frequency can be written as:

$$F_{OSC} = \frac{1}{60 \cdot R_{FSET} \cdot [1 \times 10^{-12}]} \quad \text{(EQ. 7)}$$

Estimating the value of R_{FSET} can now be written as:

$$R_{FSET} = \frac{1}{60 \cdot F_{OSC} \cdot [1 \times 10^{-12}]} \quad \text{(EQ. 8)}$$

Where:

- F_{OSC} is the PWM switching frequency.
- R_{FSET} is the F_{OSC} programming resistor.
- 60 x [1 x 10^{-12}] is a constant.

Selection of the LC Output Filter

The duty cycle of a buck converter is ideally a function of the input voltage and the output voltage. This relationship can be written as:

$$D(V_{IN}) = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 9)}$$

Where:

- D is the PWM duty cycle.
- V_{IN} is the input voltage to be converted.
- V_{OUT} is the regulated output voltage of the converter.

The output inductor peak-to-peak ripple current can be written as:

$$I_{PP} = \frac{V_{OUT} \cdot [1 - D(V_{IN})]}{F_{OSC} \cdot L_O} \quad \text{(EQ. 10)}$$

Where:

- I_{PP} is the peak-to-peak output inductor ripple current.
- F_{OSC} is the PWM switching frequency.
- L_O is the nominal value of the output inductor.

A typical step-down DC/DC converter will have an I_{PP} of 20% to 40% of the nominal DC output load current. The value of I_{PP} is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistance the inductor winding, DCR. The DC copper loss of the inductor can be estimated by:

$$P_{COPPER} = [I_{LOAD}]^2 \cdot DCR \quad \text{(EQ. 11)}$$

The inductor copper loss can be significant in the total system power loss. Attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{PP} can flow. Current I_{PP} develops a corresponding ripple voltage V_{PP} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages can be written as:

$$\Delta V_{ESR} = I_{PP} \cdot ESR \quad \text{(EQ. 12)}$$

and

$$\Delta V_C = \frac{I_{PP}}{8 \cdot C_O \cdot F_{OSC}} \quad \text{(EQ. 13)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be

paralleled to adjust the ESR to achieve the required V_{PP}. The inductance of the capacitor can cause a brief voltage dip when the load transient has an extremely high slew rate. Low inductance capacitors constructed with reverse package geometry are available.

A capacitor dissipates heat as a function of RMS current. Be sure that I_{PP} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current. Take into account that the specified value of a capacitor can drop as much as 50% as the DC voltage across it increases.

Selection of the Input Capacitor

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. Figure 5 is a graph of the input RMS ripple current, normalized relative to output load current, as a function of duty cycle that is adjusted for converter efficiency. The ripple current calculation is written as:

$$I_{IN\_RMS} = \frac{\sqrt{(I_{MAX}^2 \cdot (D - D^2)) + \left(x \cdot I_{MAX}^2 \cdot \frac{D}{12}\right)}}{I_{MAX}} \quad \text{(EQ. 14)}$$

Where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- x is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter which is written as:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF}$$

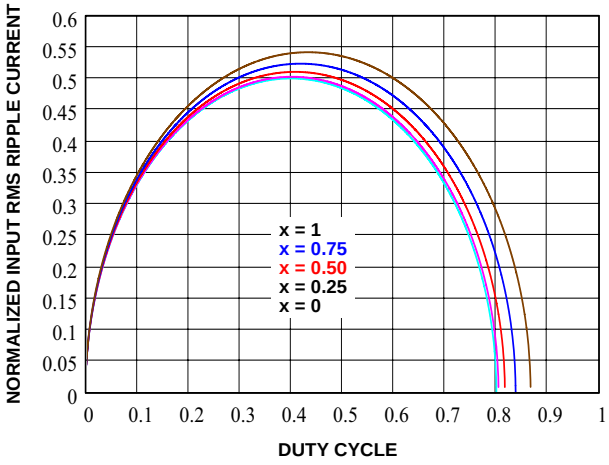


FIGURE 5. NORMALIZED RMS INPUT CURRENT FOR x = 0.8

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain terminal of the top-side MOSFET and the source terminal of the bottom-side MOSFET, in order to reduce the voltage ringing created by the switching current across parasitic circuit elements.

MOSFET Selection and Considerations

Typically, MOSFETS cannot tolerate even brief excursions beyond their maximum drain to source voltage rating. The MOSFETS used in the power conversion stage of the converter should have a maximum V_{DS} rating that exceeds the upper voltage tolerance of the input power source, and the voltage spike that occurs when the MOSFET switches off. Placing a low ESR ceramic capacitor as close as practical across the drain of the top-side MOSFET and the source of the bottom-side MOSFET will reduce the amplitude of the turn-off voltage spike.

The MOSFET input capacitance C_{ISS}, and on-state drain to source resistance $r_{DS(ON)}$, are to an extent, inversely related; reduction of $r_{DS(ON)}$ typically results in an increase of C_{ISS}. These two parameters affect the efficiency of the converter in different ways. The $r_{DS(ON)}$ affects the power loss when the MOSFET is completely turned on and conducting current. The C_{ISS} affects the power loss when the MOSFET is actively switching. Switching time increases as C_{ISS} increases. When the MOSFET switches it will briefly conduct current while the drain to source voltage is still present. The power dissipation during this time is substantial so it must be kept as short as practical. Often the top-side MOSFET and the bottom-side MOSFET are different devices due to the trade-offs that have to be made between C_{ISS} and $r_{DS(ON)}$.

The bottom-side MOSFET power loss is dominated by $r_{DS(ON)}$ because it conducts current for the majority of the PWM switching cycle; the $r_{DS(ON)}$ should be small. The switching loss is small for the bottom-side MOSFET even though C_{ISS} is large due to the low $r_{DS(ON)}$ of the device, because the drain to source voltage is clamped by the body diode. The top-side MOSFET power loss is dominated by C_{ISS} because it conducts current for the minority of the PWM switching cycle; the C_{ISS} should be small. The switching loss of the top-side MOSFET is large compared to the bottom-side MOSFET because the drain to source voltage is not clamped. For the bottom-side MOSFET, its power loss can be assumed to be the conduction loss only and can be written as:

$$P_{CONBS}D(V_{IN}) \approx [I_{LOAD}]^2 \cdot r_{DS(ON)BS} \cdot [1 - D(V_{IN})] \quad \text{(EQ. 15)}$$

For the top-side MOSFET, its conduction loss can be written as:

$$P_{CONTS}D(V_{IN}) = [I_{LOAD}]^2 \cdot r_{DS(ON)TS} \cdot D(V_{IN}) \quad \text{(EQ. 16)}$$

For the top-side MOSFET, its switching loss can be written as:

$$P_{SWTS}(V_{IN}) = \frac{V_{IN} \cdot I_{VAL} \cdot T_{ON} \cdot F_{OSC}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot T_{OFF} \cdot F_{OSC}}{2} \quad \text{(EQ. 17)}$$

The peak and valley current of the inductor can be obtained based on the inductor peak-to-peak current and the load current. The turn-on and turn-off time can be estimated with the given gate driver parameters in the Electrical Specification Table.

Selecting The Bootstrap Capacitor

The selection of the bootstrap capacitor can be written as:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 18)}$$

Where:

- Q_g is the total gate charge required to switch the top-side MOSFET
- ΔV_{BOOT}, is the maximum allowed voltage decay across the boot capacitor each time the MOSFET is switched on

As an example, suppose the top-side MOSFET has a total gate charge Q_G, of 25nC at V_{GS} = 5V, and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; select at least the first standard component value of greater capacitance than calculated, that being 0.15µF. Use an X7R or X5R ceramic capacitor.

Compensating the Converter

The LC output filter has a double pole at its resonant frequency that causes the phase to abruptly roll downward. The R^3 modulator used in the ISL8106 makes the LC output filter resemble a first order system in which the closed loop stability can be achieved with a Type II compensation network.

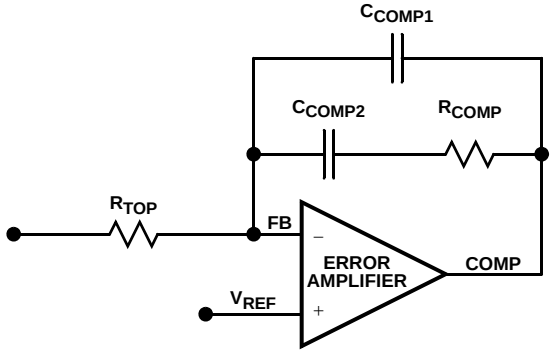


FIGURE 6. SYSTEM CONTROL BLOCK DIAGRAM

Figure 7 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage is regulated to the reference voltage level. The error amplifier output is compared with the oscillator triangle wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the LX node. The PWM wave is smoothed by the output filter. The output filter capacitor bank's equivalent series resistance is represented by the series resistor ESR.

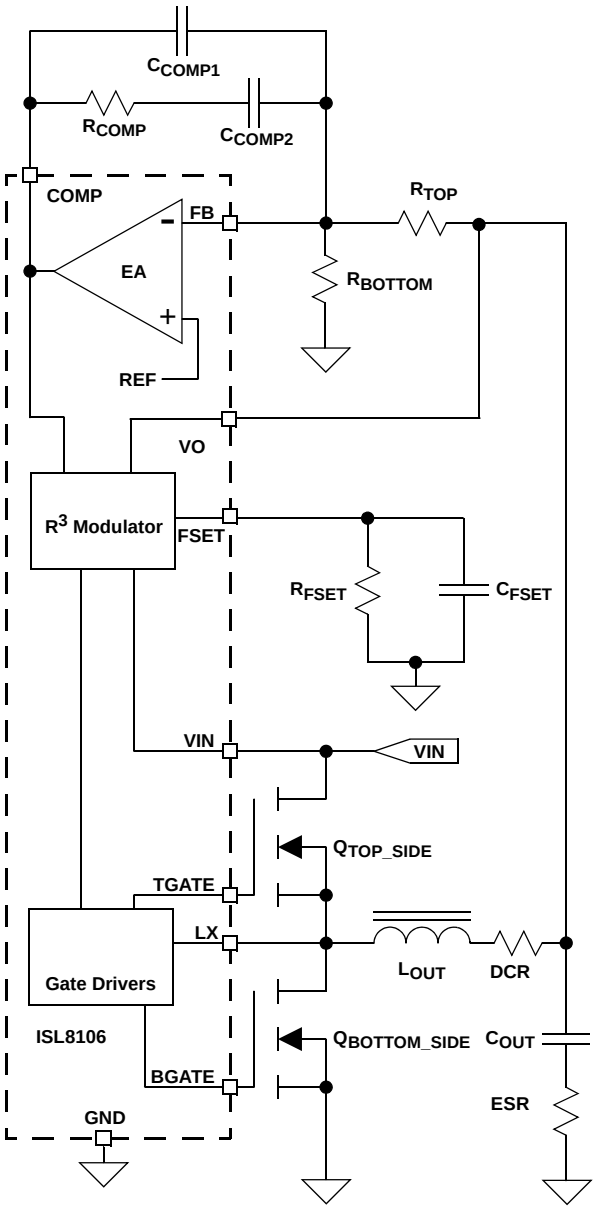


FIGURE 7. COMPENSATION REFERENCE CIRCUIT

The control loop model of the ISL8106 is partitioned into function blocks consisting of:

- The duty cycle to Vo transfer function $G_{VD}(s)$ which is determined by the value of the output power components, input voltage, and output voltage.
- The Vcomp to duty cycle transfer function $F_m(s)$ which is determined by the PWM frequency, input voltage, output voltage, resistor R_{FSET}, and capacitor C_{FSET}.
- The product of the $G_{VD}(s)$ and $F_m(s)$ transfer functions is expressed as the V_{COMP} to Vo transfer function $G_{VOVC}(s)$.
- The type-two compensation network $G_{COMP}(s)$ that connects across the COMP and FB pins.
- The product of the $G_{COMP}(s)$ and $G_{VOVC}(s)$ transfer functions is expressed as the loop transfer function T(s).

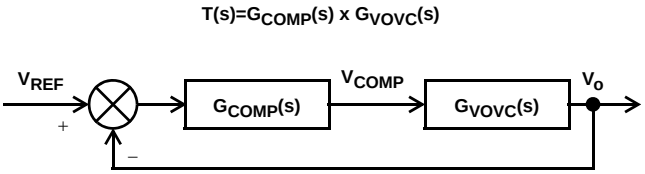


FIGURE 8. SYSTEM CONTROL BLOCK DIAGRAM

The compensator transfer function can be written as:

$$G_{COMP}(s) = \frac{\omega_i \cdot \left[1 + \frac{s}{\omega_{z1}}\right]}{s \cdot \left[1 + \frac{s}{\omega_{p1}}\right]} \quad \text{(EQ. 19)}$$

where the compensator zero *fz1* is

$$\omega_{z1} = \frac{1}{R_{COMP} \cdot C_{COMP2}} \quad \text{(EQ. 20)}$$

$$f_{z1} = \frac{\omega_{z1}}{2 \cdot \pi} \quad \text{(EQ. 21)}$$

the compensator pole *fp1* is

$$\omega_{p1} = \left[\frac{1}{C_{COMP1}} + \frac{1}{C_{COMP2}}\right] \cdot \frac{1}{R_{COMP}} \quad \text{(EQ. 22)}$$

$$f_{p1} = \frac{\omega_{p1}}{2 \cdot \pi} \quad \text{(EQ. 23)}$$

and

$$\omega_i = \frac{1}{R_{COMP} \cdot [C_{COMP1} + C_{COMP2}]} \quad \text{(EQ. 24)}$$

The Your local Intersil representative can provide a PC-based tool that can be used to calculate compensation network component values and help simulate the loop frequency response. The compensation network consists of the internal error amplifier of the ISL8106 and the external components R_{TOP}, R_{COMP}, C_{COMP1}, and C_{COMP2} as well as the frequency setting components R_{FSET}, and C_{FSET}, are identified in the schematic Figure 7.

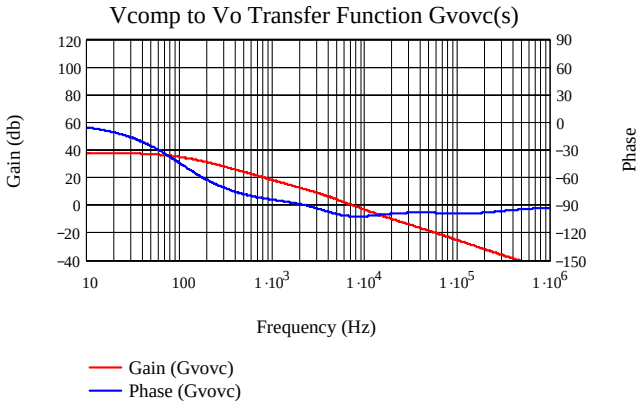


FIGURE 9. OPEN LOOP TRANSFER FUNCTION

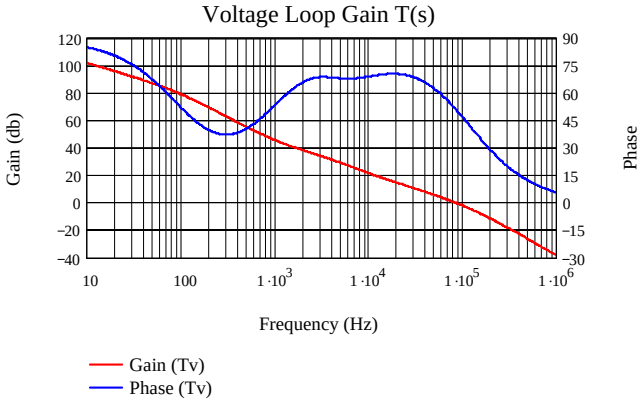
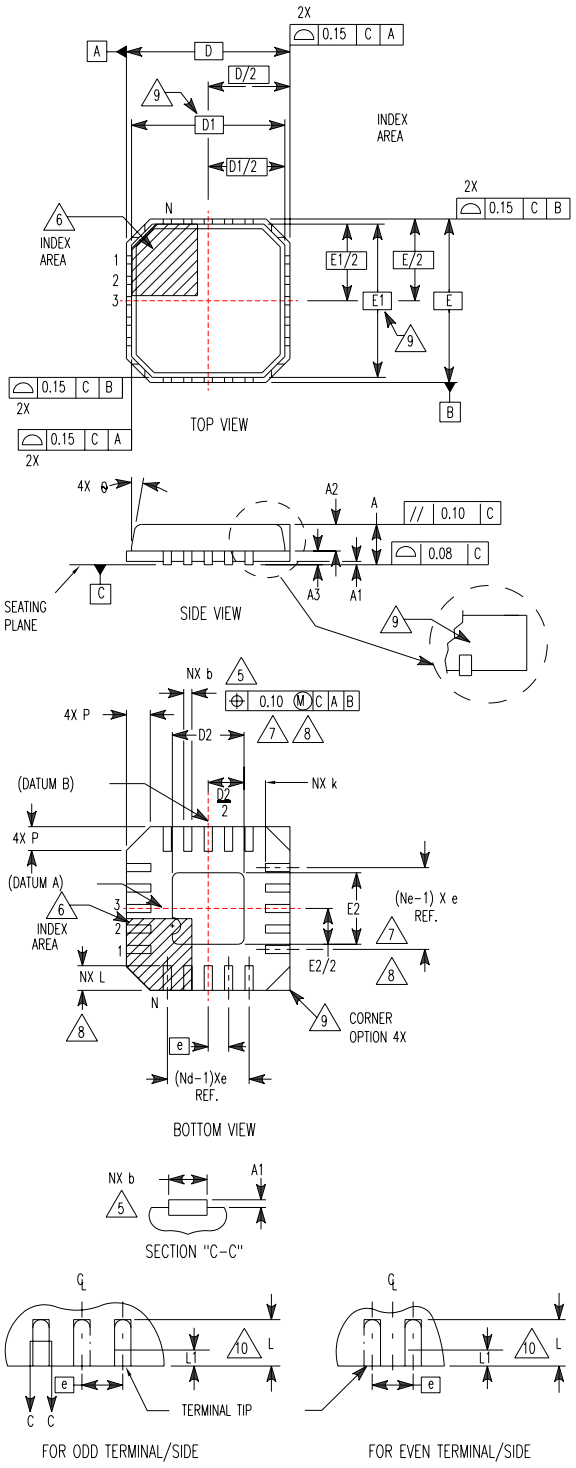


FIGURE 10. CLOSED LOOP TRANSFER FUNCTION

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerances conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.