NCP6924

6 Channel PMIC with 2 DCDC Converters and 4 LDOs

The NCP6924 integrated circuit is part of the ON Semiconductor mini power management IC family (PMIC). It is optimized to supply battery powered portable application sub−systems such as camera function, microprocessors. This device integrates two high efficiency up to 1.0 A step−down DCDC converters with Dynamic Voltage Scale (DVS) and 4 low dropout (LDO) voltage regulators in a WLCSP30 2.46 x 2.06 mm package.

Features

- 2 DCDC Converters (3 MHz, 1 μH/10 μF, up to 1.0 A)
  - Peak Efficiency 95%
  - Programmable Output Voltage: 0.6 V to 3.3 V by 12.5 mV Steps
- 4 Low Noise − Low Drop Out Regulators (2.2 μF, 150 mA and 300 mA)
  - Programmable Output Voltage: 1.0 V to 3.3 V by 50 mV Steps
  - 50 μVrms Typical Low Output Noise
- Control
  - 400 kHz / 3.4 MHz I^2C Compatible
  - Independent Enable Pins or I^2C Enable Control Bits
  - Power Good and Interrupt Output Pin
  - Customizable Power Up Sequence
- Extended Input Voltage Range from 2.3 V to 5.5 V
- 105 μA Very Low Quiescent Current at No Load
- Less than 1 μA Off Mode Current
- Small Footprint: 2.46 x 2.06 mm WLCSP 0.4 mm Pitch
- These are Pb−Free Devices

Typical Applications

- Cellular Phones, Tablets
- Digital Cameras

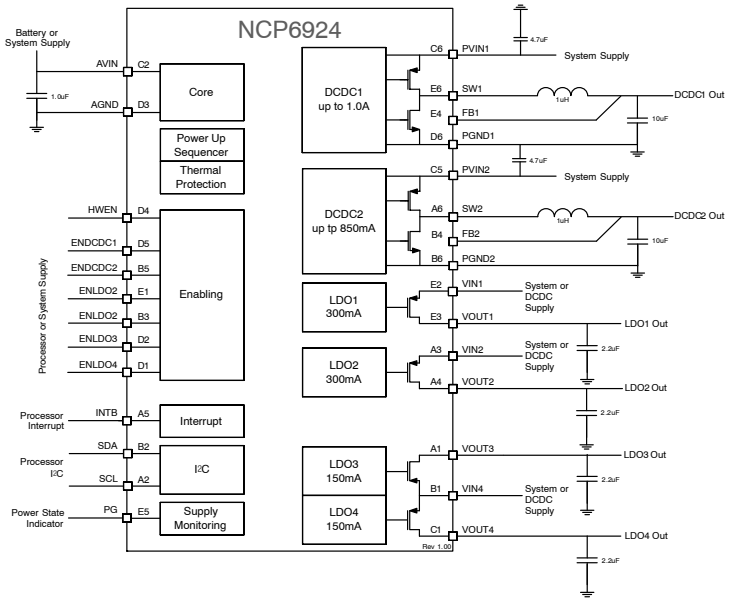


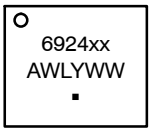
Figure 1. Application Schematic

ON Semiconductor®

http://onsemi.com

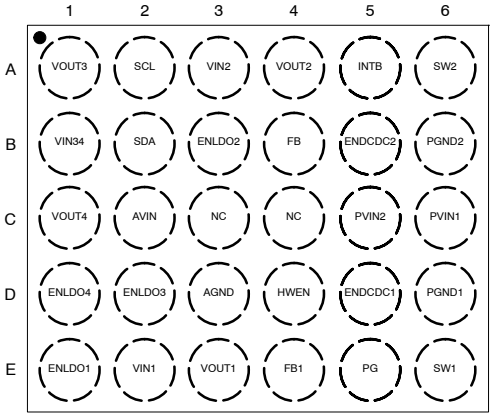
WLCSP30
CASE 567CU

MARKING DIAGRAM*



xx	= AH for NCP6924AH (HWEN Version) = AE for NCP6924AE (Enable Version) = BH for NCP6924BFCHT1G = CH for NCP6924CFCHT1G
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.)



(Top View)
30 pins 2.46 x 2.06 mm WLCSP, 0.44 mm Pitch

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 39 of this data sheet.

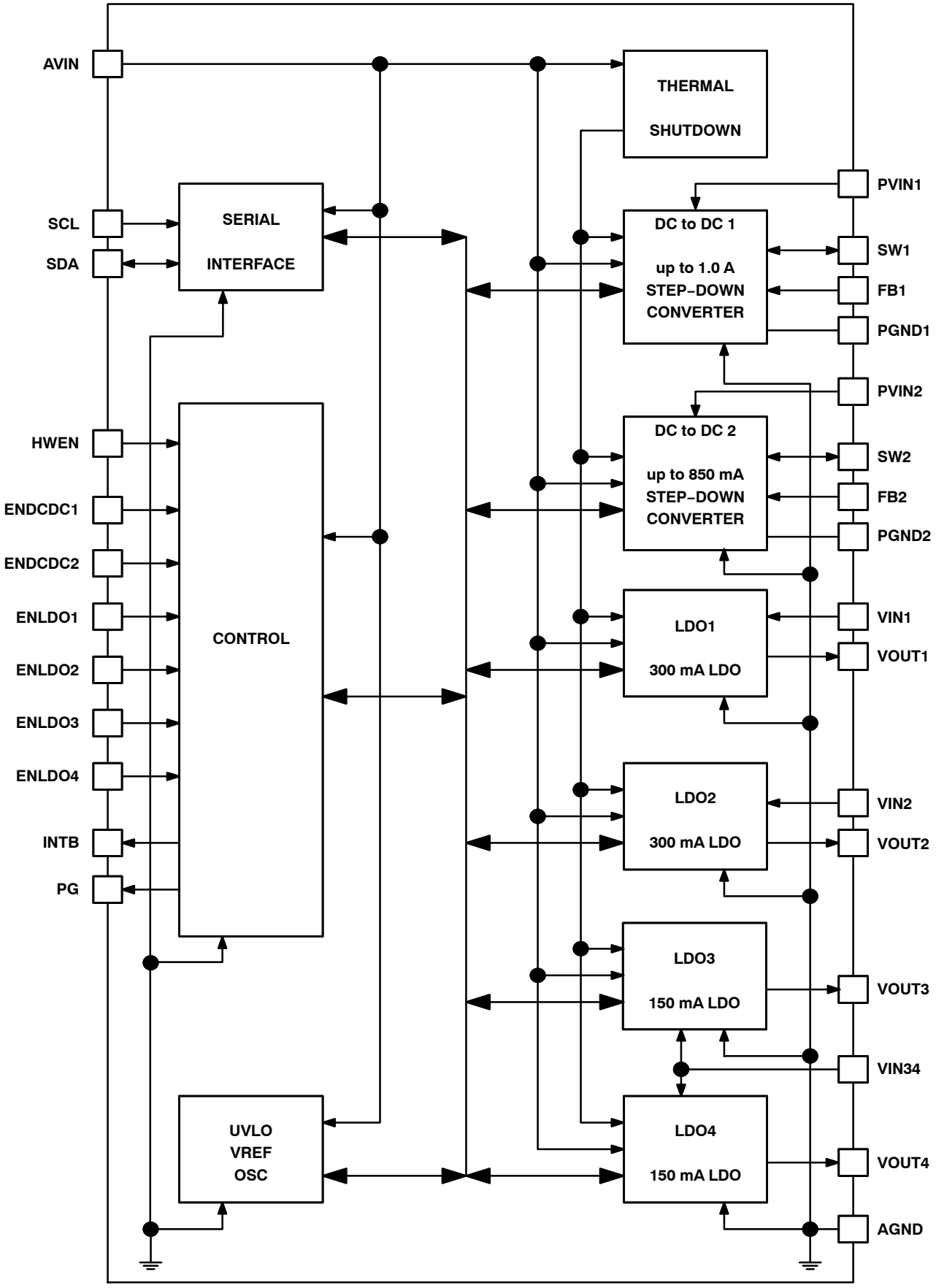


Figure 2. Functional Block Diagram

PIN OUT DESCRIPTION

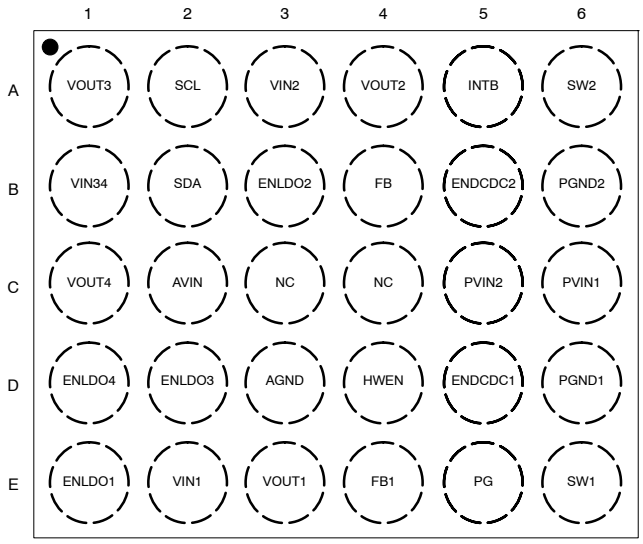


Figure 3. Pin Out (Top view)

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
SUPPLY			
C2	AVIN	Analog Input	Analog Supply. This pin is the device analog and digital supply. A 1.0 μF ceramic capacitor or larger must bypass this input to ground. This capacitor should be placed as close as possible to this pin.
D3	AGND	Analog Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
CONTROL AND SERIAL INTERFACE			
D4	HWEN	Digital Input	Hardware Enable. Active high will enable the part. There is an internal pull down resistor on this pin.
D5	ENDCDC1	Digital Input	DCDC1 Enable. Active high will enable DCDC1. There is internal pull down resistor on this pin.
B5	ENDCDC2	Digital Input	DCDC2 Enable, Active high will enable DCDC2. There is internal pull down resistor on this pin.
E1	ENLDO1	Digital Input	LDO1 Enable, Active high will enable LDO1. There is internal pull down resistor on this pin.
B3	ENLDO2	Digital Input	LDO2 Enable, Active high will enable LDO2. There is internal pull down resistor on this pin.
D2	ENLDO3	Digital Input	LDO3 Enable Active high will enable LDO3. There is internal pull down resistor on this pin.
D1	ENLDO4	Digital Input	LDO4 Enable Active high will enable LDO4. There is internal pull down resistor on this pin.
A2	SCL	Digital Input	I^2C interface Clock line
B2	SDA	Digital Input/Output	I^2C interface Bi−directional Data line.
E5	PG	Digital Output	Power Good open drain output.
A5	INTB	Digital Output	Interrupt open drain output.
DCDC CONVERTERS			
C6	PVIN1	Power Input	DCDC1 Power Supply. This pin must be decoupled to ground by a 4.7 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
E6	SW1	Power Output	DCDC1 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
E4	FB1	Analog Input	DCDC1 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
DCDC CONVERTERS			
D6	PGND1	Power Ground	DCDC1 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track..
C5	PVIN2	Power Input	DCDC2 Power Supply. This pin must be decoupled to ground by a 4.7 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
A6	SW2	Power Output	DCDC2 Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
B4	FB2	Analog Input	DCDC2 Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
B6	PGND2	Power Ground	DCDC1 Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
LDO REGULATORS			
E2	VIN1	Power Input	LDO1 Power Supply.
E3	VOUT1	Power Output	LDO1 Output Power. This pin requires a 2.2 μF decoupling capacitor.
A3	VIN2	Power Input	LDO2 Power Supply
A4	VOUT2	Power Output	LDO2 Output Power. This pin requires a 2.2 μF decoupling capacitor.
B1	VIN34	Power Input	LDO3 & LDO4 Power Supply
A1	VOUT3	Power Output	LDO3 Output Power. This pin requires a 2.2 μF decoupling capacitor.
C1	VOUT4	Power Output	LDO4 Output Power. This pin requires a 2.2 μF decoupling capacitor.

Table 2. MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Analog and power pins: AVIN, PVIN1, SW1, PVIN2, SW2, VIN1, VOUT1, VIN2, VOUT2, VIN34, VOUT3, VOUT4, PG, INTB, FB1, FB2	V_A	−0.3 to + 6.0	V
Digital pins: SCL, SDA, HWEN, ENDCDC1, ENDCDC2, ENLDO1, ENLDO2, ENLDO3, ENLDO4: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_A +0.3 ≤ 6.0 10	 V mA
Human Body Model (HBM) ESD Rating (Note 2)	ESD HBM	2000	V
Machine Model (MM) ESD Rating (Note 2)	ESD MM	200	V
Latch up Current: (Note 3) All digital pins All other pins	I_{LU}	 ±10 ±100	mA
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. All voltages are related to AGND.
2. ESD rated to the following:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
3. Latch up Current per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$AV_{IN,}$ PV_{IN}	Analog and Power Supply		2.3		5.5	V
LDO_{VIN}	LDO Input Voltage range		1.7		5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range (Note 6)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 7)	WLCSP30 on Demo−board	−	55	−	°C/W
P_D	Power Dissipation Rating (Note 8)	$T_A \le 85°C$	−	730	−	mW
		$T_A = 40°C$	−	1550	−	mW
L	Inductor for DC to DC converters (Note 5)		0.5	1	2.2	μH
Co	Output Capacitor for DC to DC Converters (Note 5)		5	10	40	μF
	Output Capacitors for LDO (Note 5)		1.20	2.2	5.0	μF
C_{IN}	Input Capacitor for DC to DC Converters (Note 5)		3.0	4.7	−	μF

5. Refer to the Application Information section of this data sheet for more details.
6. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
7. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a NCP6924EVB board. It is a multilayer board with 1−once internal power and ground planes and 2−once copper traces on top and bottom of the board.
8. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}$$

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. $AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34}$ = 3.6 V and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C and default configuration, unless otherwise specified (Note 11).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS AV_{IN} – PV_{IN1} – PV_{IN2} – V_{IN1} – V_{IN2} – V_{IN34}						
IQ	Operating quiescent current	DCDC1&2 on, no load, no switching LDOs off, T_A = up to +85°C	−	60	100	μA
		DCDC1&2 on, no load, no switching LDOs on, no load, T_A = up to +85°C	−	105	190	
		DCDC1&2 Off LDOs on, no load, T_A = up to +85°C	−	55	100	
ISLEEP	Sleep mode current	HWEN pin on All DC to DC and LDOs off V_{IN} = 2.3 V to 5.5 V, T_A = up to +85°C	−	7	15	μA
IOFF	Shutdown current	All DCDCs and LDOs off HWEN pin = off I^2C interface disabled V_{IN} = 2.3 V to 5.5 V, T_A = up to +85°C	−	0.1	2.0	μA
DCDC1&2 STEP DOWN CONVERTERS						
$PV_{IN1,2}$	Input Voltage Range		2.3	−	5.5	V
I_{OUTMAX}	Maximum Output Current	NCP6924AFCHT1G (DCDC1&2) & NCP6924AFCET1G (DCDC1&2)	0.80	−	−	A
		NCP6924BFCHT1G (DCDC1&2), NCP6924CFCHT1G (DCDC2)	0.85	−	−	
		NCP6924CFCHT1G (DCDC1)	1.00	−	−	
ΔV_{OUT}	Output Voltage DC Error	I_{OUT} = 300 mA	−1	0	1	%

9. ENx (enable control signal of output channel, ENDCDC1, ENDCDC2, ENLDO1, ENLDO2, ENLDO3, ENLDO4).
10. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
11. Refer to the Application Information section of this data sheet for more details.
12. Guaranteed by design and characterized.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. $AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34}$ = 3.6 V and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C and default configuration, unless otherwise specified (Note 11).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DCDC1&2 STEP DOWN CONVERTERS						
F_{SW}	Switching Frequency		2.7	–	3.3	MHz
R_{ONHS}	P−Channel MOSFET On Resistance	From PVIN1 / PVIN2 pins to SW1 / SW2 pins T_J up to 85°C, PV_{IN} = 5.5 V	–	250	–	mΩ
R_{ONLS}	N−Channel MOSFET On Resistance	From SW1 / SW2 pins to PGND1 / PGND2 pins, T_J up to 85°C, PV_{IN} = 5.5 V	–	200	–	mΩ
I_{PK}	Peak Inductor Current	Open loop, 2.3 V ≤ $PV_{IN1,2}$ ≤ 5.5 V NCP6924AFCHT1G (DCDC1&2) & NCP6924AFCET1G (DCDC1&2)	1.00	1.30	1.60	A
		Open loop, 2.3 V ≤ $PV_{IN1,2}$ ≤ 5.5 V NCP6924BFCHT1G (DCDC1&2), NCP6924CFCHT1G (DCDC2)	1.05	1.35	1.65	
		Open loop, 2.3 V ≤ $PV_{IN1,2}$ ≤ 5.5 V NCP6924CFCHT1G (DCDC1)	1.20	1.60	2.00	
	Load Regulation	I_{OUT} from 300 mA to I_{OUTMAX}	–	5	–	mV/A
	Line Regulation	I_{OUT} = 300 mA 2.3 V ≤ PV_{IN1} ≤ 5.5 V	–	0	–	mV
D	Maximum Duty Cycle		–	100	–	%
t_{START}	Soft−Start Time	Time from I^2C command ACK to 90% of Output Voltage	–	–	1	ms
$R_{DISDCDC}$	DCDC Active Output Discharge		–	7	–	Ω
LDO1 AND LDO2						
$V_{IN1,2}$	LDO1 and LDO2 input voltage range, 300 mA load	V_{OUT} ≤ 1.5 V, I_{OUT} = 300 mA	1.7	–	5.5	V
		V_{OUT} > 1.5 V, I_{OUT} = 300 mA	V_{out} + V_{DROP}	–	5.5	
$I_{OUTMAX1,2}$	Maximum Output Current		300	–	–	mA
$I_{SC1,2}$	Short Circuit Protection		360	–	700	mA
$\Delta V_{OUT1,2}$	Output Voltage Accuracy DC	I_{OUT} = 300 mA	−2	V_{NOM}	+2	%
	Load Regulation	I_{OUT} = 0 mA to 300 mA	–	0.4	–	%
	Line Regulation	V_{IN} = max(1.7 V, V_{OUT} + V_{DROP}) to 5.5 V I_{OUT} = 300 mA	–	0.3	–	%
V_{DROP}	Dropout Voltage	I_{OUT} = 300 mA, V_{OUT} = V_{NOM} − 2% V_{OUT} = 1.8 V	–	130	250	mV
		I_{OUT} = 300 mA, V_{OUT} = V_{NOM} − 2% V_{OUT} = 2.8 V	–	90	200	mV
PSRR	Ripple Rejection	F = 1 kHz V_{OUT} = 1.1 V, I_{OUT} = 100 mA	–	−65	–	dB
		F = 10 kHz V_{OUT} = 1.1 V, I_{OUT} = 100 mA	–	−55	–	
Noise		100 Hz → 100 kHz, V_{OUT} = 1.1 V, I_{OUT} = 100 mA	–	55	–	μV
$R_{DISLDO1,2}$	LDO Active Output Discharge		–	25	–	Ω

9. ENx (enable control signal of output channel, ENDCDC1, ENDCDC2, ENLDO1, ENLDO2, ENLDO3, ENLDO4).
10. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
11. Refer to the Application Information section of this data sheet for more details.
12. Guaranteed by design and characterized.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. $AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34}$ = 3.6 V and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C and default configuration, unless otherwise specified (Note 11).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO3 AND LDO4						
V_{IN34}	LDO3 and LDO4 Input Voltage	$V_{OUT} \le 1.5$ V, I_{OUT} = 150 mA	1.7	–	5.5	V
		$V_{OUT} > 1.5$ V, I_{OUT} = 150 mA	V_{out}+ V_{DROP}	–	5.5	
$I_{OUTMAX3,4}$	Maximum Output Current		150	–	–	mA
$I_{SC3,4}$	Short Circuit Protection		200	–	600	mA
ΔV_{OUT}	Output Voltage Accuracy	I_{OUT} = 150 mA	−2	V_{NOM}	+2	%
	Load Regulation	I_{OUT} = 0 mA to 150 mA	–	0.4	–	%
	Line Regulation	V_{IN} = max(1.7 V, V_{OUT} + V_{DROP}) to 5.5 V I_{OUT} = 150 mA	–	0.3	–	%
V_{DROP}	Dropout Voltage	I_{OUT} = 150 mA, $V_{OUT} = V_{NOM} - 2\%$ V_{OUT} = 1.8 V	–	110	230	mV
		I_{OUT} = 150 mA, $V_{OUT} = V_{NOM} - 2$ % V_{OUT} = 2.8 V		70	180	
PSRR	Ripple Rejection	F = 1 kHz V_{OUT} = 1.1 V, I_{OUT} = 100 mA	–	−65	–	dB
		F = 10 kHz V_{OUT} = 1.1 V, I_{OUT} = 100 mA	–	−55	–	
Noise		10 Hz → 100 kHz V_{OUT} = 1.1 V, I_{OUT} = 100 mA		55		μV
$R_{DISLDO3,4}$	LDO Active Output Discharge		–	25	–	Ω
HWEN / ENx (Note 9)						
V_{IH}	Positive Going Input High Voltage Threshold		1.1	–	–	V
V_{IL}	Negative Going Input Low Voltage Threshold		–	–	0.4	V
t_{FR}	Enable pin filter	(Note 12)	4	–	9	μs
I_{PD}	Enable Pins Pull−Down (input bias current)		–	0.1	1.0	μA
PG						
V_{PGL}	Power Good Low threshold	Falling edge as a percentage of nominal output voltage	86	90 of V_{NOM}	94	%
V_{PGHYS}	Power Good detection level		0	3	5	%
t_{RT}	Power Good Reaction Time DCDC case	Falling (Note 12) Rising (Note 12)	– 4	5 –	– 9	μs
	Power Good Reaction Time LDO case	Falling (Note 12) Rising (Note 12)	– 228	5 –	– 265	μs
V_{PGL}	Power Good low output voltage	I_{PG} = 5 mA	–	–	0.2	V
PG_{LK}	Power Good leakage current	3.6 V at PG pin when power good valid	–	–	100	nA
V_{PGH}	Power Good high output voltage	Open drain	–	–	5.5	V

9. ENx (enable control signal of output channel, ENDCDC1, ENDCDC2, ENLDO1, ENLDO2, ENLDO3, ENLDO4).
10. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
11. Refer to the Application Information section of this data sheet for more details.
12. Guaranteed by design and characterized.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. $AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34}$ = 3.6 V and default configuration, unless otherwise specified. Typical values are referenced to T_J = +25°C and default configuration, unless otherwise specified (Note 11).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INTB						
V_{INTBL}	INTB low output voltage	I_{INTB} = 5 mA	0	–	0.2	V
V_{INTBH}	INTB high output voltage	Open drain	–	–	5.5	V
$INTB_{LK}$	INTB leakage current	3.6 V at INTB pin when INTB valid	–	–	100	nA
I^2C						
V_{I2CINT}	High level at SCL/SDA line		–	–	5.0	V
V_{I2CIL}	SCL, SDA low input voltage	SCL, SDA pin (Notes 10 and 12)	–	–	0.5	V
V_{I2CIH}	SCL, SDA high input voltage	SCL, SDA pin (Notes 10 and 12)	$0.8xV_{I2CINT}$	–	–	V
V_{I2COL}	SCL, SDA low output voltage	I_{SINK} = 3 mA (Note12)	–	–	0.4	V
F_{SCL}	I^2C clock frequency	(Note 12)	–	–	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} falling	–	–	2.3	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} rising	60	–	200	mV
T_{SD}	Thermal Shut Down Protection		–	150	–	°C
$T_{WARNING}$	Warning Rising Edge		–	135	–	°C
T_{SDHYS}	Thermal Shut Down Hysteresis		–	35	–	°C

9. ENx (enable control signal of output channel, ENDCDC1, ENDCDC2, ENLDO1, ENLDO2, ENLDO3, ENLDO4).
10. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
11. Refer to the Application Information section of this data sheet for more details.
12. Guaranteed by design and characterized.

TYPICAL OPERATING CHARACTERISTICS

AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34} = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (LQH44PN1R0NP02) – C_{DCDC} = 10 μF 0603

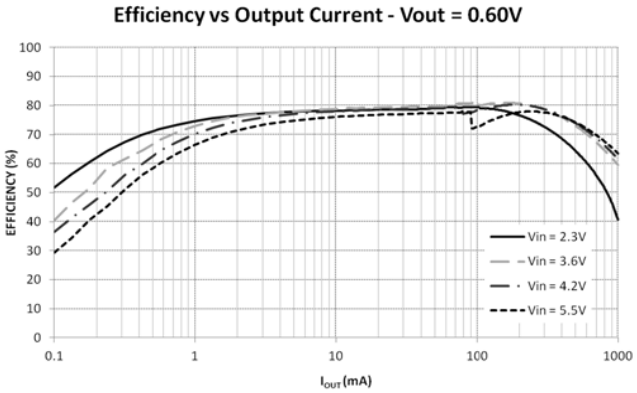


Figure 5. DCDC1 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 0.6 V

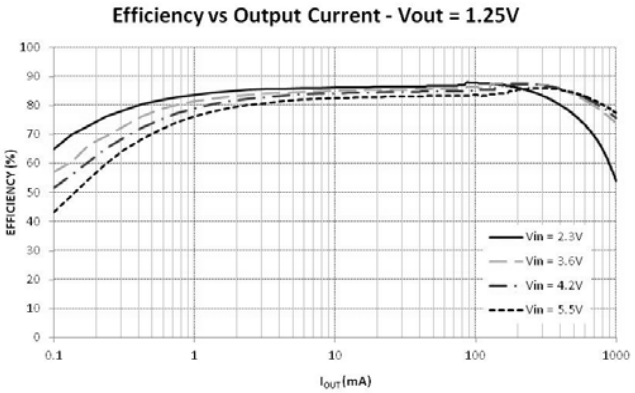


Figure 6. DCDC1 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 1.25 V

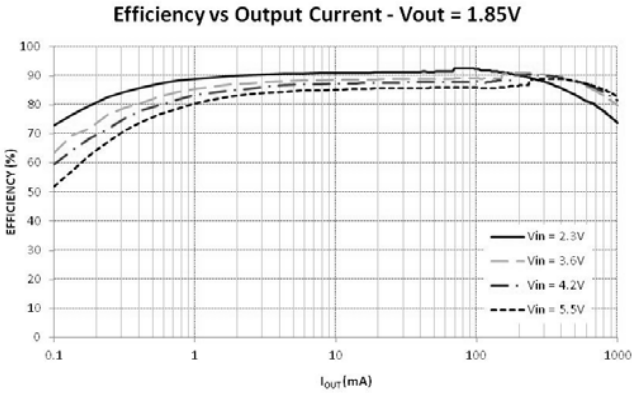


Figure 7. DCDC1 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 1.85 V

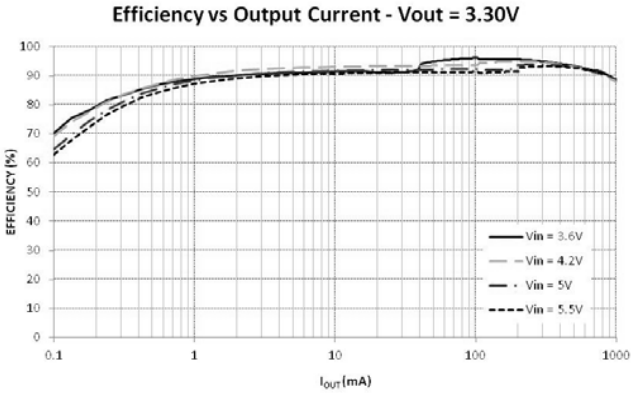


Figure 4. DCDC1 Efficiency vs. IOUT (auto mode) VOUT = 3.3 V

TYPICAL OPERATING CHARACTERISTICS

AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34} = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (LQH44PN1R0NP02) – C_{DCDC} = 10 μF 0603

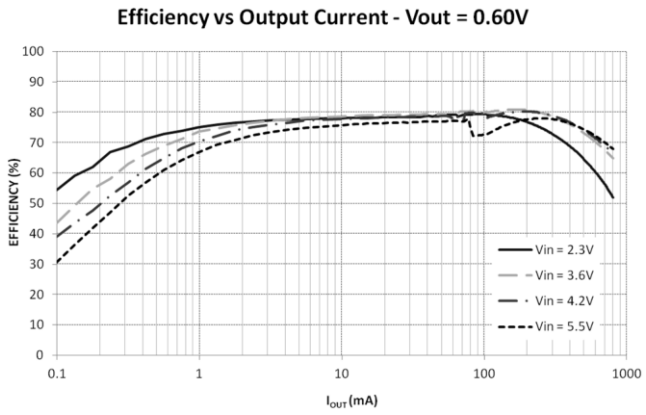


Figure 8. DCDC2 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 0.6 V

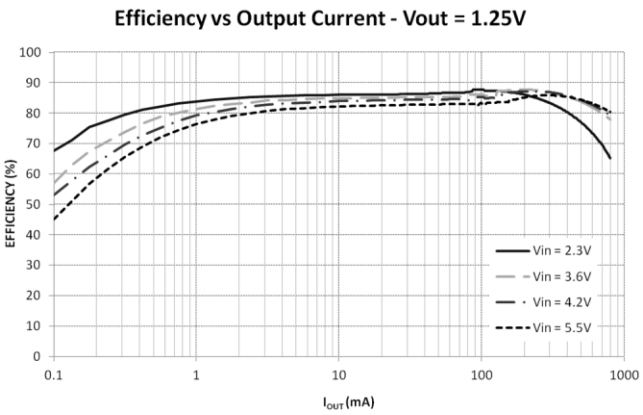


Figure 9. DCDC2 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 1.25 V

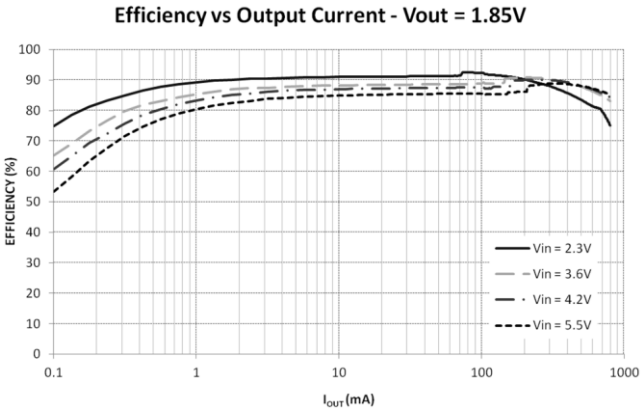


Figure 10. DCDC2 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 1.85 V

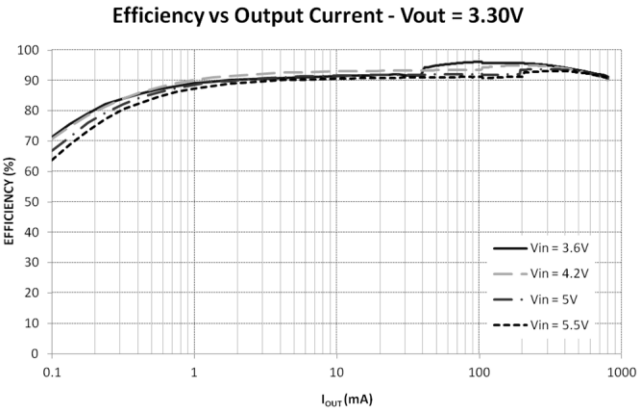


Figure 11. DCDC2 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 3.3 V

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (LQH44PN1R0NP02) – C_{DCDC} = 10 μF 0603

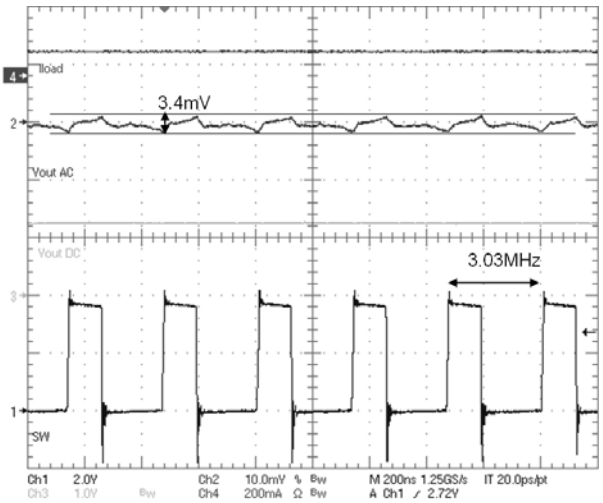


Figure 12. DCDC1 Ripple Voltage in PWM Mode (V_{IN} = 3.6 V – V_{OUT} = 1.25 V – I_{OUT} = 100 mA)

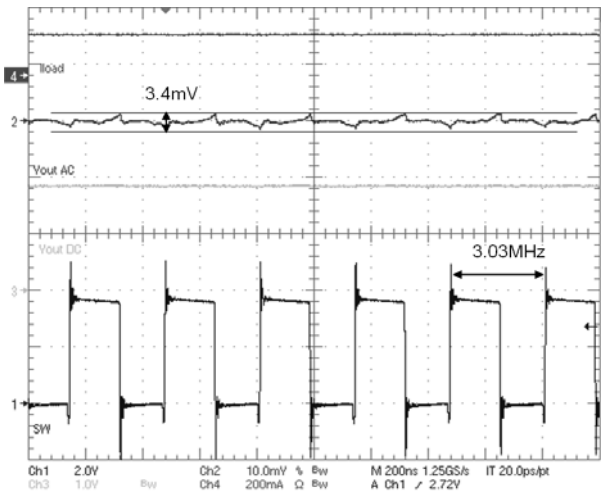


Figure 13. DCDC2 Ripple Voltage in PWM Mode (V_{IN} = 3.6 V – V_{OUT} = 1.85 V – I_{OUT} = 175 mA)

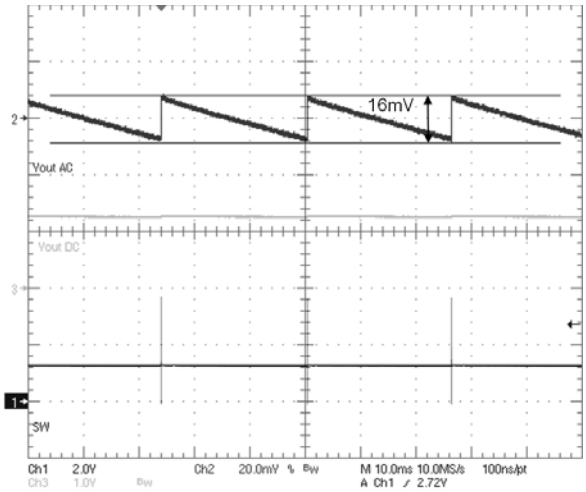


Figure 14. DCDC1 Ripple voltage in PFM mode (V_{IN} = 3.6 V – V_{OUT} = 1.25 V – No load)

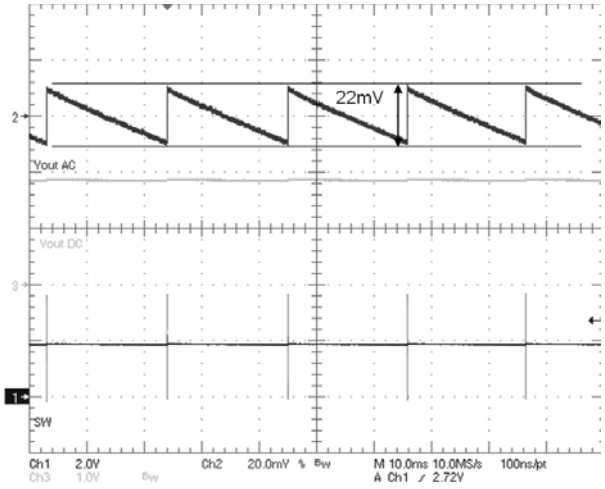


Figure 15. DCDC2 Ripple voltage in PFM mode (V_{IN} = 3.6 V – V_{OUT} = 1.85 V – No load)

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (LQH44PN1R0NP02) – C_{DCDC} = 10 μF 0603

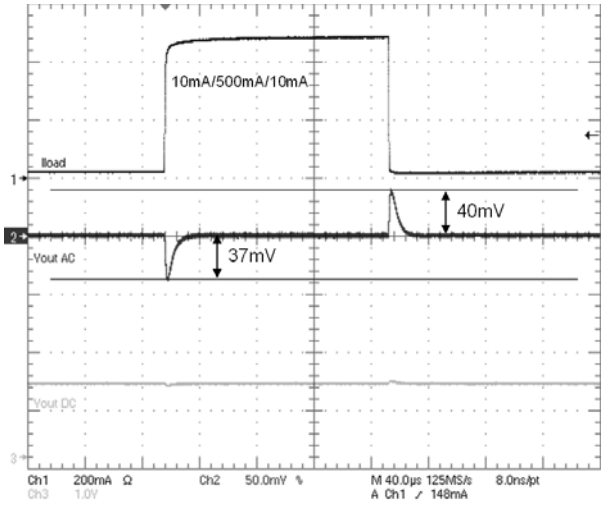


Figure 16. DCDC1 Load Transient Response (PWM Mode, V_{IN} = 3.6 V – V_{OUT} = 1.25 V)

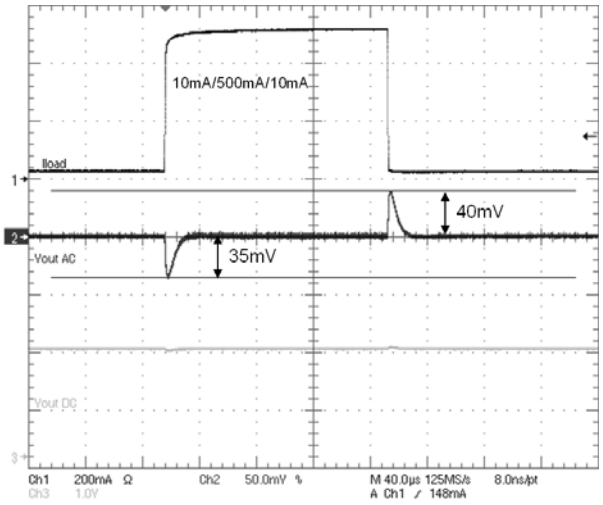


Figure 17. DCDC2 Load Transient Response (PWM Mode, V_{IN} = 3.6 V – V_{OUT} = 1.85 V)

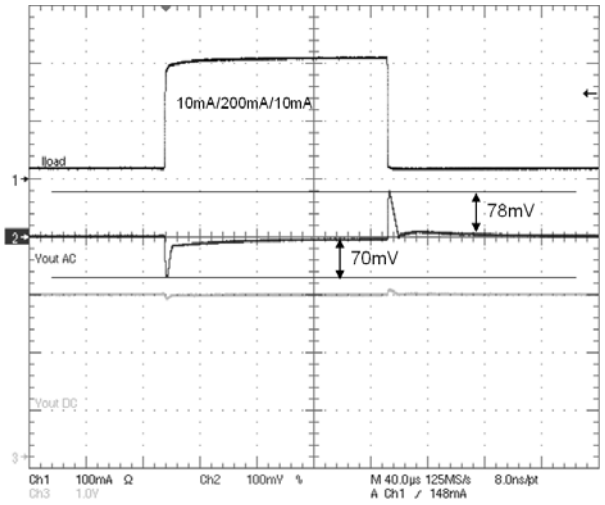


Figure 18. LDO1 Load Transient Response (V_{IN} = 3.6 V – V_{OUT} = 2.80 V)

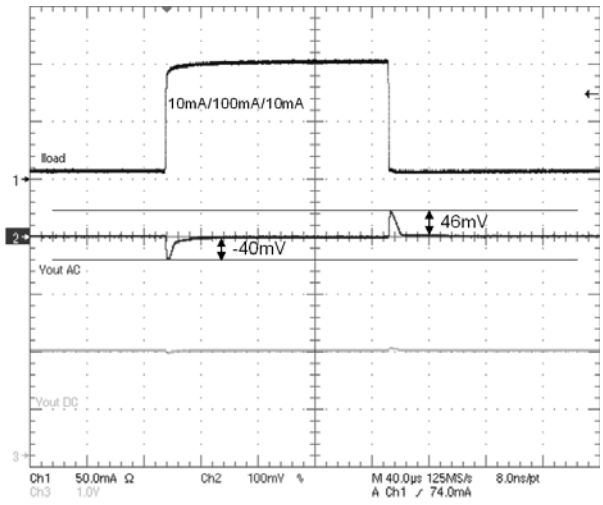


Figure 19. LDO4 Load Transient Response (V_{IN} = 3.6 V – V_{OUT} = 1.80 V)

TYPICAL OPERATING CHARACTERISTICS

$AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34}$ = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (LQH44PN1R0NP02) – C_{DCDC} = 10 μF 0603

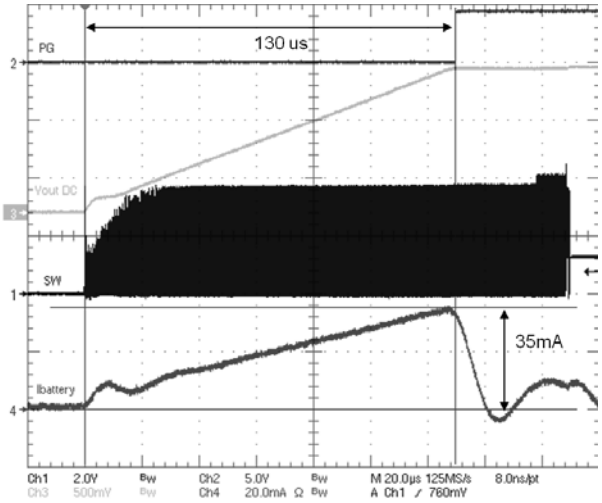


Figure 20. DCDC Soft−Start (Inrush Current, V_{IN} = 3.6 V – V_{OUT} = 1.25 V)

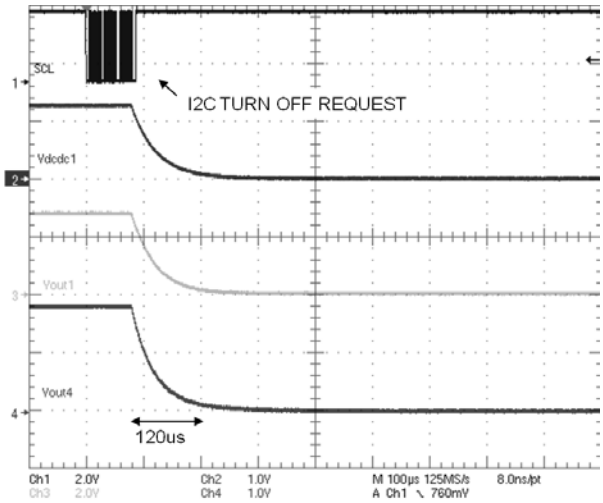


Figure 21. I²C Shutdown Sequence with Active Discharge Enabled

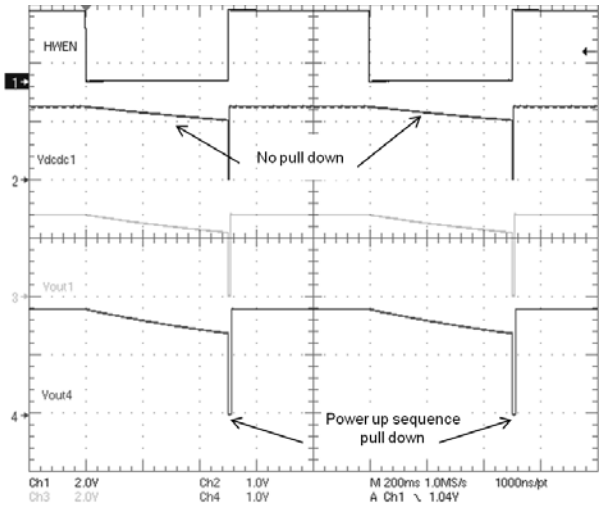


Figure 22. HWEN Shutdown Sequence with Active Discharge Disabled

TYPICAL OPERATING CHARACTERISTICS

AV_{IN} = PV_{IN1} = PV_{IN2} = V_{IN1} = V_{IN2} = V_{IN34} = 3.6 V (Unless otherwise noted). T_J = +25°C, DCDC1 = 1.25 V, DCDC2 = 1.85 V, LDO1&3 = 2.80 V, LDO3&4 = 1.80 V, C_{LDO} = 2.2 μF 0603, L_{DCDC} = 1.0 μF (LQH44PN1R0NP02) – C_{DCDC} = 10 μF 0603

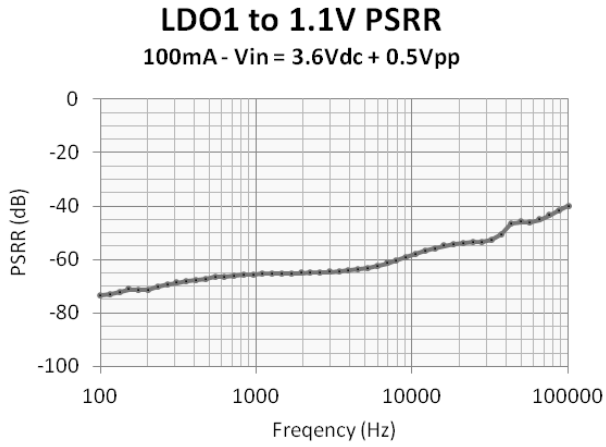


Figure 23. LDO1 PSRR
(V_{IN} = 3.6 V – V_{OUT} = 1.1 V – I_{OUT} = 100 mA)

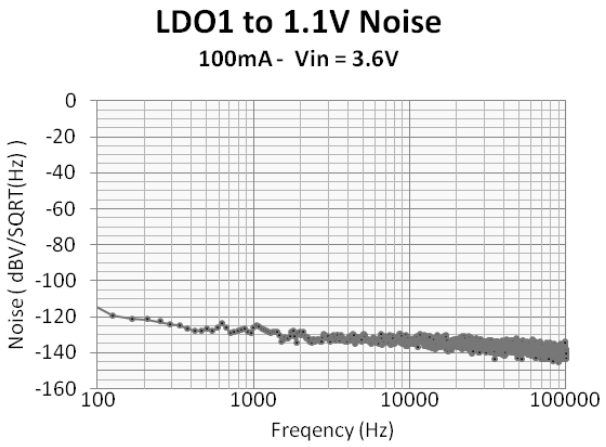


Figure 24. LDO1 Output Noise
(V_{IN} = 3.6 V – V_{OUT} = 1.1 V – I_{OUT} = 100 mA)

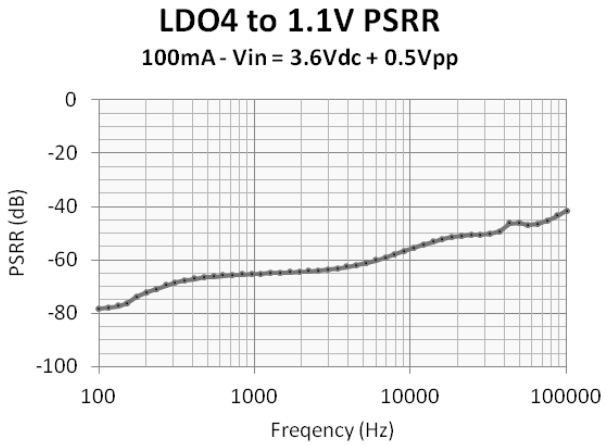


Figure 25. LDO4 PSRR
(V_{IN} = 3.6 V – V_{OUT} = 1.1 V – I_{OUT} = 100 mA)

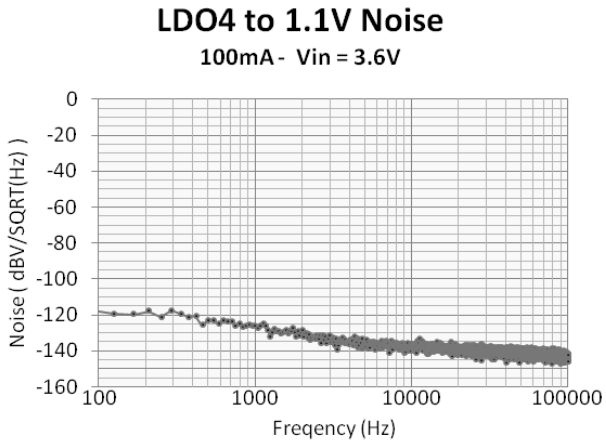


Figure 26. LDO4 Output Noise
(V_{IN} = 3.6 V – V_{OUT} = 1.1 V – I_{OUT} = 100 mA)

DETAILED OPERATING DESCRIPTION

General Description

The NCP6924 mini power management integrated circuit is optimized to supply different sub systems of battery powered portable applications. The IC can be supplied directly from the latest technology single cell batteries such as Lithium−Polymer as well as from triple alkaline cells. Alternatively, the IC can be supplied from a pre−regulated supply rail in case of multi−cell or main powered applications.

It integrates two switched mode DCDC converters and four low dropout linear regulators. The IC is widely programmable through an I^2C interface and includes low level IO signaling. An analog core provides the necessary references for the IC while a digital core ensures proper control.

The output voltage range, current capabilities and performance of the switched mode DCDC converters are well suited to supply the different peripherals in the system as well as to supply processor cores. To reduce overall power consumption of the application, Dynamic Voltage Scaling (DVS) is supported on the DCDC converters. For PWM operation, the converters run on a local 3MHz clock. A low power PFM mode is provided that ensures that even at low loads high efficiency can be obtained. All the switching components are integrated including the compensation networks and synchronous rectifier. Only a small sized 1uH inductor and 10 μF bypass capacitor are required for typical applications.

The general purpose low dropout regulators can be used to supply the lower power rails in the application. To improve the overall application standby current, the bias current of these regulators are made very low. The regulators have their own input supply pin to be able to connect them independently to either the system supply voltage or to the output of the DCDC converter in the application. The regulators are bypassed with a small size 2.2uF capacitor.

The feature can be controlled through the I^2C interface. In addition to this bus, digital control pins including hardware enable (HWEN), individual enable (ENx), power good (PG) and interrupt (INTB) are provided.

Two different enable versions are available:

- The 6924xH version offers one master enable pin (HWEN) with default power up sequence factory programmed (customizable upon request) and modifiable via I^2C.
- The 6924xE version ignores the HWEN pin. In this case pulling high one of the enable pins ENDCDCx or ENLDOx will enable the corresponding supply without initiating a power up sequence (this version does not require I^2C).

Under Voltage Lockout

The core does not operate for voltages below the Under Voltage Lock Out (UVLO) level. Below the UVLO threshold, all internal circuitry (both analog and digital) is held in reset.

NCP6924 operation is guaranteed down to UVLO when battery voltage is dropping off. To avoid erratic on / off behaviour, a maximum 200 mV hysteresis is implemented. Restart is guaranteed at 2.5 V when VBAT voltage is recovering or rising.

Thermal Shutdown

The thermal capabilities of the device can be exceeded due to the output power capabilities of the on chip step down converters and low drop out regulators. A thermal protection circuit is therefore implemented to prevent the part from being damaged. This protection circuit is only activated when the core is in active mode (at least one output channel is enabled). During thermal shutdown, all outputs of the NCP6924 are off.

When the NCP6924 returns from thermal shutdown mode, it can re−start in three different configurations depending on REARM[1:0] bits:

- If REARM[1:0] = 00, NCP6924 re−starts with default register values,
- If REARM[1:0] = 01 NCP6924 re−starts with register values set prior to thermal shutdown,
- Finally if REARM[1:0] = 10, NCP6924 does not re−start automatically, a toggle of HWEN or ENx pins is needed.

In addition, a thermal warning is implemented which can inform the processor through an interrupt (if not masked) that NCP6924 is close to its thermal shutdown so that preventive measurement can be taken by software.

Active Output Discharge

Active output discharge can be independently enabled / disabled by the appropriate settings in the DIS register (refer to the register definition section).

However to prevent any disturbances on the power−up sequence, a quick active output discharge is done during the start−up sequence for all output channels.

When the IC is turned off through HWEN pin (or ENx pins) or AVIN drops down below UVLO threshold, no shut down sequence is expected, all supplies are disabled and outputs discharged simultaneously if discharge enabled.

Enabling 6924xH Case (HWEN Version)

The HWEN pin controls the device start up. If HWEN is raised, this starts the power up sequencer. If HWEN is made low, device enters in shutdown mode and all regulators are turned off. A built−in pull−down resistor disables the device if this pin is left unconnected.

When HWEN is high, the different power rails can be independently enabled / disabled by writing the appropriate bit in the ENABLE register or by changing Enable pins (ENx) state (see Table 7).

Power Up Sequence and HWEN

When enabling the part with the HWEN pin, the part will start up in the configuration factory programmed in the registers. Any order and output voltage setting can be factory programmed upon request.

By default, the power up sequence is the following:

Table 5. DEFAULT POWER UP SEQUENCE FOR NCP6924AH

Delay (in ms)	Default Assignment	Default V_{prog}	Default Mode and ON/OFF
2	DCDC1	1.25 V	Auto mode ON
4	DCDC2	1.85 V	Auto mode ON
6	LDO1	2.8 V	ON
8	LDO2	1.8 V	ON
10	LDO3	2.8 V	ON
12	LDO4	1.8 V	ON

Table 6. DEFAULT POWER UP SEQUENCE FOR NCP6924BH AND NCP6924CH

Delay (in ms)	Default Assignment	Default V_{prog}	Default Mode and ON/OFF
2	DCDC1	1.2 V	Forced PWM OFF
4	DCDC2	1.8 V	Auto mode OFF
6	LDO1	2.9 V	OFF
8	LDO2	2.85 V	OFF
10	LDO3	1.8 V	OFF
10	LDO4	1.8 V	OFF

I^2C registers can be read and written while HWEN pin is still low. By programming the appropriate registers (see registers description section), the power up sequence can be modified.

Reset to the factory default configuration can be achieved either by hardware reset (all power supplies removed) or by writing through the I^2C in the RESET register.

Enable Control

Table 7. TRUTH TABLE OF ENABLE/DISABLE CONTROL 6924xH

HWEN Pin	ENDCDCx ENLDOx Pins	ENDCDCx ENLDOx Registers Bits	Outputx Enabled / Disabled
H	L	0	Disabled
H	L	1	Enabled
H	H	0	Enabled
H	H	1	Enabled
L	*	*	Disabled

NOTE: * means undefined

Shutdown

When shutting down the device, no shut down sequence is applied. All supplies are disabled and outputs are discharged simultaneously, and PG open drain output is low whereas INTB open drain is released. However, the power down sequence can be achieved by disabling DCDC/LDOs via I^2C and/or ENx pins before setting HWEN pin to low.

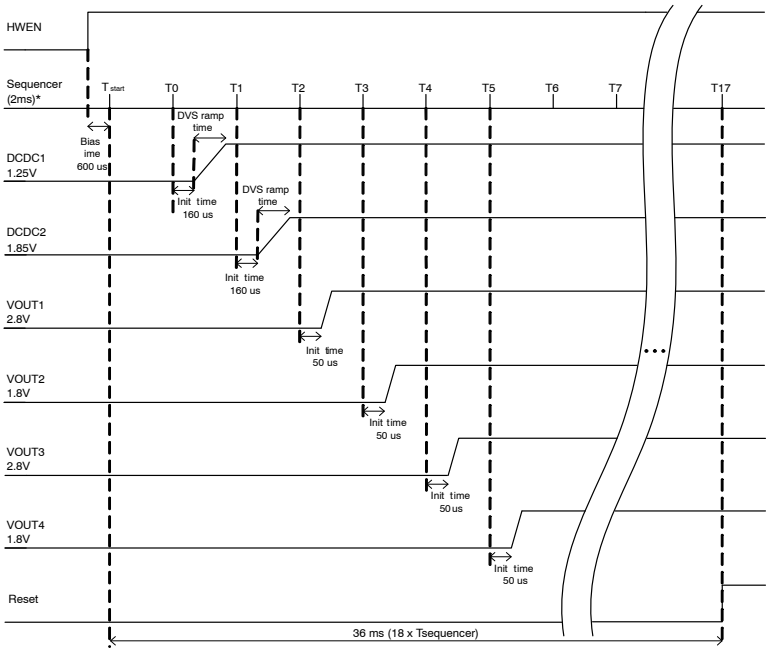


Figure 27. Default Power Up Sequence 6924AH

Enabling 6924xE Case (Enable Version)

The HWEN pin does not have any influence on the device, I^{2}C “enable” and “TAP” either. Device starts up as soon as one ENx rises. When the remaining ENx pin is made low, device enters in shutdown mode. A built−in pull−down resistor disables the device if ENx pins are left unconnected.

The different power rails can be independently enabled / disabled by using the corresponding ENx pin (see table 5).

Power Up Sequence

The power up sequence is managed by the processor with the ENx. The part will start up in the configuration factory programmed in the registers. Any output voltage setting can be factory programmed upon request.

By default, the power up is the following:

Table 8. DEFAULT POWER UP SEQUENCE 6924AE

Default Assignment	Default Vprog	Default Mode
DCDC1	1.25 V	Auto mode
DCDC2	1.85 V	Auto mode
LDO1	2.80 V	–
LDO2	1.80 V	–
LDO3	2.80 V	–
LDO4	1.80 V	–

I^{2}C registers can be read and written while ENx pins are low. By programming the appropriate registers (see registers description section), the power up can be modified.

Reset to the factory default configuration can be achieved either by hardware reset (all power supplies removed) or by writing through the I^{2}C in the RESET register.

Enable Control

Table 9. TRUTH TABLE OF ENABLE/DISABLE CONTROL 6924xE

HWEN Pin	ENDCDCx ENLDOx Pins	ENDCDCx ENLDOx Registers Bits	Outputx Enabled / Disabled
*	L	*	Disabled
*	H	*	Enabled

*means undefined

Shutdown

When shutting down the device, no shut down sequence is applied. All supplies are disabled and outputs are discharged simultaneously, and open drain outputs (PG and INTB) are low. However, the power down sequence can be achieved by disabling DCDC/LDOs via ENx pins.

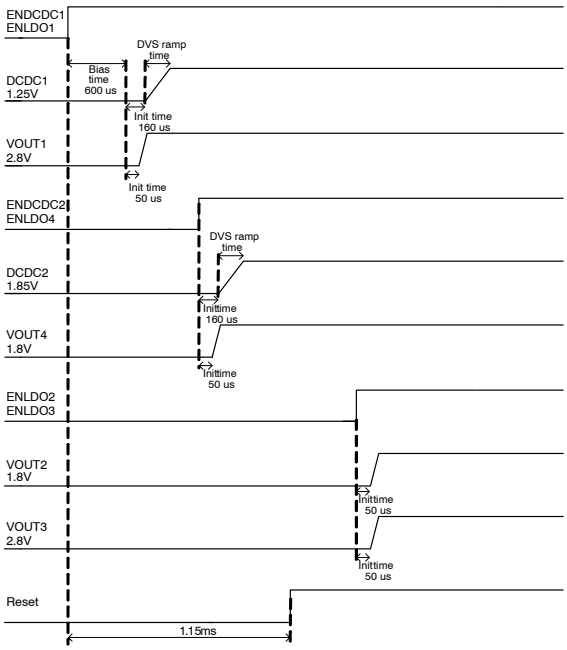


Figure 28. Default Power Up Sequence 6924AE

Dynamic Voltage Scaling (DVS)

The step down converters support dynamic voltage scaling (DVS). This means that the output voltage can be reprogrammed based upon the I^{2}C commands to provide the different voltages required by the processor. The change between set points is managed in a smooth manner without disturbing the operation of the processor.

When programming a higher voltage, the reference of the switcher and therefore the output is raised in equidistant steps per defined time period such that the dV/dt is controlled (by default 12.5 mV/1.33 μs). When programming a lower voltage the output voltage will decrease accordingly. The DVS step is fixed and the speed is programmable.

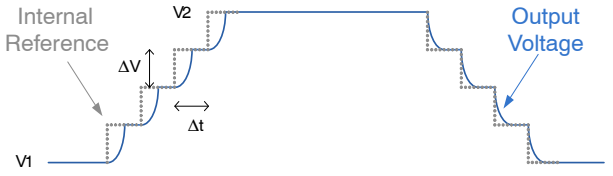


Figure 29. Default Dynamic Voltage Scaling Effect Timing Diagram

Programmability

DCDC converter output voltage can be controlled by GOx bit (TIME register) with VPROGDCDCx[7:0] and VDVSDCDCx[7:0] registers. Available output levels are listed in table VPROGDCDCx[7:0] and VDVSDCDCx[7:0] in register description.

GOx bit determines whether DCDC output voltage value is set in VPROGDCDCx[7:0] register or in VDVSDCDCx[7:0] register.

Table 10. GO BIT DESCRIPTION

GOx	Bit Description
0	Output voltage is set to VPROGDCDCx
1	Output voltage is set to VDVSDCDCx

The two DVS bits in the TIME register determine the ramp up time per each voltage step.

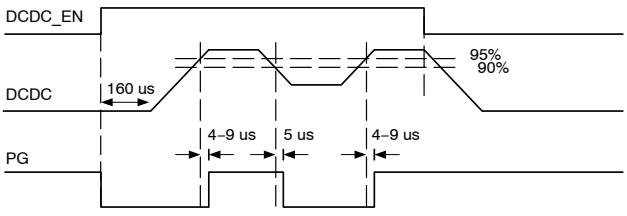


Figure 30. DCDC Channel Internal Power Good Signal

Table 11. DVS BITS DESCRIPTION

DVS [1:0]	Bit Description
00	1.33 μs per step (default)
01	2.67 μs per step
10	5.33 μs per step
11	10.67 μs per step

There are two ways of I^{2}C registers programming to switch the DCDC converters output voltages between different levels:

- Preset VPROGDCDCx[7:0] and VDVSDCDCx[7:0] registers, and start DVS sequence by changing GOx bit state.
- GOx bit remains unchanged, change output voltage value in either VPROGDCDCx[7:0] or VDVSDCDCx[7:0] register.

For example, the device needs to supply either 1.2 V or 0.9 V depending on working conditions. If using method 1, VPROGDCDCx[7:0] and VDVSDCDCx[7:0] should be set as shown in Table 8. GOx bit should be programmed to 1 to change DCDCx Output Voltage from 1.2 V to 0.9 V, and be programmed to 0 to move back from 0.9 V to 1.2 V.

Table 12. VPROGDCDC / VDVSDCDC SETTINGS FOR VDCDC SWITCHING BETWEEN 1.2 V AND 0.9 V

Register Name	Values	Target VDCDC (V)
VPROGDCDC	0$30	1.2
VDVSDCDC	0$18	0.9

DCDC Step Down Converter and LDO's Power Good

To indicate that the output of an output channel is established, a power good signal is available for each output channel.

The power good signal is high when the channel is off and goes low when enabling the channel. Once the output voltage reaches the expected output level, the power good signal becomes high again.

When during operation the output gets below 90% of the expected level, the power good signal goes low which indicates a power failure. When the voltage rises again above 95% the power good signal goes high again.

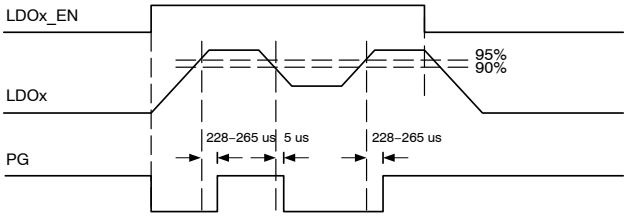


Figure 31. LDOx Channel Internal Power Good Signal

POWER GOOD ASSIGNMENT

Each channel generates an internal Power Good signal (either DCDC's or LDO's). These internal power good signals can be individually assigned to the PG pin through the PGOOD1 and PGOOD2 registers. The PG pin state is an AND combination of assigned internal power good signals.

By default only the power good signal of the DCDC's converter is assigned. The PG pin is an open drain output. In addition, two other signals can be assigned to the PG pin: the internal reset signal through the PGOOD1 register and the DVS signal through the PGOOD2 register. By assigning the internal reset signal, the PG pin is held low throughout the power up sequence and the reset period. By assigning the DVS signal of the DCDC's converter, the PG pin is made low during the period the output voltage is being raised to the new setting as shown in Figure 32.

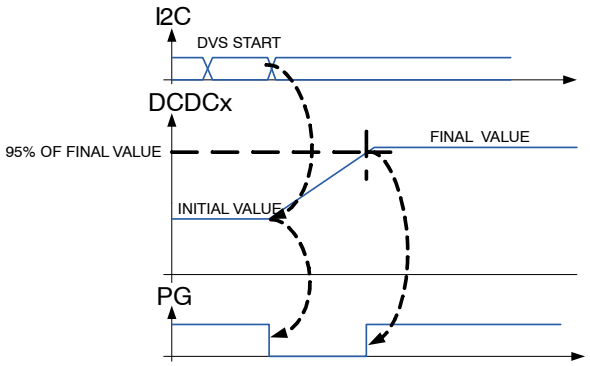


Figure 32. PG Operation in DVS Sequence

POWER GOOD DELAY

A delay can be programmed between the moment the AND result of the assigned internal power good signals becomes high and the moment the PG pin is released. The delay is set from 0 ms to 512 ms through the TOR[2:0] bits in the TIME register.

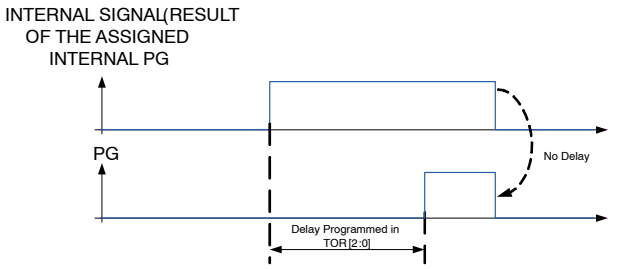


Figure 33. PG Delay

Interrupt

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring). The interrupt sources include:

Table 13. INTERRUPT SOURCES

Interrupt Sources	Description
PG_DCDC1	DCDC1 Converter Power Good
PG_DCDC2	DCDC2 Converter Power Good
PG_LDO1	LDO1 Power Good
PG_LDO2	LDO2 Power Good
PG_LDO3	LDO3 Power Good
PG_LDO4	LDO4 Power Good
UVLO	UVLO state
ILDO1	LDO1 Output Over Current
ILDO2	LDO2 Output Over Current
ILDO3	LDO3 Output Over Current
ILDO4	LDO4 Output Over Current
WNRG	Thermal Warning
TSD	Thermal Shutdown

Individual bits generating interrupts will be set to 1 in the INT_ACK1/INT_ACK2 registers (I^2C read only registers), indicating the interrupt source. INT_ACK1/INT_ACK2 registers are automatically reset by an I^2C read. INT_SEN1/INT_SEN2 registers (read only registers) contain real time indicators of interrupt sources.

All interrupt sources can be masked by writing registers INT_MSK1/INT_MSK2. Masked sources will never generate an interrupt request on INTB pin.

The INTB pin is an open drain output. A non masked interrupt request will result in the INTB pin being driven low.

When the host reads the INT_ACK1/INT_ACK2 registers the INTB pin is released to high impedance and the interrupt registers INT_ACK1/INT_ACK2 are cleared.

Below figure shows how DCDC1 converter power good produces interrupt on INTB pin with INT_SEN1/INT_MSK1/INT_ACK1 and an I^2C read access (assuming no other interrupt happens during this read period).

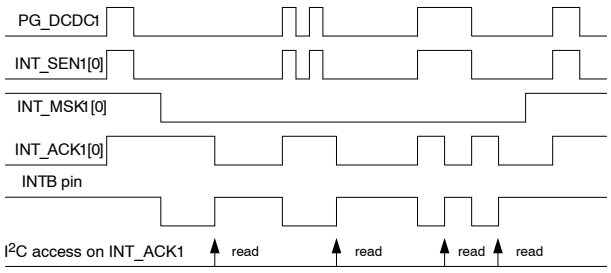


Figure 34. Interrupt Timing Chart Example of PG_DCDC1

INT_MSK1 and INT_MSK2 registers are set to disable INTB feature by default during power−up.

Force Reset and I²C Interface Disable

The I²C interface can be disabled by the I2C_DISABLE bit in the SYNC register. This saves current consumption which is especially of interest when all supply channels of the NCP6924 are disabled. To re−activate the I²C, the IC needs to be enabled through the HWEN pin.

The I²C registers can be reset by setting the FORCERST bit in register RESET. It forces a restart of the device with its default settings. After startup the RSTSTATUS bit defaults to 1 and can be cleared through I²C.

DCDC Step Down Converters

The DCDC converters are synchronous rectifier type with both high side and low side integrated switches. Neither external transistor nor diodes are required for proper operation. Feedback and compensation network are also fully integrated.

The DCDC converters can operate in two different modes: PWM and PFM. The transition between PWM/PFM modes can occur automatically or the switcher can be placed in forced PWM mode by I²C programming. (MODEDCDC1 and MODEDCDC2 bits of ENABLE register)

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, DCDC converters operates in PWM mode from a fixed 3 MHz clock and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM. The internal N−MOS switch operates as synchronous rectifier and is driven complementary to the P−MOS switch. In CCM the lower (N−MOS switch) in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads the DCDC converters operate in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The upper FET on time is kept constant and the switching frequency is variable. Output voltage is regulated by varying the switching frequency which becomes proportional to loading current. As it does in PWM mode, the internal N−MOSFET operates as synchronous rectifier after each P−MOSFET on−pulse with very small negative current limit. When load increases and current in inductor becomes continuous again, the controller automatically turns back to PWM fixed frequency mode.

Forced PWM

The DCDC converters can be programmed to only use PWM and disable the transition to PFM if so desired.

Table 14. MODEDCDC1&2 BIT DESCRIPTION

MODEDCDC1&2	Bit Description
0	Auto switching PFM / PWM
1	Forced PWM

Inductor Peak Current Limitation

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrains inductor power

Soft Start

A soft start is provided to limit inrush currents when enabling the converter. After enabling and internal delays elapsed, the DC to DC converter output will gradually ramp up to the programmed voltage.

I²C Compatible Interface

NCP6924 can support a subset of I²C protocol, below are detailed introduction for I²C programming.

I²C Communication Description

ON Semiconductor communication protocol is a subset of I²C protocol.

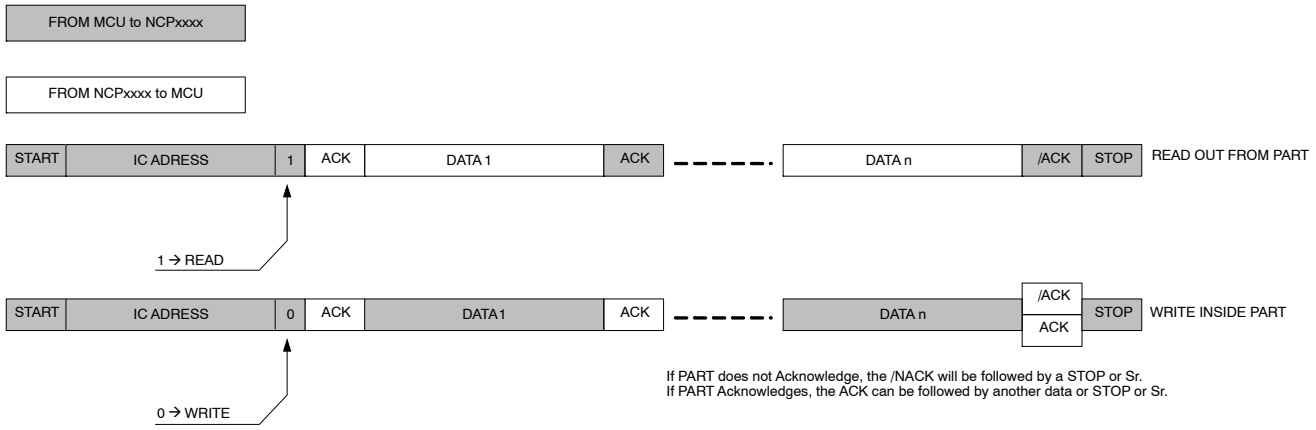


Figure 35. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) we want to write in followed by the data we will write in the chip. The writing process is incremental. So the first data will be written in @REG, the second one in @REG + 1 .... The data are optional.
- In case of read operation, the NCP6924 will output the data out from the last register that has been accessed by the last write operation. Like writing process, reading process is an incremental process.

Read Out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has set:

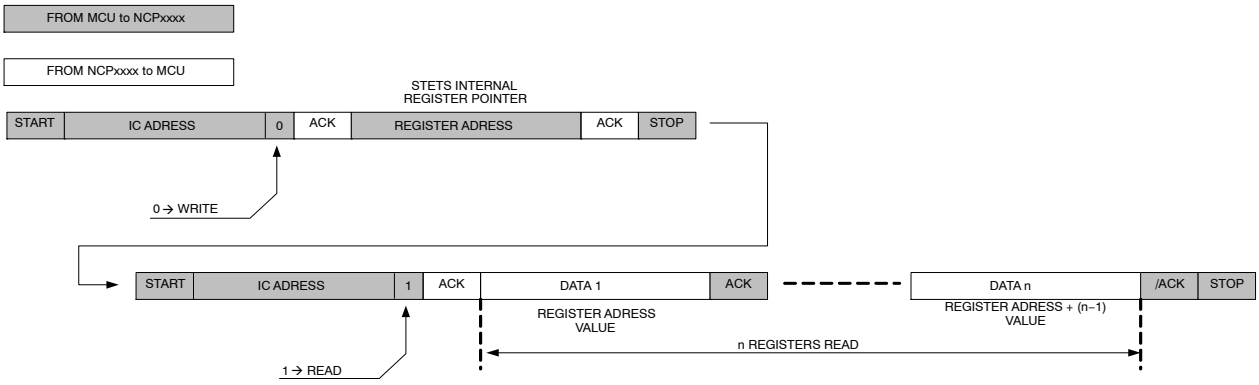


Figure 36. Read Out from Part

The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read:

With Stop Then Start

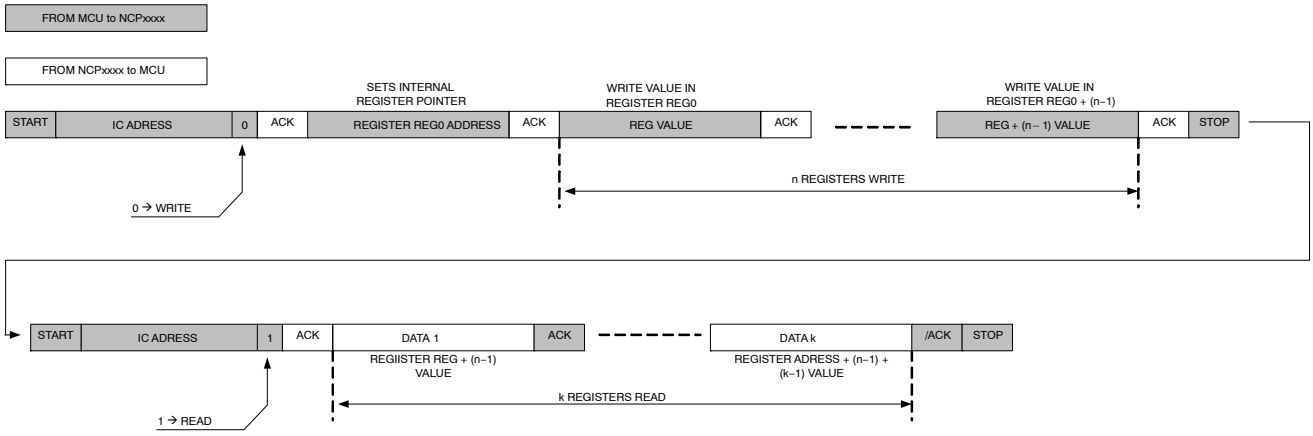


Figure 37. Write Followed by Read Transaction

Write in Part:

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, ..., Reg +n.

Write n Registers:

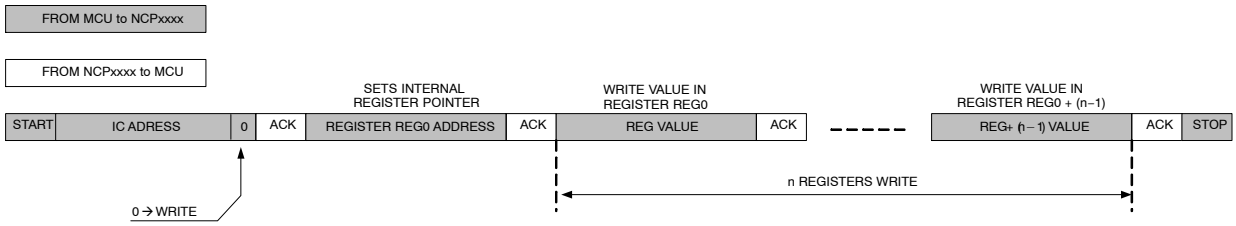


Figure 38. Write in n Registers

I²C Address

NCP6924 has fixed I²C but different I²C address (0$10, 7 bit address, see below table A7~A1), NCP6924 supports 7−bit address only.

Table 15. NCP6924 I²C ADDRESS

I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
Default, others	$20 / $21	0	0	1	0	0	0	0	X

Other addresses are available upon request.

Register Map

Following register map describes I^2C registers.

Registers can be:

R	Read only register
RC	Read then Clear
RW	Read and Write register
RWM	Read, Write and can be Modified by the IC
Reserved	Address is reserved and register is not physically designed
Spare	Address is reserved and register is physically designed

Address	Register Name	Type	Default	Function
$00	INT_ACK1	RC	$00	Interrupt 1 Register (dual edge)
$01	INT_ACK2	RC	$00	Interrupt 2 Register (rising edge and dual edge)
$02	INT_SEN1	R	$00	Sense 1 Register (real time status)
$03	INT_SEN2	R	$00	Sense 2 Register (real time status)
$04	INT_MSK1	RW	$FF	Mask 1 Register to Enable or Disable Interrupt Sources
$05	INT_MSK2	RW	$FF	Mask 2 Register to Enable or Disable Interrupt Sources
$06 to $0F	–	–	–	Reserved for future use
$10	RESET	RW	$10	Reset Internal Registers to Default
$11	PID	R	Metal	Product Identification (metal)
$12	RID	R	Metal	Revision Identification (metal)
$13	FID	R	fuse	Features Identification (fuse)
$14	ENABLE	RWM	fuse ($FA)	Enable Register (fuse)
$15	DIS	RW	fuse ($3F)	Active Output Discharge Register (fuse)
$16	PGOOD1	RW	$43	Power Good Pin Assignment 1
$17	PGOOD2	RW	$00	Power Good Pin Assignment 2
$18	TIME	RW	$00	Timing Definition
$19	BUCKTAP	RW	fuse ($08)	buck sequencer register (fuse)
$1A	LDOTAP1	RW	fuse ($1A)	LDO1 and LDO2 sequencer register (fuse)
$1B	LDOTAP2	RW	fuse ($2C)	LDO3 and LDO4 sequencer register (fuse)
$1C to $1F	–	–	–	Reserved for future use
$20	VPROGDCDC1	RW	fuse ($34)	DCDC1 Output Voltage Setting
$21	VPROGDVS1	RW	fuse ($34)	DCDC1 DVS Output Voltage Setting
$22	VPROGDCDC2	RW	fuse ($64)	DCDC2 Output Voltage Setting
$23	VPROGDVS2	RW	fuse ($64)	DCDC2 DVS Output Voltage Setting
$24	VPROGLDO1	RW	fuse ($24)	LDO1 Output Voltage Setting
$25	VPROGLDO2	RW	fuse ($10)	LDO2 Output Voltage Setting
$26	VPROGLDO3	RW	fuse ($24)	LDO3 Output Voltage Setting
$27	VPROGLDO4	RW	fuse ($10)	LDO4 Output Voltage Setting
$28 to $3F	–	–	–	Reserved for future use

Registers Description

Table 16. INT_ACK1 REGISTER

Name: INT_ACK1				Address: $00			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	ACK_UVLO	ACK_PG_LDO4	ACK_PG_LDO3	ACK_PG_LDO2	ACK_PG_LDO1	ACK_PG_DCDC2	ACK_PG_DCDC1

Table 17. BIT DESCRIPTION OF INT_ACK1 REGISTER

Bit	Bit Description
ACK_PG_DCDC1	DCDC1 Power Good Sense Acknowledgement 0: Cleared 1: DCDC1 Power Good Event detected
ACK_PG_DCDC2	DCDC2 Power Good Sense Acknowledgement 0: Cleared 1: DCDC2 Power Good Event detected
ACK_PG_LDO1	LDO1 Power Good Sense Acknowledgement 0: Cleared 1: LDO1 Power Good Event detected
ACK_PG_LDO2	LDO2 Power Good Sense Acknowledgement 0: Cleared 1: LDO2 Power Good Event detected
ACK_PG_LDO3	LDO3 Power Good Sense Acknowledgement 0: Cleared 1: LDO3 Power Good Event detected
ACK_PG_LDO4	LDO4 Power Good Sense Acknowledgement 0: Cleared 1: LDO4 Power Good Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected

Table 18. INT_ACK2 REGISTER

Name: INT_ACK2				Address: $01			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ACK_TSD	ACK_WNRG	ACK_ILDO4	ACK_ILDO3	ACK_ILDO2	ACK_ILDO1	spare = 0	spare = 0

Table 19. BIT DESCRIPTION OF INT_ACK2 REGISTER

Bit	Bit Description
ACK_ILDO1	LDO1 Over Current Sense Acknowledgement 0: Cleared 1: LDO1 Over Current Event detected
ACK_ILDO2	LDO2 Over Current Sense Acknowledgement 0: Cleared 1: LDO2 Over Current Event detected
ACK_ILDO3	LDO3 Over Current Sense Acknowledgement 0: Cleared 1: LDO3 Over Current Event detected
ACK_ILDO4	LDO4 Over Current Sense Acknowledgement 0: Cleared 1: LDO4 Over Current Event detected
ACK_WNRG	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 20. INT_SEN1 REGISTER

Name: INT_SEN1				**Address: $02**			
Type: R				**Default: $00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	SEN_UVLO	SEN_PG_LDO4	SEN_PG_LDO3	SEN_PG_LDO2	SEN_PG_LDO1	SEN_PG_DCDC2	SEN_PG_DCDC1

Table 21. BIT DESCRIPTION OF INT_SEN1 REGISTER

Bit	Bit Description
SEN_PG_DCDC1	DCDC1 Power Good Sense 0: DCDC1 Output Voltage below target 1: DCDC1 Output Voltage within nominal range
SEN_PG_DCDC2	DCDC2 Power Good Sense 0: DCDC2 Output Voltage below target 1: DCDC2 Output Voltage within nominal range
SEN _PG_LDO1	LDO1 Power Good Sense 0: LDO1 Output Voltage below target 1: LDO1 Output Voltage within nominal range
SEN _PG_LDO2	LDO2 Power Good Sense 0: LDO2 Output Voltage below target 1: LDO2 Output Voltage within nominal range
SEN _PG_LDO3	LDO3 Power Good Sense 0: LDO3 Output Voltage below target 1: LDO3 Output Voltage within nominal range
SEN _PG_LDO4	LDO4 Power Good Sense 0: LDO4 Output Voltage below target 1: LDO4 Output Voltage within nominal range
SEN _UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold

Table 22. INT_SEN2 Register

Name: INT_SEN2				Address: $03			
Type: R				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
SEN_TSD	SEN_WNRG	SEN_ILDO4	SEN_ILDO3	SEN_ILDO2	SEN_ILDO1	spare = 0	spare = 0

Table 23. BIT DESCRIPTION OF INT_SEN2 REGISTER

Bit	Bit Description
	1: DCDC2 Output Current over limit
SEN _ILDO1	LDO1 Over Current Sense 0: LDO1 Output Current below limit 1: LDO1 Output Current over limit
SEN _ILDO2	LDO2 Over Current Sense 0: LDO2 Output Current below limit 1: LDO2 Output Current over limit
SEN _ILDO3	LDO3 Over Current Sense 0: LDO3 Output Current below limit 1: LDO3 Output Current over limit
SEN _ILDO4	LDO4 Over Current Sense 0: LDO4 Output Current below limit 1: LDO4 Output Current over limit
SEN _WNRG	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN _TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 24. INT_MSK1 REGISTER

Name: INT_MSK1				Address: $04			
Type: RW				Default: $FF			
D7	D6	D5	D4	D3	D2	D1	D0
spare=0	MSK_UVLO	MSK_PG_LDO4	MSK_PG_LDO3	MSK_PG_LDO2	MSK_PG_LDO1	MSK_PG_DCDC2	MSK_PG_DCDC1

Table 25. BIT DESCRIPTION OF INT_MSK1 REGISTER

Bit	Bit Description
MSK _PG_DCDC1	DCDC1 Power Good Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _PG_DCDC2	DCDC2 Power Good Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _PG_LDO1	LDO1 Power Good Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _PG_LDO2	LDO2 Power Good Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _PG_LDO3	LDO3 Power Good Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 25. BIT DESCRIPTION OF INT_MSK1 REGISTER

Bit	Bit Description
MSK _PG_LDO4	LDO4 Power Good Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _UVLO	UVLO Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 26. INT_MSK2 REGISTER

Name: INT_MSK2				**Address: $05**			
Type: RW				**Default: $FF**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MSK_TSD	MSK_WNRG	MSK_ILDO4	MSK_ILDO3	MSK_ILDO2	MSK_ILDO1	spare = 1	spare = 1

Table 27. BIT DESCRIPTION OF INT_MSK2 REGISTER

Bit	Bit Description
MSK _ILDO1	LDO1 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _ILDO2	LDO2 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _ILDO3	LDO3 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _ILDO4	LDO4 Over Current Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _WNRG	Thermal Warning Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK _TSD	Thermal Shutdown Interrupt Source Mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 28. RESET REGISTER

Name: RESET				**Address: $10**			
Type: RW				**Default: $10**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
FORCERST	spare=0	spare=0	RSTSTATUS	spare=0	spare=0	REARM	

Table 29. BIT DESCRIPTION OF RESET REGISTER

Bit	Bit Description
REARM[1:0]	Rearming of device after TSD 00: Re−arming active after TSD with reset of I²C registers: new power−up sequence is initiated with default I²C registers values (default) 01: Re−arming active after TSD with no reset of I²C registers: new power−up sequence is initiated with I²C registers values 10: No re−arming after TSD 11: N/A
RSTSTATUS	Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset)
FORCERST	Force Reset Bit 0: Default 1: Force reset of internal registers to default

Table 30. PID (PRODUCT IDENTIFICATION) REGISTER

Name: PID				**Address: $11**			
Type: R				**Default:**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
pid7	pid6	pid5	pid4	pid3	pid2	pid1	pid0

Table 31. RID: (REVISION IDENTIFICATION) REGISTER

Name: RID				**Address: $12**			
Type: R				**Default:**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
rid7	rid6	rid5	rid4	rid3	rid2	rid1	rid0

Table 32. FID (FEATURES IDENTIFICATION) REGISTER

Name: FID				**Address: $13**			
Type: R				**Default:**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
fid7	fid6	fid5	fid4	fid3	fid2	fid1	fid0

Table 33. ENABLE REGISTER

Name: ENABLE				**Address: $14**			
Type: RWM				**Default: $FA**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ENLDO4	ENLDO3	ENLDO2	ENLDO1	ENDCDC2	MODEDCDC2	ENDCDC1	MODEDCDC1

Table 34. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
MODEDCDC1	DCDC1 Operating Mode 0: Auto switching PFM / PWM 1: Forced PWM (default)
ENDCDC1	DCDC1 Enabling 0: Disabled 1: Enabled

Table 34. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
MODEDCDC2	DCDC2 Operating Mode 0: Auto switching PFM / PWM 1: Forced PWM (default)
ENDCDC2	DCDC2 Enabling 0: Disabled 1: Enabled
ENLDO1	LDO1 Enabling 0: Disabled 1: Enabled
ENLDO2	LDO2 Enabling 0: Disabled 1: Enabled
ENLDO3	LDO3 Enabling 0: Disabled 1: Enabled
ENLDO4	LDO4 Enabling 0: Disabled 1: Enabled

Table 35. DIS REGISTER

Name: DIS				**Address: $15**			
Type: RW				**Default: $3F**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	DISLDO4	DISLDO3	DISLDO2	DISLDO1	DISDCDC2	DISDCDC1

Table 36. BIT DESCRIPTION OF DIS REGISTER

Bit	Bit Description
DISDCDC1	DCDC1 Active Output Discharge 0: Disabled 1: Enabled
DISDCDC2	DCDC2 Active Output Discharge 0: Disabled 1: Enabled
DISLDO1	LDO1 Active Output Discharge 0: Disabled 1: Enabled
DISLDO2	LDO2 Active Output Discharge 0: Disabled 1: Enabled
DISLDO3	LDO3 Active Output Discharge 0: Disabled 1: Enabled
DISLDO4	LDO4 Active Output Discharge 0: Disabled 1: Enabled

Table 37. PGOOD1 REGISTER

Name: PGOOD1				**Address: $16**			
Type: RW				**Default: $43**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
I2C_DISABLE	PGASSIGN_RST	PGASSIGN_LDO4	PGASSIGN_LDO3	PGASSIGN_LDO2	PGASSIGN_LDO1	PGASSIGN_DCDC2	PGASSIGN_DCDC1

Table 38. BIT DESCRIPTION OF PGOOD1 REGISTER

Bit	Bit Description
PGASSIGN_DCDC1	DCDC1 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_DCDC2	DCDC2 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO1	LDO1 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO2	LDO2 Power Good Assignment 0: Not assigned 1: Assigned to PG
PGASSIGN_LDO3	LDO3 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO4	LDO4 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_RST	Internal Reset Signal Assignment 0: Not assigned 1: Assigned to PG pin
I2C_DISABLE	I^2C Interface Enabling 0: Enabled 1: Disabled

Table 39. PGOOD2 REGISTER

Name: PGOOD2				**Address: $17**			
Type: RW				**Default: $00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	PGASSIGN_DVS2	PGASSIGN_DVS1	spare=0	spare=0	spare=0	spare=0

Table 40. BIT DESCRIPTION OF PGOOD2 REGISTER

Bit	Bit Description
PGASSIGN_DVS1	DCDC1 DVS Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_DVS2	DCDC2 DVS Assignment 0: Not assigned 1: Assigned to PG pin

Table 41. TIME REGISTER

Name: TIME				**Address: $38**			
Type: RW				**Default: 0$00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
GO2	GO1	spare=0	DVS[1:0]		TOR[2:0]		

Table 42. BIT DESCRIPTION OF TIME REGISTER

Bit	Bit Description
TOR[2:0]	Power Good Out of Reset Delay Time (ms) 000: 0(default) 001: 8 010: 16 011: 32 100: 64 101: 128 110: 256 111: 512
DVS[1:0]	DVS Timing (μs) 00: 1.33 μs (default) 01: 2.67 μs 10: 5.33 μs 11: 10.67 μs
GO1	0: DCDC1 Output Voltage set to VPROGDCDC1[7:0] 1: DCDC1 Output Voltage set to VDVSDCDC1[7:0]
GO2	0: DCDC2 Output Voltage set to VPROGDCDC2[7:0] 1: DCDC2 Output Voltage set to VDVSDCDC2[7:0]

Table 43. BUCKTAP REGISTER

Name: BUCKTAP				**Address: $19**			
Type: RW				**Default: $08**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	DCDC2_T[2:0]			DCDC1_T[2:0]		

Table 44. LDOTAP1 REGISTER

Name: LDOTAP1				**Address: $1A**			
Type: RW				**Default: $1A**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	LDO2_T[2:0]			LDO1_T[2:0]		

Table 45. LDOTAP2 REGISTER

Name: LDOTAP2				**Address: $1B**			
Type: RW				**Default: $2C**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	LDO4_T[2:0]			LDO3_T[2:0]		

Table 46. START−UP DELAY

LDOx_T[2:0] / DCDCx_T[2:0]	Start−up Delay
000	2 ms
001	4 ms
010	6 ms
011	8 ms
100	10 ms
101	12 ms
110	14 ms
111	16 ms

Table 47. VPROGDCDC1[7:0] REGISTER

Name: VPROGDCDC1				Address: $20			
Type: RW				Default: $34			
D7	D6	D5	D4	D3	D2	D1	D0
VPROGDCDC1[7:0]							

Table 48. VDVSDCDC1[7:0] REGISTER

Name: VDVSDCDC1				Address: $21			
Type: RW				Default: $34			
D7	D6	D5	D4	D3	D2	D1	D0
VDVSDCDC1[7:0]							

Table 49. VPROGDCDC2[7:0] REGISTER

Name: VPROGDCDC2				Address: $22			
Type: RW				Default: $64			
D7	D6	D5	D4	D3	D2	D1	D0
VPROGDCDC2[7:0]							

Table 50. VDVSDCDC2[7:0] REGISTER

Name: VDVSDCDC2				Address: $23			
Type: RW				Default: $64			
D7	D6	D5	D4	D3	D2	D1	D0
VDVSDCDC2[7:0]							

Table 51. VPROGDCDCx[7:0] AND VDVSDCDCx[7:0] BITS DESCRIPTION

Bit[7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)
$00	0.6000	$40	1.4000	$80	2.2000	$C0	3.0000
$01	0.6125	$41	1.4125	$81	2.2125	$C1	3.0125
$02	0.6250	$42	1.4250	$82	2.2250	$C2	3.0250
$03	0.6375	$43	1.4375	$83	2.2375	$C3	3.0375
$04	0.6500	$44	1.4500	$84	2.2500	$C4	3.0500
$05	0.6625	$45	1.4625	$85	2.2625	$C5	3.0625
$06	0.6750	$46	1.4750	$86	2.2750	$C6	3.0750
$07	0.6875	$47	1.4875	$87	2.2875	$C7	3.0875
$08	0.7000	$48	1.5000	$88	2.3000	$C8	3.1000
$09	0.7125	$49	1.5125	$89	2.3125	$C9	3.1125
$0A	0.7250	$4A	1.5250	$8A	2.3250	$CA	3.1250
$0B	0.7375	$4B	1.5375	$8B	2.3375	$CB	3.1375
$0C	0.7500	$4C	1.5500	$8C	2.3500	$CC	3.1500
$0D	0.7625	$4D	1.5625	$8D	2.3625	$CD	3.1625
$0E	0.7750	$4E	1.5750	$8E	2.3750	$CE	3.1750
$0F	0.7875	$4F	1.5875	$8F	2.3875	$CF	3.1875
$10	0.8000	$50	1.6000	$90	2.4000	$D0	3.2000
$11	0.8125	$51	1.6125	$91	2.4125	$D1	3.2125

Table 51. VPROGDCDCx[7:0] AND VDVSDCDCx[7:0] BITS DESCRIPTION

Bit[7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)
$12	0.8250	$52	1.6250	$92	2.4250	$D2	3.2250
$13	0.8375	$53	1.6375	$93	2.4375	$D3	3.2375
$14	0.8500	$54	1.6500	$94	2.4500	$D4	3.2500
$15	0.8625	$55	1.6625	$95	2.4625	$D5	3.2625
$16	0.8750	$56	1.6750	$96	2.4750	$D6	3.2750
$17	0.8875	$57	1.6875	$97	2.4875	$D7	3.2875
$18	0.9000	$58	1.7000	$98	2.5000	$D8	3.3000
$19	0.9125	$59	1.7125	$99	2.5125	$D9	3.3000
$1A	0.9250	$5A	1.7250	$9A	2.5250	$DA	3.3000
$1B	0.9375	$5B	1.7375	$9B	2.5375	$DB	3.3000
$1C	0.9500	$5C	1.7500	$9C	2.5500	$DC	3.3000
$1D	0.9625	$5D	2.4525	$9D	2.5625	$DD	3.3000
$1E	0.9750	$5E	1.7750	$9E	2.5750	$DE	3.3000
$1F	0.9875	$5F	1.7875	$9F	2.5875	$DF	3.3000
$20	1.0000	$60	1.8000	$A0	2.6000	$E0	3.3000
$21	1.0125	$61	1.8125	$A1	2.6125	$E1	3.3000
$22	1.0250	$62	1.8250	$A2	2.6250	$E2	3.3000
$23	1.0375	$63	1.8375	$A3	2.6375	$E3	3.3000
$24	1.0500	$64	1.8500	$A4	2.6500	$E4	3.3000
$25	1.0625	$65	1.8625	$A5	2.6625	$E5	3.3000
$26	1.0750	$66	1.8750	$A6	2.6750	$E6	3.3000
$27	1.0875	$67	1.8875	$A7	2.6875	$E7	3.3000
$28	1.1000	$68	1.9000	$A8	2.7000	$E8	3.3000
$29	1.1125	$69	1.9125	$A9	2.7125	$E9	3.3000
$2A	1.1250	$6A	1.9250	$AA	2.7250	$EA	3.3000
$2B	1.1375	$6B	1.9375	$AB	2.7375	$EB	3.3000
$2C	1.1500	$6C	1.9500	$AC	2.7500	$EC	3.3000
$2D	1.1625	$6D	1.9625	$AD	2.7625	$ED	3.3000
$2E	1.1750	$6E	1.9750	$AE	2.7750	$EE	3.3000
$2F	1.1875	$6F	1.9875	$AF	2.7875	$EF	3.3000
$30	1.2000	$70	2.0000	$B0	2.8000	$F0	3.3000
$31	1.2125	$71	2.0125	$B1	2.8125	$F1	3.3000
$32	1.2250	$72	2.0250	$B2	2.8250	$F2	3.3000
$33	1.2375	$73	2.0375	$B3	2.8375	$F3	3.3000
$34	1.2500	$74	2.0500	$B4	2.8500	$F4	3.3000
$35	1.2625	$75	2.0625	$B5	2.8625	$F5	3.3000
$36	1.2750	$76	2.0750	$B6	2.8750	$F6	3.3000
$37	1.2875	$77	2.0875	$B7	2.8875	$F7	3.3000
$38	1.3000	$78	2.1000	$B8	2.9000	$F8	3.3000
$39	1.3125	$79	2.1125	$B9	2.9125	$F9	3.3000
$3A	1.3250	$7A	2.1250	$BA	2.9250	$FA	3.3000
$3B	1.3375	$7B	2.1375	$BB	2.9375	$FB	3.3000

Table 51. VPROGDCDCx[7:0] AND VDVSDCDCx[7:0] BITS DESCRIPTION

Bit[7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)	Bit [7:0]	V_{OUT} (V)
$3C	1.3500	$7C	2.1500	$BC	2.9500	$FC	3.3000
$3D	1.3625	$7D	2.1625	$BD	2.9625	$FD	3.3000
$3E	1.3750	$7E	2.1750	$BE	2.9750	$FE	3.3000
$3F	1.3875	$7F	2.1875	$BF	2.9875	$FF	3.3000

Table 52. VPROGLDO1[5:0] REGISTERS

Name: VPROGLDO1				**Address: $24**			
Type: RW				**Default: $24**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	VPROGLDO1[5:0]					

Table 53. VPROGLDO2[5:0] REGISTERS

Name: VPROGLDO2				**Address: $25**			
Type: RW				**Default: $10**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	VPROGLDO2[5:0]					

Table 54. VPROGLDO3[5:0] REGISTERS

Name: VPROGLDO3				**Address: $26**			
Type: RW				**Default: $24**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	VPROGLDO3[5:0]					

Table 55. VPROGLDO4[5:0] REGISTERS

Name: VPROGLDO4				**Address: $27**			
Type: RW				**Default: $10**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	VPROGLDO4[5:0]					

Table 56. VPROGLDOx[5:0] BITS DESCRIPTION

VPROGLDOx [5:0]	V_{OUT} (V)	VPROGLDOx [5:0]	V_{OUT} (V)	VPROGLDOx [5:0]	V_{OUT}(V)	VPROGLDOx [5:0]	V_{OUT} (V)
000000	1.00	010000	1.80	100000	2.60	110000	3.30
000001	1.05	010001	1.85	100001	2.65	110001	3.30
000010	1.10	010010	1.90	100010	2.70	110010	3.30
000011	1.15	010011	1.95	100011	2.75	110011	3.30
000100	1.20	010100	2.00	100100	2.80	110100	3.30
000101	1.25	010101	2.05	100101	2.85	110101	3.30
000110	1.30	010110	2.10	100110	2.90	110110	3.30
000111	1.35	010111	2.15	100111	2.95	110111	3.30
001000	1.40	011000	2.20	101000	3.00	111000	3.30
001001	1.45	011001	2.25	101001	3.05	111001	3.30

Table 56. VPROGLDOx[5:0] BITS DESCRIPTION

VPROGLDOx [5:0]	V_{OUT} (V)	VPROGLDOx [5:0]	V_{OUT} (V)	VPROGLDOx [5:0]	V_{OUT}(V)	VPROGLDOx [5:0]	V_{OUT} (V)
001010	1.50	011010	2.30	101010	3.10	111010	3.30
001011	1.55	011011	2.35	101011	3.15	111011	3.30
001100	1.60	011100	2.40	101100	3.20	111100	3.30
001101	1.65	011101	2.45	101101	3.25	111101	3.30
001110	1.70	011110	2.50	101110	3.30	111110	3.30
001111	1.75	011111	2.55	101111	3.30	111111	3.30

APPLICATION INFORMATION

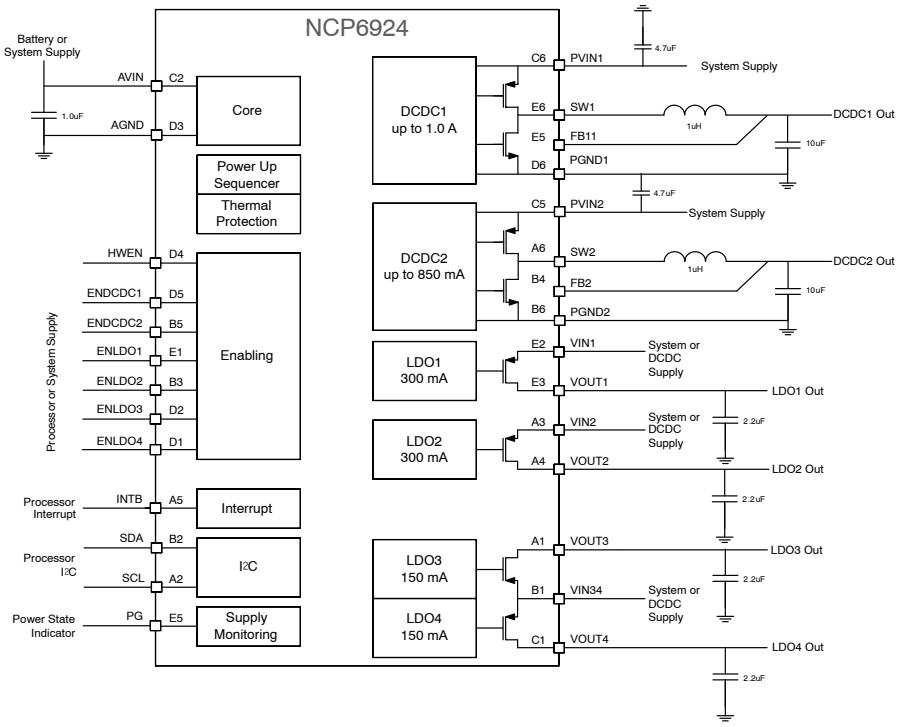


Figure 39. Typical Application Schematic

Inductor selection

NCP6924 DCDC converters typically use 1 μH inductor. Use of different values can be considered to optimize operation in specific conditions. The inductor parameters directly related to device performances are saturation current, DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \quad \text{(eq. 1)}$$

$$I_{LMAX} = I_{OMAX} + \frac{\Delta I_L}{2} \quad \text{(eq. 2)}$$

With:

- Fsw = Switching Frequency (Typical 3 MHz)
- L = Inductor value
- ΔI_L = Peak−To−Peak inductor ripple current
- I_{LMAX} = Maximum Inductor Current

To achieve better efficiency, ultra low DC resistance inductor should be selected.

The saturation current of the inductor should be higher than the I_{LMAX} calculated with the above equations.

Table 57. INDUCTOR L = 1.0 μH

Supplier	Part #	Size (mm) (L x l x T)	DC Rated Current (A)	DCR Max at 25°C (mΩ)
TDK	TFM252010A−1R0M	2.5 x 2.0 x 1.0	3.5	65
TDK	TFM201610A−1R0M	2.0 x 1.6 x 1.0	2.5	75
MURATA	LQH44PN−1R0NP0	4.0 x 3.5 x 1.8	2.5	36
MURATA	LQM2HPN−1R0MG0	2.5 x 2.0 x 1.0	1.6	69
TOKO	DFE252012C−1R0N	2.5 x 2.0 x 1.2	3.0	59

Table 58. INDUCTOR L = 2.2 μH

Supplier	Part #	Size (mm) (L x l x T)	DC Rated Current (A)	DCR Max at 25°C (mΩ)
TDK	TFM252010A−2R2M	2.5 x 2.0 x 1.0	2.3	115
TDK	TFM201610A−2R2M	2.0 x 1.6 x 1.0	1.7	200
MURATA	LQH44PN−2R2MP0	4.0 x 3.5 x 1.8	1.8	59
MURATA	LQM2HPN−2R2MG0	2.5 x 2.0 x 1.0	1.3	100
TOKO	DFE252012C−2R2N	2.5 x 2.0 x 1.2	2.0	108

Output Capacitor Selection for DC to DC converters

Selecting the proper output capacitor is based on the desired output ripple voltage. NCP6924 DCDC converters typically use 10uF output capacitor. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode can be estimated by:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \times \left(\frac{1}{2 \times \pi \times C_O \times F_{SW}} + ESR \right) \quad \text{(eq. 3)}$$

Table 59. RECOMMENDED OUTPUT CAPACITOR FOR DC TO DC CONVERTERS

Manufacturer	Part Number	Case Size	HeightTyp. (mm)	C (μF)
MURATA	GRM188R60J106ME47	0603	0.8	10
MURATA	GRM219R60J106KE19	0805	1.25	10
MURATA	GRM21BR60J226ME39	0805	1.25	22
TDK	C1608X5R0C106K/M	0603	0.8	10
TDK	C2012X5R0C106K/M	0805	1.25	10
TDK	C2012X5R0C226K/M	0805	1.25	22

Input Capacitor Selection for DC TO DC converters

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is ⍰ of maximum output current. A low profile ceramic capacitor of 4.7μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to PVIN1 and PVIN2 pins.

Table 60. RECOMMENDED INPUT CAPACITOR FOR DC TO DC CONVERTERS

Supplier	Part Number	CaseSize	HeightTyp. (mm)	C (μF)
MURATA	GRM188R60J475KE	0603	0.8	4.7
MURATA	GRM188R60J106ME	0603	0.8	10
TDK	C1608X5R0C475K/M	0603	0.8	4.7
TDK	C1608X5R0C106K/M	0603	0.8	10

Output Capacitor for LDOs

For stability reason, a typical 2.2uF ceramic output capacitor is suitable for LDOs. The LDO output capacitor should be placed as close as possible to the NCP6924 output pin.

Input Capacitor for LDOs

NCP6924 LDOs do not require specific input capacitors. However, a typical 1uF ceramic capacitor placed close to LDOs' input is helpful for load transient.

Power input of LDO can be connected to main power supply. However, for optimum efficiency and lower NCP6924 thermal dissipation, the lowest voltage available in the system is preferred. Input voltage of each LDO should always be higher than V_{OUT} + $V_{LDODROP}$ (V_{DROP}, LDO dropout voltage at maximum current).

Capacitor DC bias characteristics

Real capacitance of ceramic capacitor changes versus DC voltage. Special care should be taken to DC bias effect in order to make sure that the real capacitor value is always higher than the minimum allowable capacitor value specified.

PCB Layout Recommendation

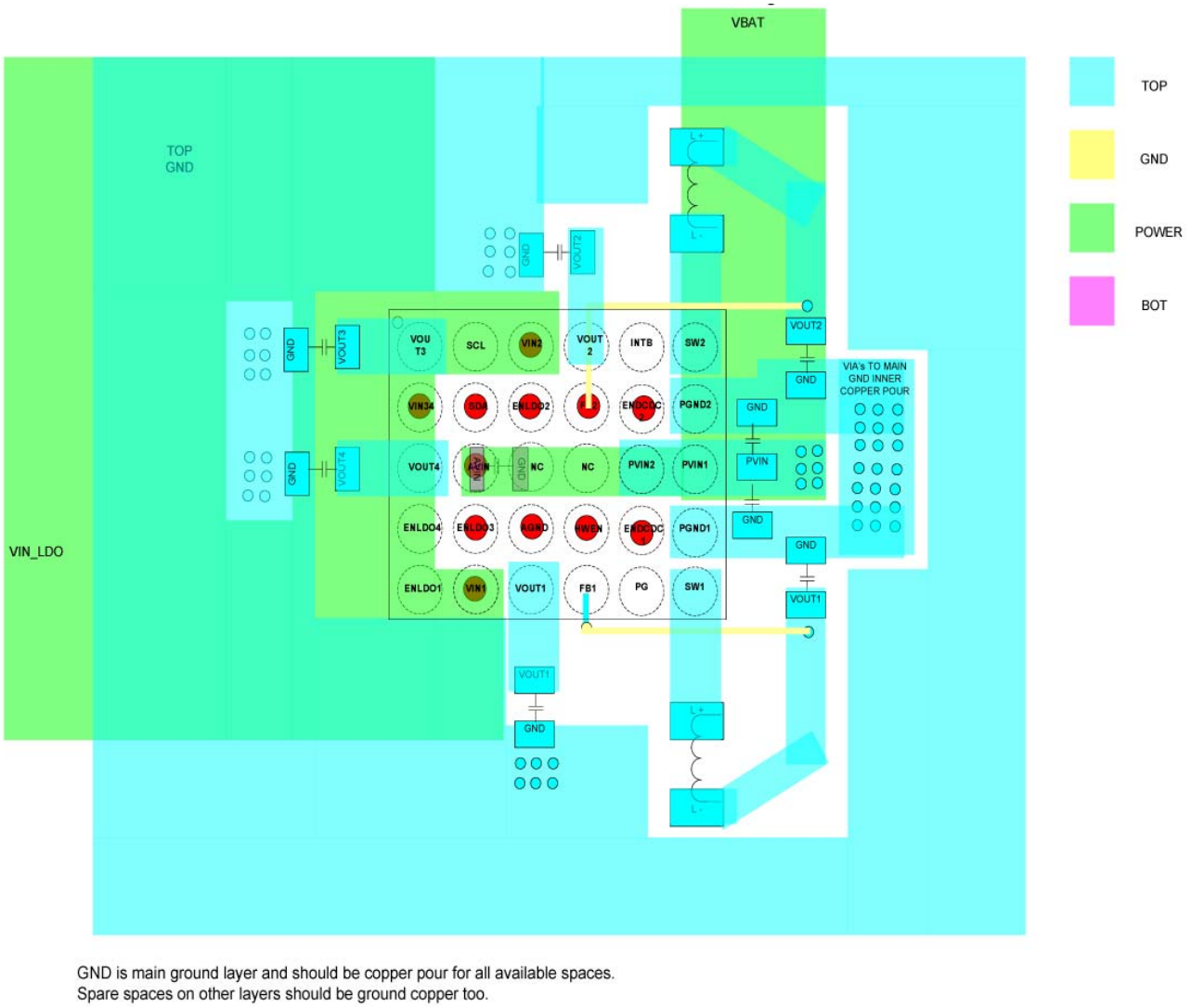
The high speed operation of the NCP6924 demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device, any high current copper trace which see high frequency switching should be optimized. Therefore, use short and wide traces for power current paths and for power ground tracks, power plane and ground plane are recommended if possible.

Both the inductor and input/output capacitor of each DC to DC converters are in the high frequency switching path where current flow may be discontinuous. These components should be placed as close to NCP6924 as

possible to reduce parasitic inductance connection. Also it is important to minimize the area of the switching nodes and use the ground plane under them to minimize cross−talk to sensitive signals and ICs. It's suggested to keep as complete of a ground plane under NCP6924 as possible.

PGND and AGND pin connection must be connected to the ground plane. Care should be taken to avoid noise interference between PGND and AGND.

It is always good practice to keep the sensitive tracks such as feedback connection (FB1 / FB2) away from switching signal connections (SW1 / SW2) by laying the tracks on the other side or inner layers of PCB.



GND is main ground layer and should be copper pour for all available spaces.
Spare spaces on other layers should be ground copper too.

Figure 40. Recommended PCB Layout

Thermal Considerations

Careful attention must be paid to the power dissipation of the NCP6924. The power dissipation is a function of efficiency and output power. Hence, increasing the output power requires better components selection. Care should be taken of LDO V_{DROP}, the larger it is, the higher dissipation it will bring to NCP6924. Keep a large copper plane under and close to NCP6924 is helpful for thermal dissipation.

ORDERING INFORMATION

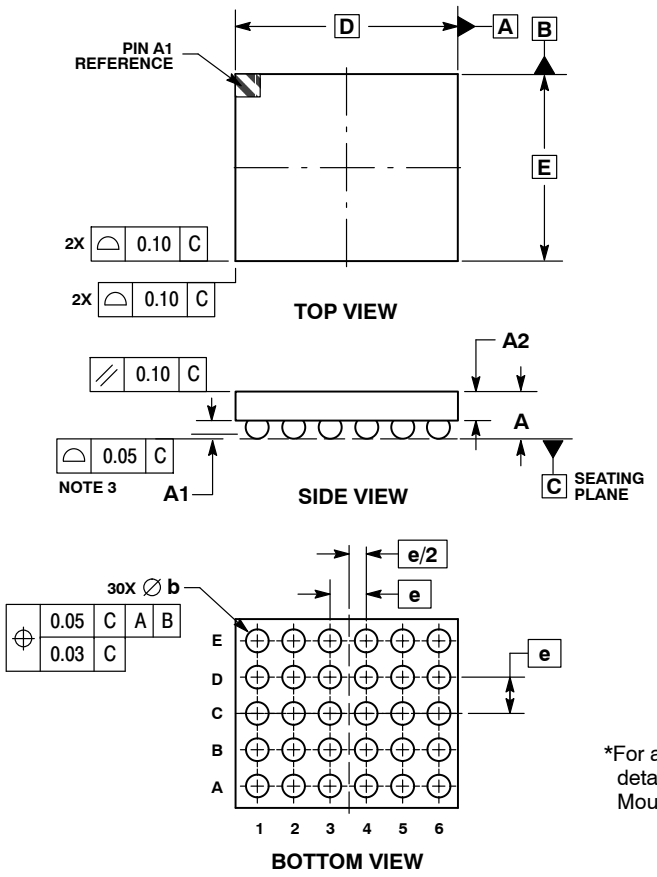
Device	Marking	Comment	Package	Shipping†
NCP6924AFCHT1G*	6924AH	HWEN default version (See detailed description)	WLCSP30 (Pb–Free)	3000 / Tape & Reel
NCP6924AFCET1G*	6924AE	Enabled default version (See detailed description)		
NCP6924BFCHT1G*	6924BH	HWEN version (See detailed description)		
NCP6924CFCHT1G*	6924CH	HWEN version (See detailed description)		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This is flip chip package without die coating

Demo Board Available:
The NCP6924GEVB/D evaluation board configures the device in typical application to supply constant voltage.

PACKAGE DIMENSIONS

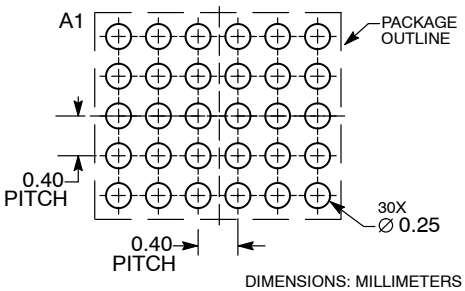
WLCSP30, 2.46x2.06
CASE 567CU
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.33	0.39
b	0.24	0.29
D	2.46 BSC	
E	2.06 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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