- **Output Swing includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 850 μV Max at T_A = 25°C (TLC2252A)**
- **Macromodel Included**

description

The TLC2252 and TLC2252A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices exhibit rail-to-rail output performance while having better input offset voltage and lower power dissipation levels than existing CMOS operational amplifiers. In addition, the noise performance has been dramatically improved for this class of low-power CMOS amplifier. Figure 1 depicts the low level of voltage noise for this CMOS amplifier, which has only 35 μA (typical) of supply current per amplifier. Also, the common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

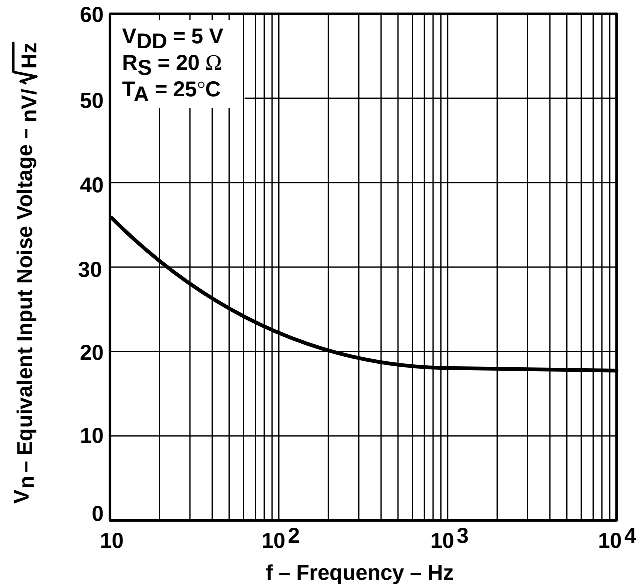

Figure 1

The TLC2252 and TLC2252A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the low-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features, combined with its temperature performance, make the TLC2252 family ideal for sonobuoys, remote pressure sensors, temperature control, active VR sensors, accelerometers, portable medical applications, hand-held metering, and many other applications.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	1500 μV	TLC2252CD	TLC2252CP	TLC2252CPWLE	TLC2252Y
–40°C to 125°C	850 μV 1500 μV	TLC2252AID TLC2252ID	TLC2252AIP TLC2252IP	TLC2252AIPWLE —	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2252CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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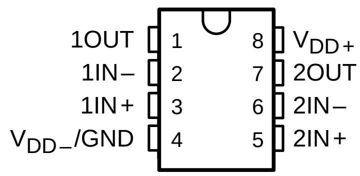
description (continued)

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

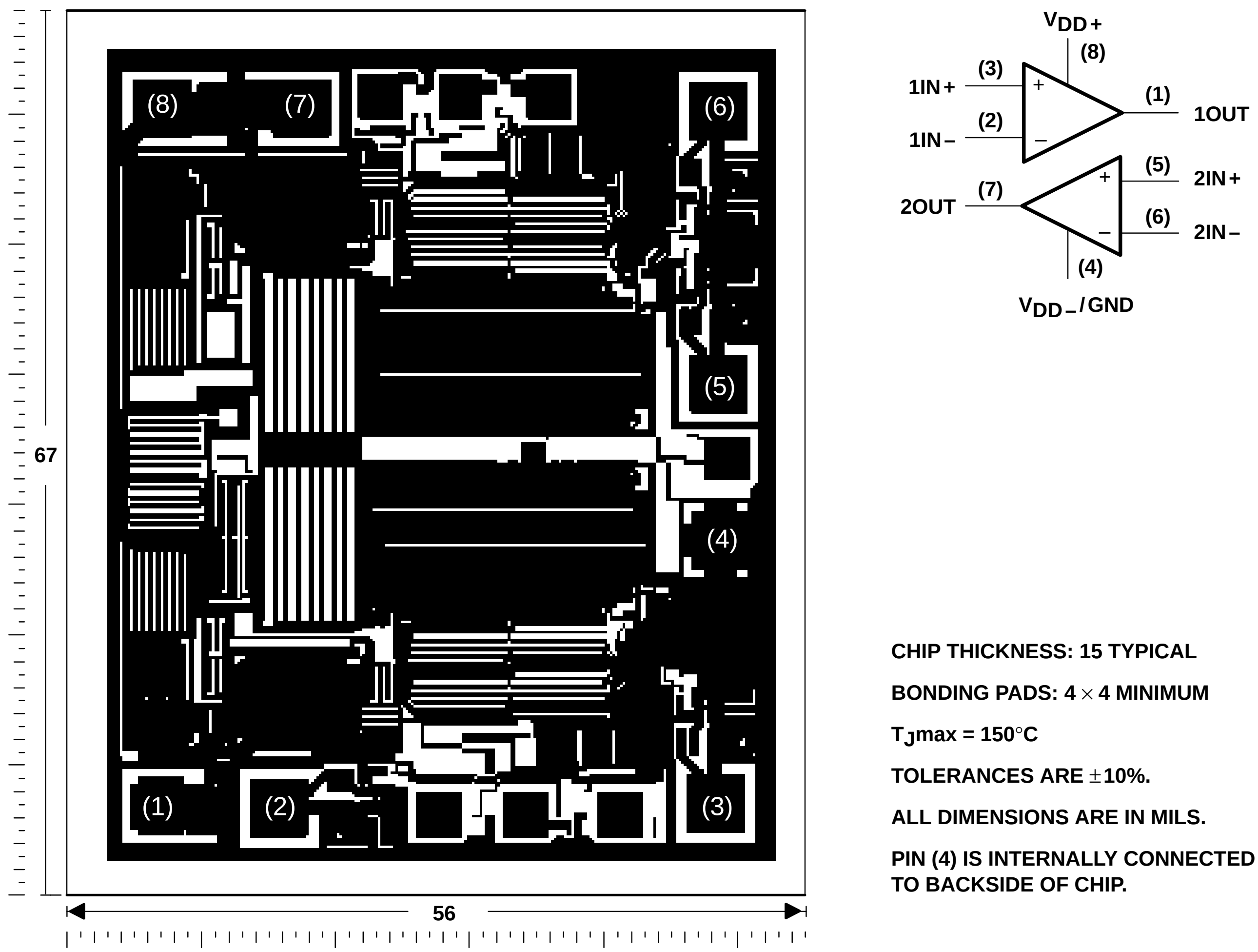
D, P, OR PW PACKAGE
(TOP VIEW)



TLC2252Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2252C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

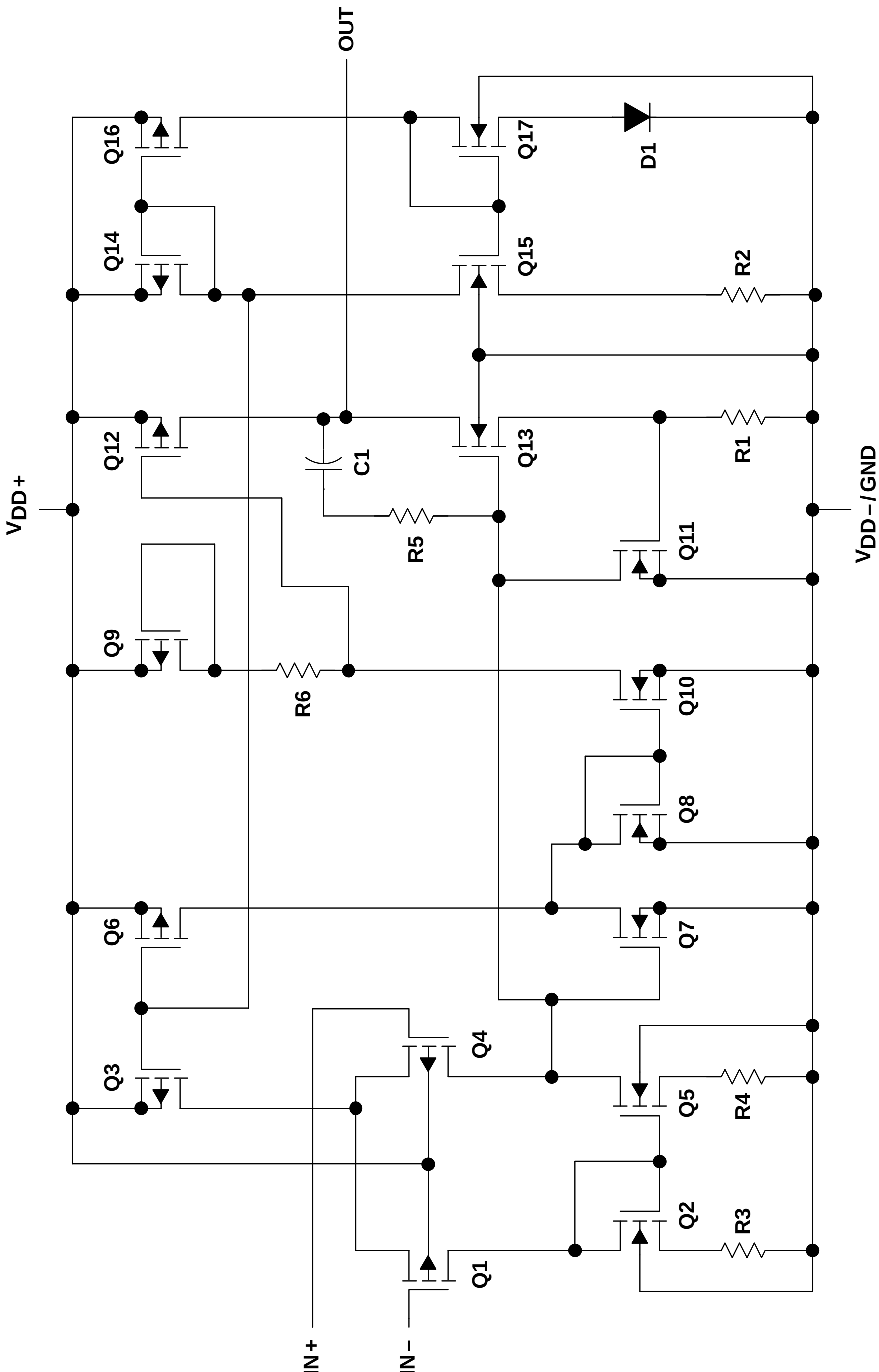
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	30
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows if input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Operating free-air temperature, T_A	0	70	–40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2252C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD}\pm$ = ±2.5 V, V_O = 0, R_S = 50 Ω	25°C		200	1500	µV
			Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\|$ ≤ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA	25°C		4.98		V
		I_{OH} = −75 µA	25°C	4.9	4.94		
			Full range	4.8			
		I_{OH} = −150 µA	25°C	4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 µA	25°C		0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.09	0.15	
			Full range			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3	
			Full range			0.3	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C		0.7	1	
			Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 100 kΩ‡	25°C	100	350		V/mV
			Full range	10			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		1700		
r_{id}	Differential input resistance		25°C		10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10	25°C		200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		dB
			Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		70	125	µA
			Full range			125	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 100 kΩ‡,	25°C	0.07	0.12		V/μs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%		
			A_V = 10			1%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A†	TLC2252C MIN	TLC2252C TYP	TLC2252C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500	μV
			Full range			1750	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV, $R_S = 50\ \Omega$	25°C	–5 to 4	–5.3 to 4.2		V
			Full range	–5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.98		V
		$I_O = -100\ \mu A$	25°C	4.9	4.93		
			Full range	4.7			
		$I_O = -200\ \mu A$	25°C	4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		–4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	–4.85	–4.91		
			Full range	–4.85			
		$V_{IC} = 0$, $I_O = 1$ mA	25°C	–4.7	–4.8		
			Full range	–4.7			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	–4	–4.3		
			Full range	–3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 100\ k\Omega$	25°C	45	650		V/mV
			Full range	10			
		$V_O = \pm 4$ V, $R_L = 1\ M\Omega$	25°C		3000		
r_{id}	Differential input resistance		25°C		10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C		190		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		dB
			Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = 2.2$ V to ± 8 V, $V_{IC} = 0$, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current	$V_O = 0$, No load	25°C		80	125	μA
			Full range			125	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252C MIN	TLC2252C TYP	TLC2252C MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm1.9$ V, $C_L = 100$ pF	$R_L = 100$ kΩ,	25°C	0.07	0.12		V/µs
				Full range	0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38		nV/√Hz
		f = 1 kHz		25°C		19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion pulse duration	$V_O = \pm2.3$ V, f = 10 kHz, $R_L = 50$ kΩ	$A_V = 1$	25°C		0.2%		
			$A_V = 10$			1%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		14		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		63°		
	Gain margin			25°C		15		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\| \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.98			4.98		V
		I_{OH} = −75 μA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 μA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		70	125		70	125	μA
				Full range			125			125	

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2252I			TLC2252AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500		200	850	µV
			Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\|V_{IO}\| \le 5$ mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
			Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.98			4.98		V
		$I_O = -100\ \mu A$	25°C	4.9	4.93		4.9	4.93		
			Full range	4.7			4.7			
		$I_O = -200\ \mu A$	25°C	4.8	4.86		4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		−4.99			−4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	−4.85	−4.91		−4.85	−4.91		
			Full range	−4.85			−4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	−4	−4.3		−4	−4.3		
			Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V, $R_L = 50\ k\Omega$	25°C	40	150		40	150		V/mV
			Full range	10			10			
		$V_O = \pm4$ V, $R_L = 1\ M\Omega$	25°C		3000			3000		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C		190			190		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V, No load	25°C		80	125		80	125	µA
			Full range			125			125	

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2252I			TLC2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9$ V, $R_L = 50$ kΩ, $C_L = 100$ pF		25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		38			38		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 50$ kΩ, f = 10 kHz	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	f =10 kHz, $R_L = 50$ kΩ, $C_L = 100$ pF		25°C		0.21			0.21		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		14			14		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ, $C_L = 100$ pF		25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is –40°C to 125°C.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLC2252Y MIN	TLC2252Y TYP	TLC2252Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω			200	1500	μV
I_{IO}	Input offset current					0.5	100	pA
I_{IB}	Input bias current					1	100	pA
V_{ICR}	Common-mode input voltage range	| V_{IO} | ≤5 mV,	R_S = 50 Ω		0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				4.98		V
		I_{OH} = −75 μA			4.9	4.94		
		I_{OH} = −150 μA			4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA			0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA			0.8	1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ†		100	350		V/mV
			R_L = 1 MΩ†			1700		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V,	R_S = 50 Ω	70	83		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V,	V_{IC} = V_{DD}/2,	No load	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load			70	125	μA

† Referenced to 2.5 V

electrical characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLC2252Y MIN	TLC2252Y TYP	TLC2252Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$,	$V_O = 0$, $R_S = 50\ \Omega$			200	1500	μV
I_{IO}	Input offset current	$V_{IC} = 0$,	$V_O = 0$, $R_S = 50\ \Omega$			0.5	100	pA
I_{IB}	Input bias current	$V_{IC} = 0$,	$V_O = 0$, $R_S = 50\ \Omega$			1	100	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	$R_S = 50\ \Omega$		–5 to 4	–5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$				4.99		V
		$I_O = -100\ \mu A$			4.9	4.93		
		$I_O = -200\ \mu A$			4.8	4.86		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_{OL} = 50\ \mu A$			–4.99		V
		$V_{IC} = 0$,	$I_{OL} = 500\ \mu A$		–4.85	–4.91		
		$V_{IC} = 0$,	$I_{OL} = 4$ mA		–3.8	–4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V	$R_L = 100\ k\Omega$		40	150		V/mV
		$V_O = \pm4$ V	$R_L = 1\ M\Omega$			3000		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	$A_V = 10$			190		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V,	$V_O = 0$,	$R_S = 50\ \Omega$	75	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V,	$V_{IC} = 0$,	No load	80	95		dB
I_{DD}	Supply current	$V_O = 0$,	No load			80	125	μA

TYPICAL CHARACTERISTICS

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V_{OM-}	Maximum negative peak output voltage	vs Output current	15
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TYPICAL CHARACTERISTICS

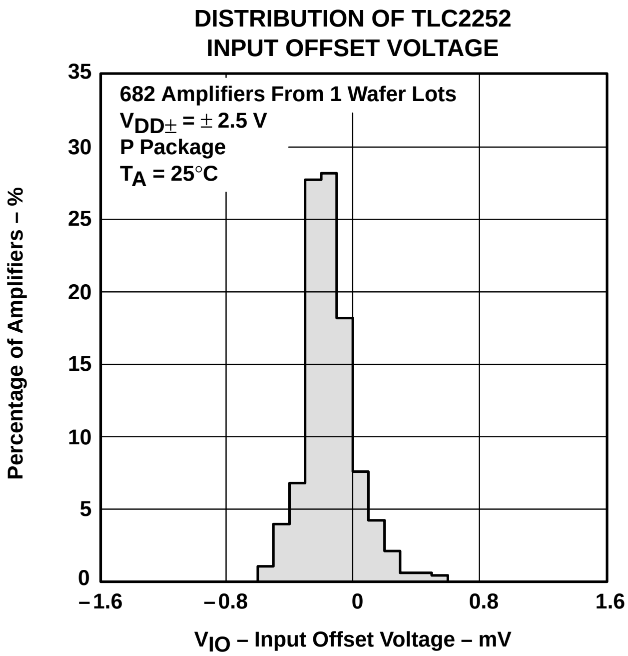


Figure 2

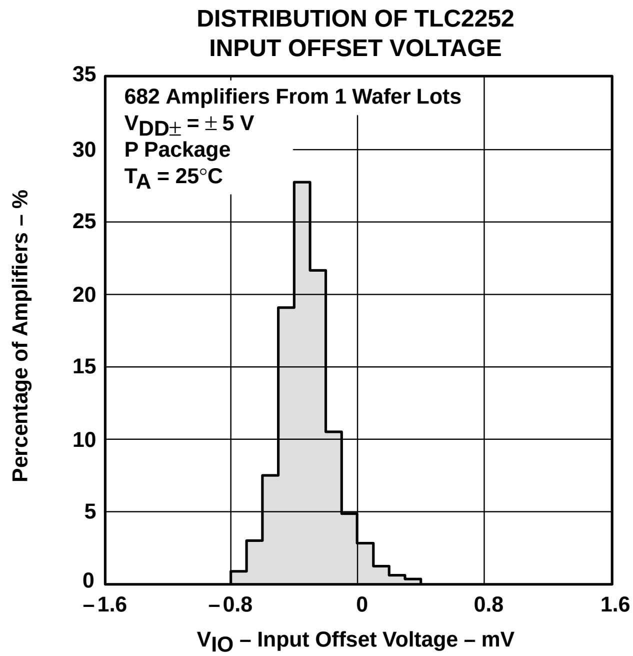
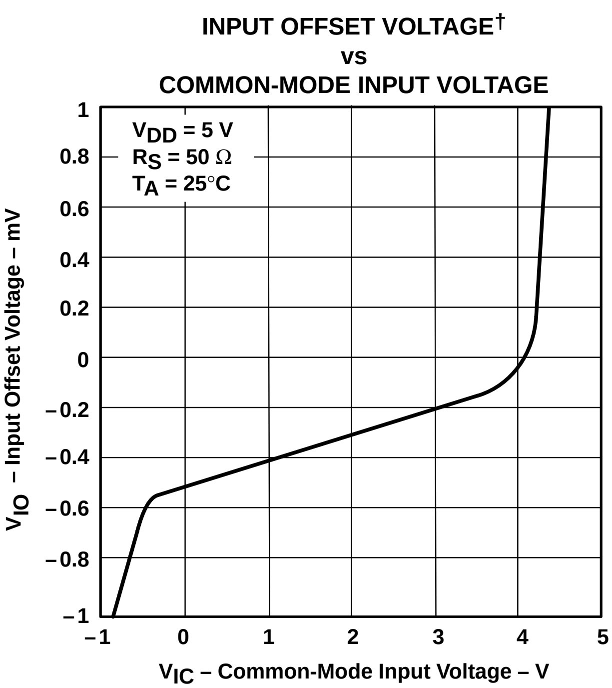


Figure 3



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 4

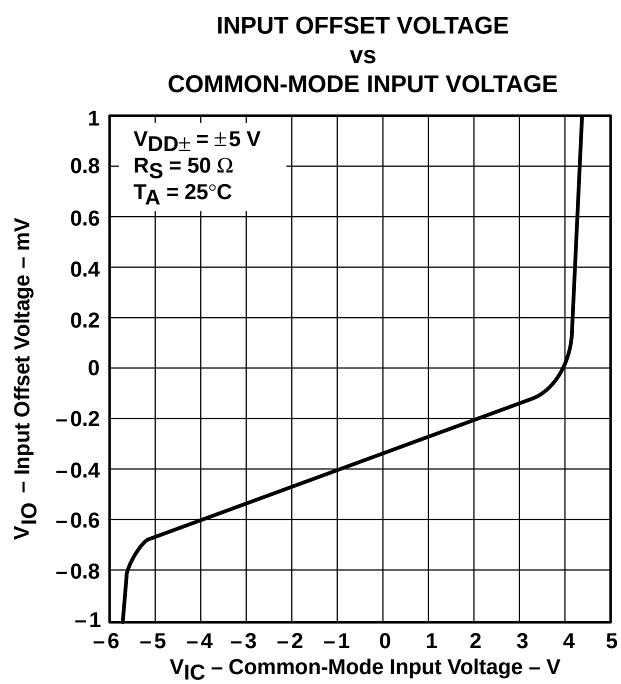


Figure 5

TYPICAL CHARACTERISTICS†

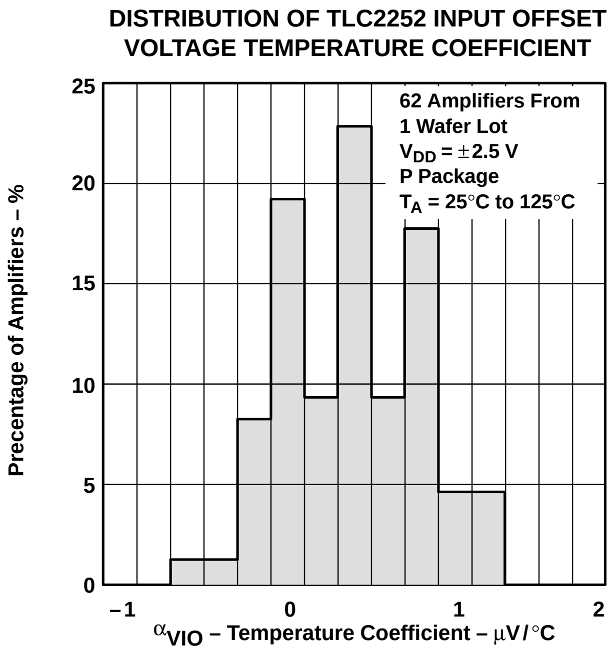


Figure 6

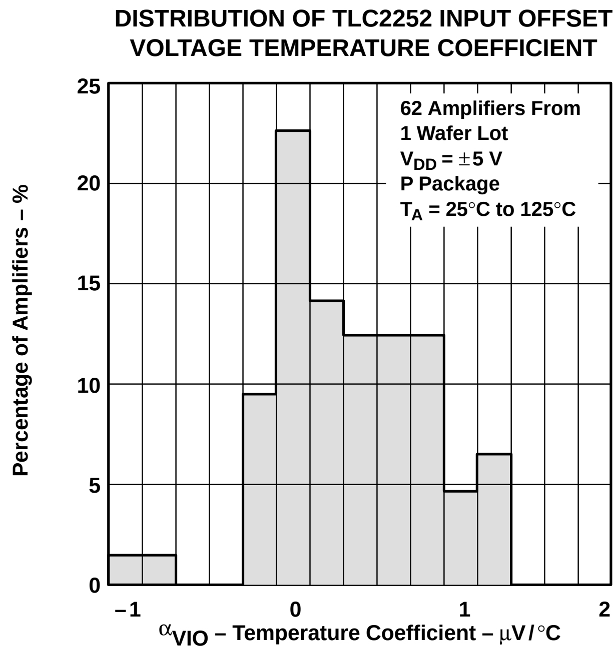


Figure 7

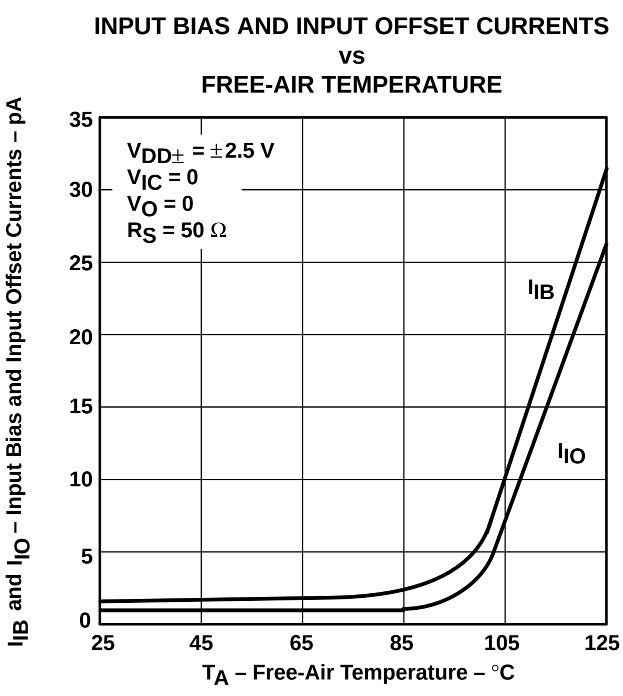


Figure 8

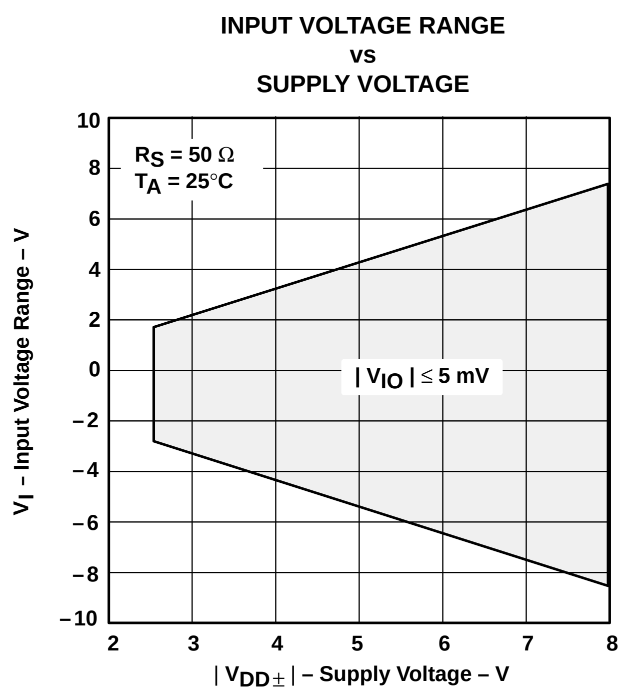


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

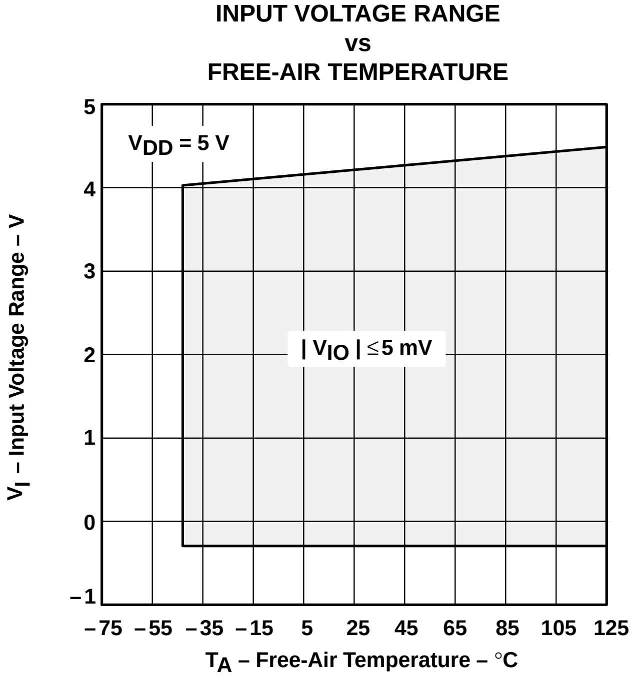


Figure 10

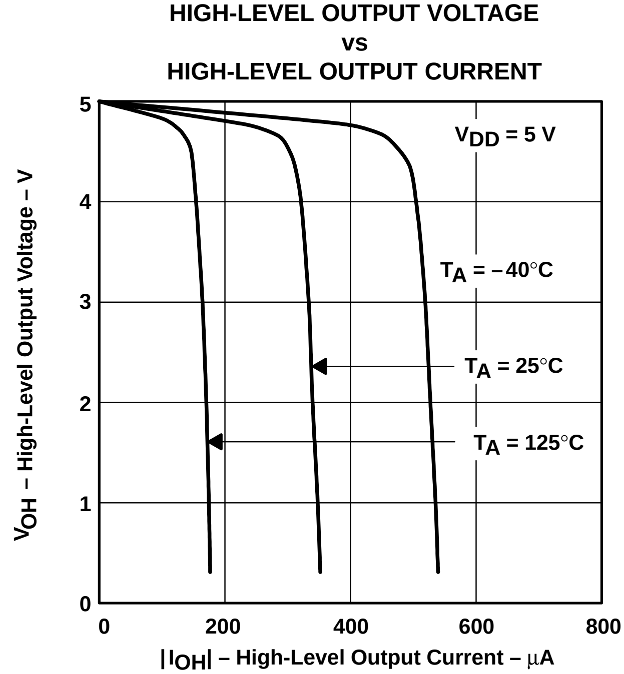


Figure 11

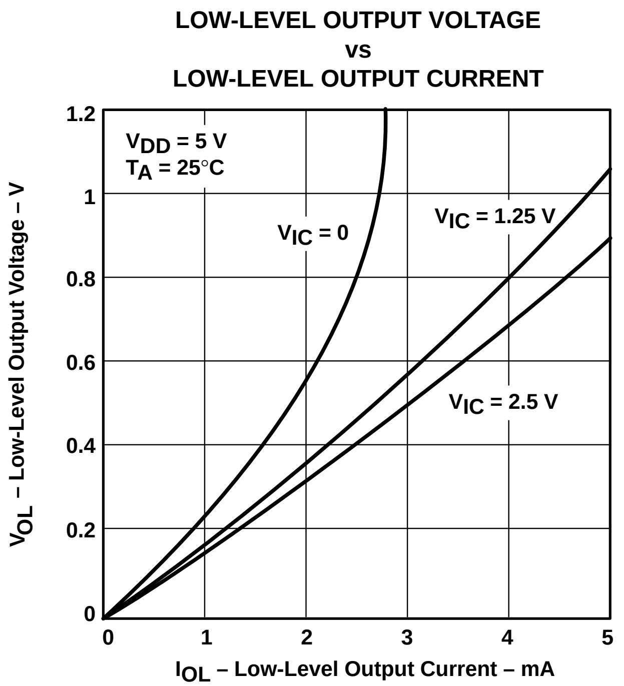


Figure 12

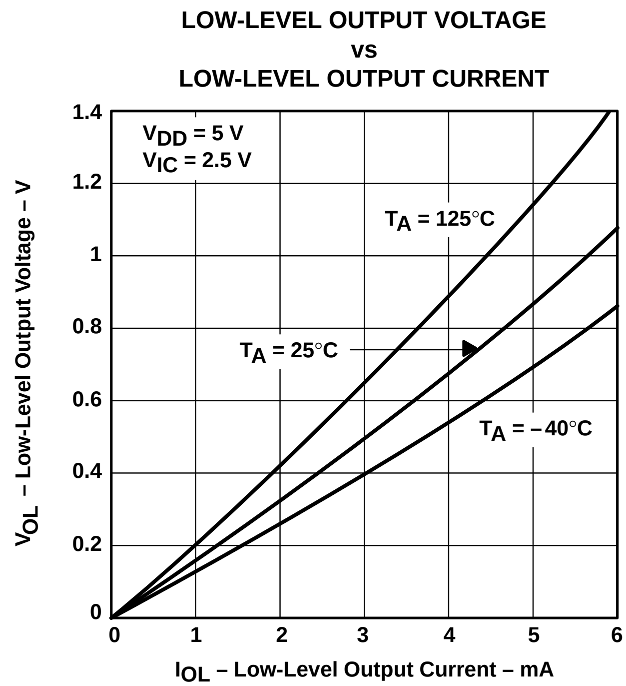


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

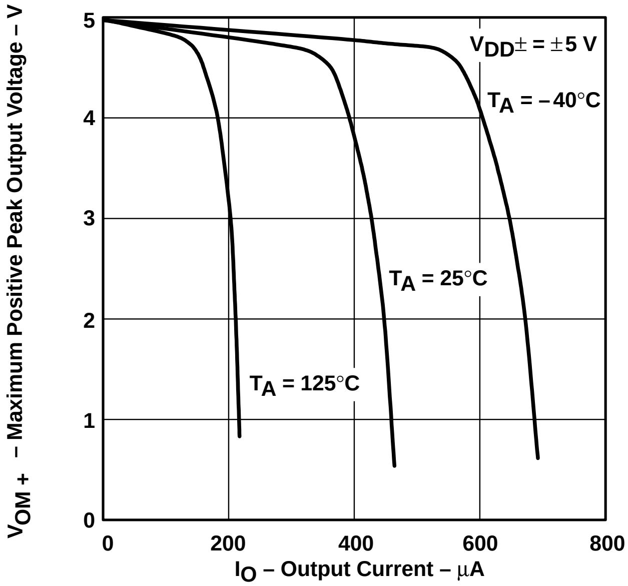


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

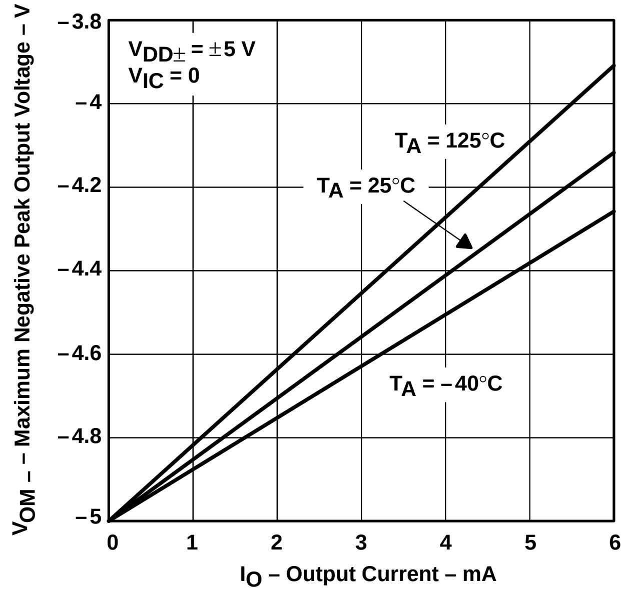
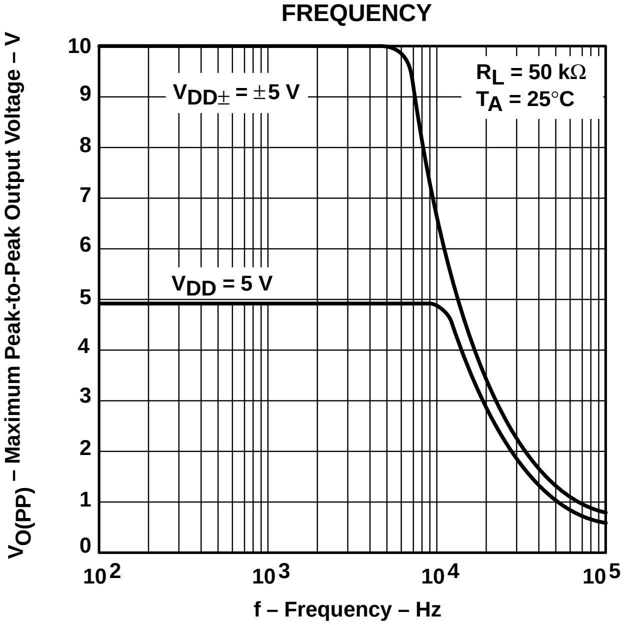


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE† vs FREQUENCY



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

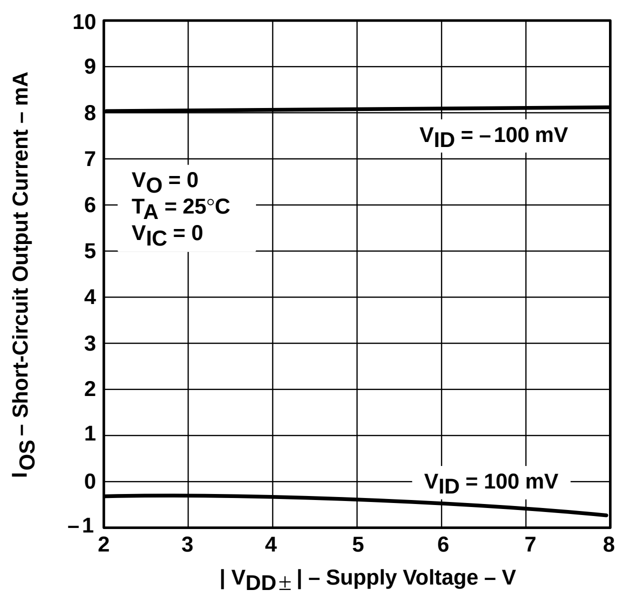


Figure 17

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

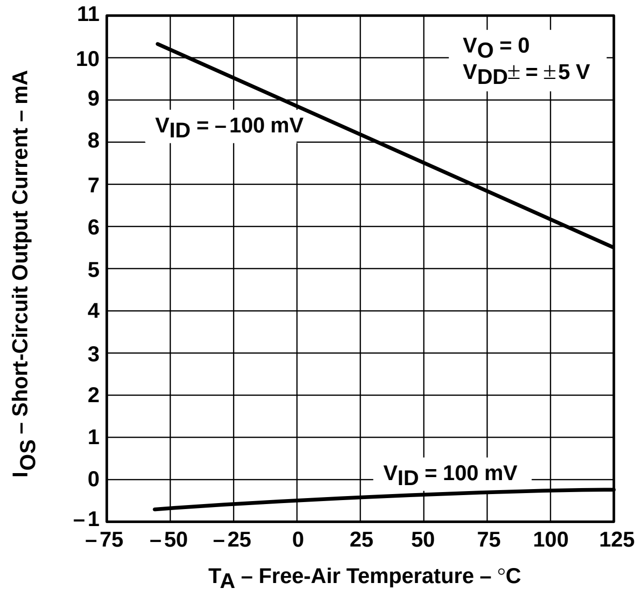


Figure 18

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

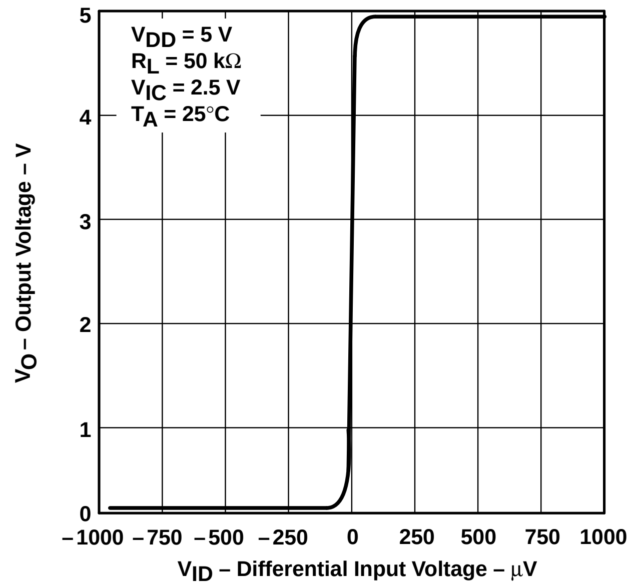


Figure 19

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

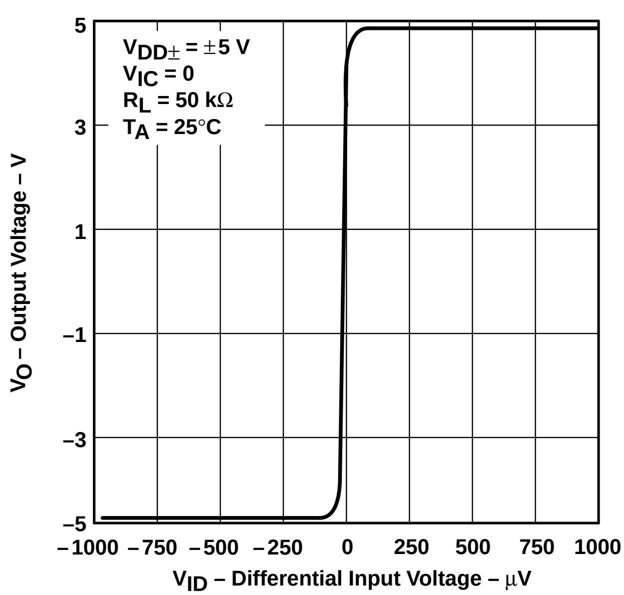


Figure 20

DIFFERENTIAL GAIN‡
vs
LOAD RESISTANCE

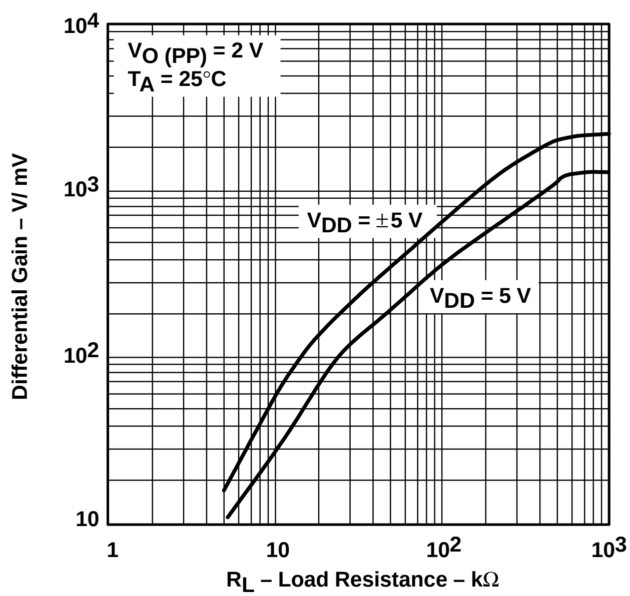
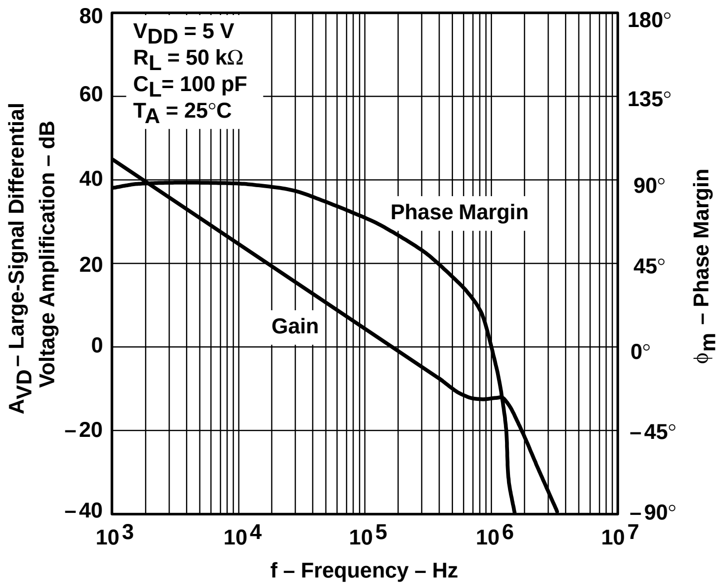


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

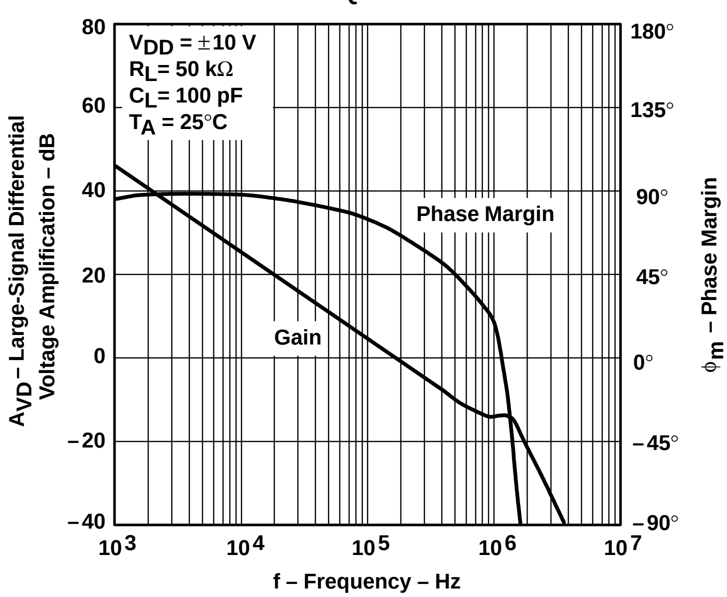


Figure 23

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL‡ VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

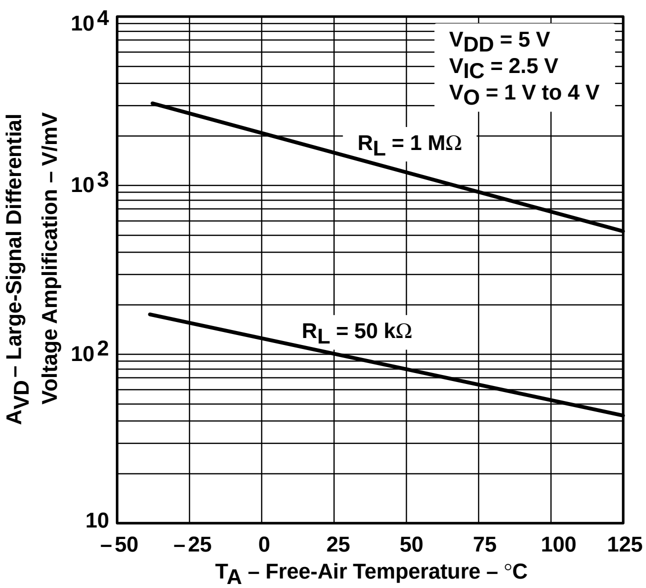


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

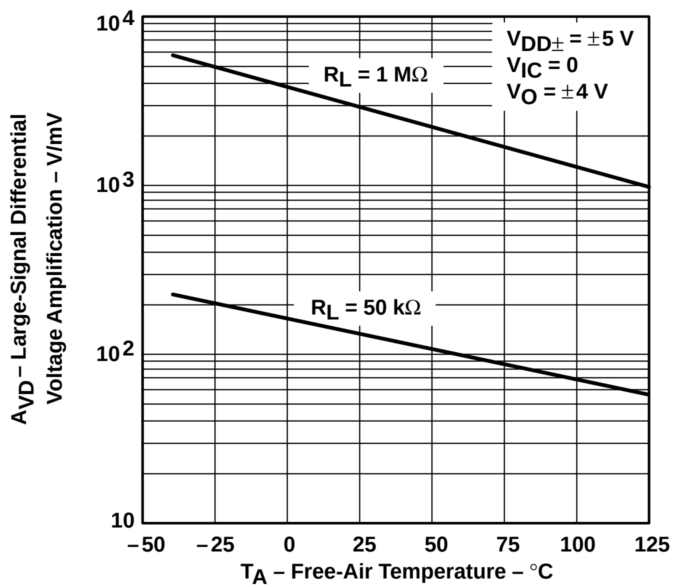


Figure 25

OUTPUT IMPEDANCE‡ vs FREQUENCY

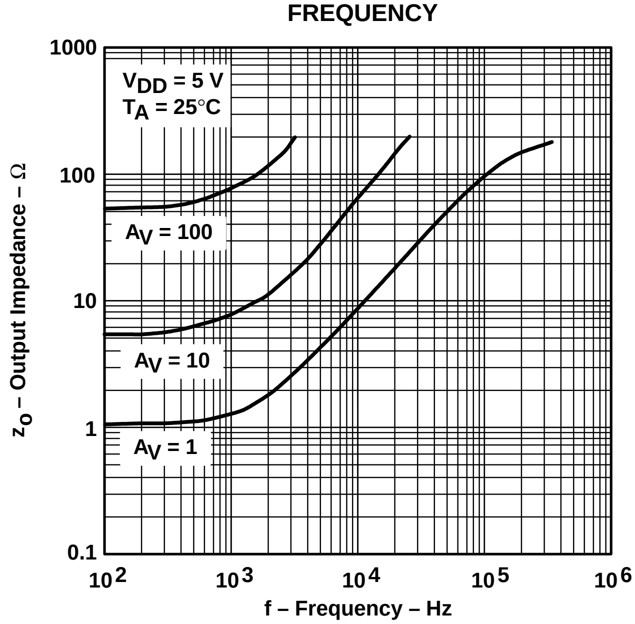


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

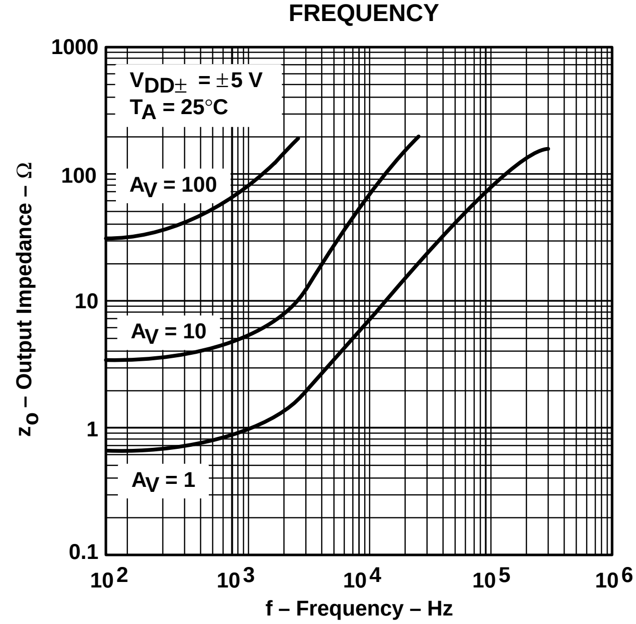


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

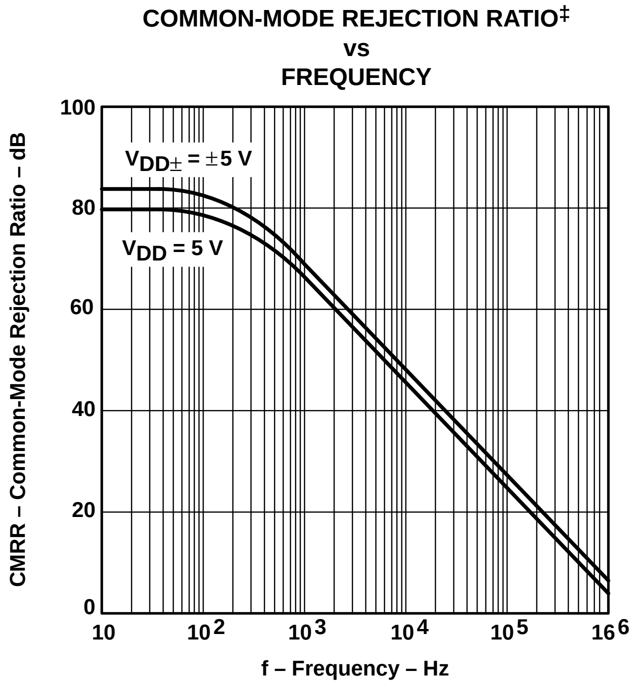


Figure 28

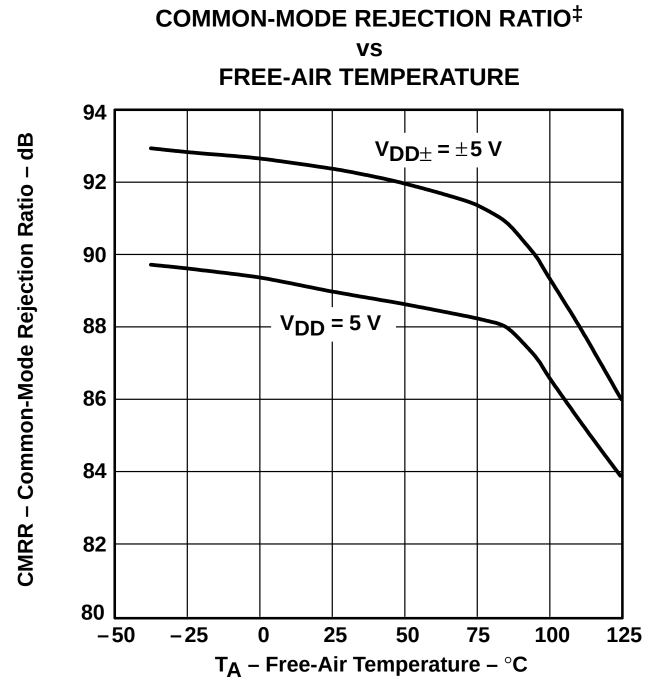


Figure 29

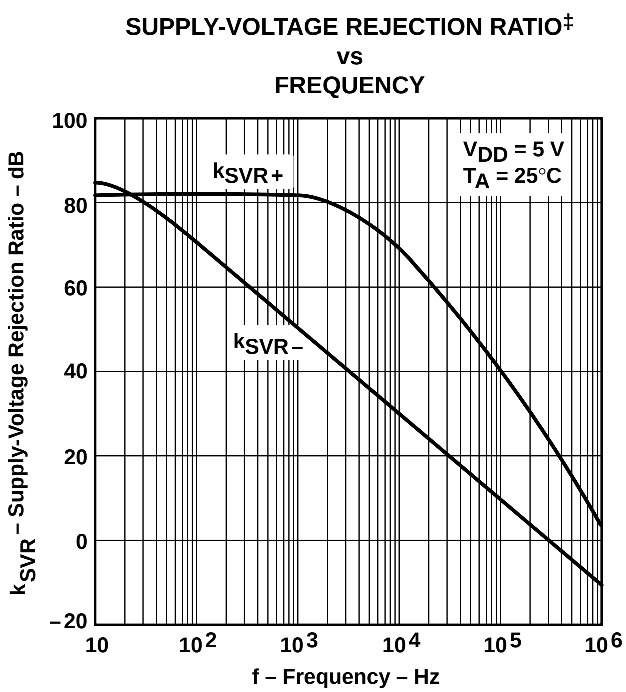


Figure 30

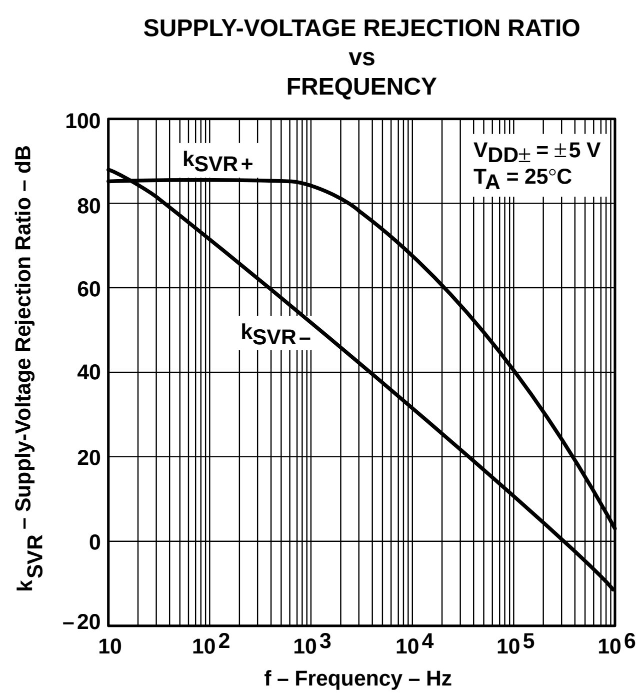


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

**SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE**

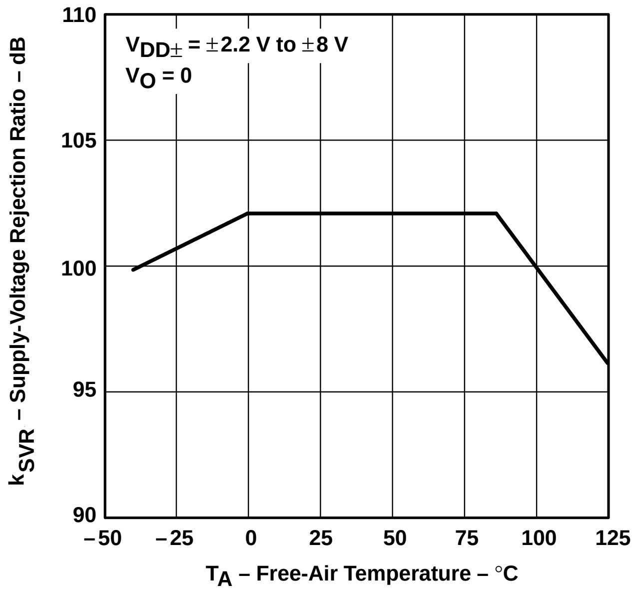


Figure 32

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

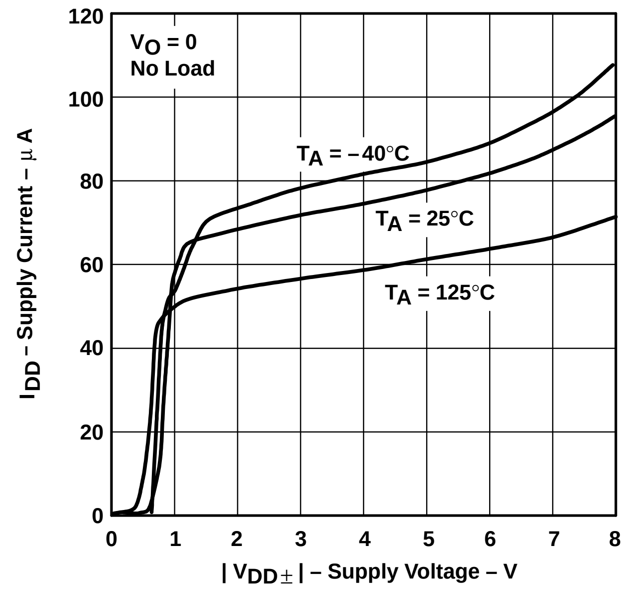


Figure 33

**SUPPLY CURRENT‡
vs
FREE-AIR TEMPERATURE**

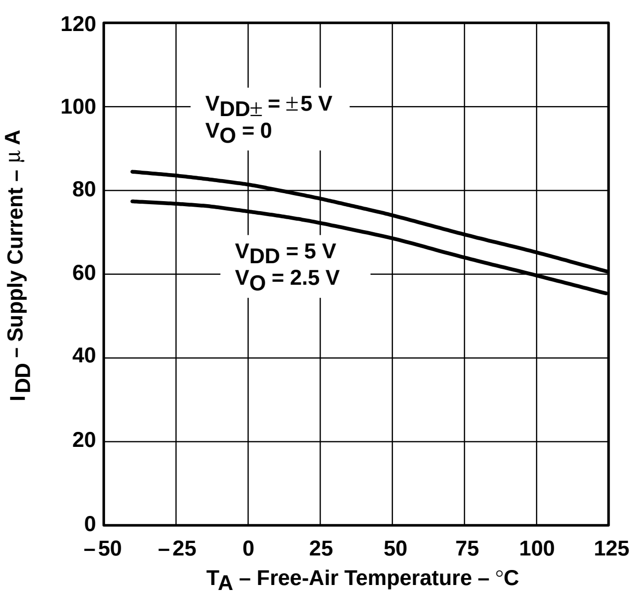


Figure 34

**SLEW RATE‡
vs
LOAD CAPACITANCE**

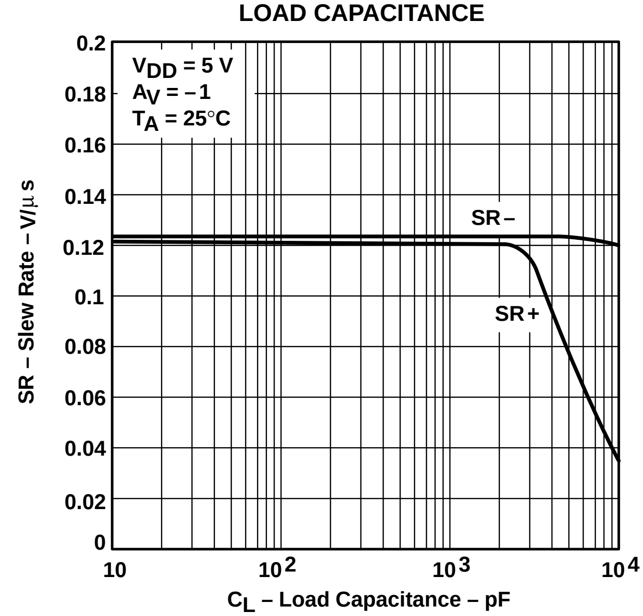


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

SLEW RATE‡ vs FREE-AIR TEMPERATURE

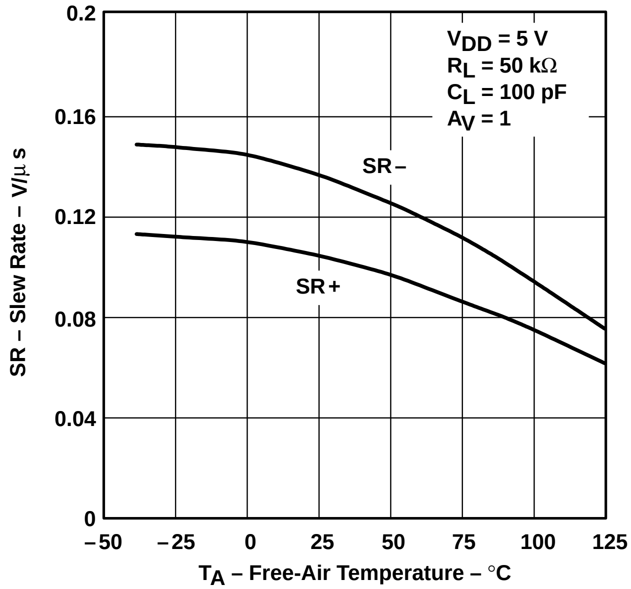


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE‡

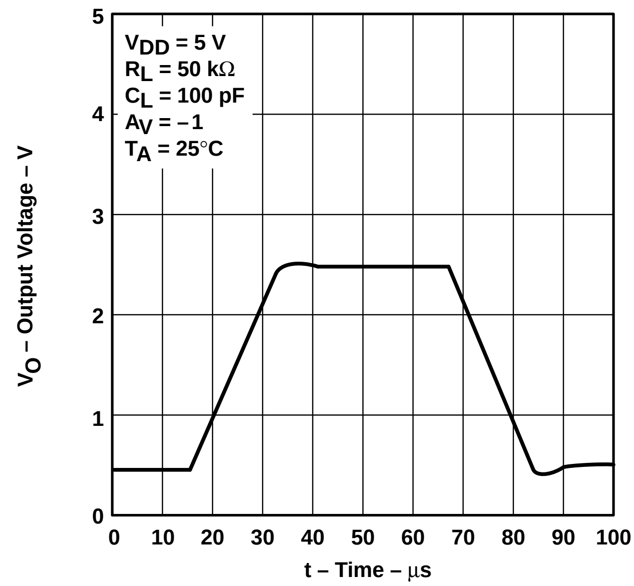


Figure 37

INVERTING LARGE-SIGNAL PULSE RESPONSE

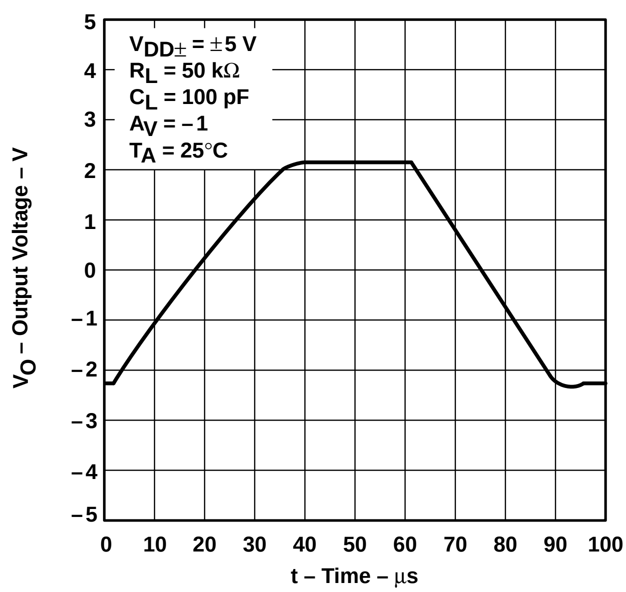


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE‡

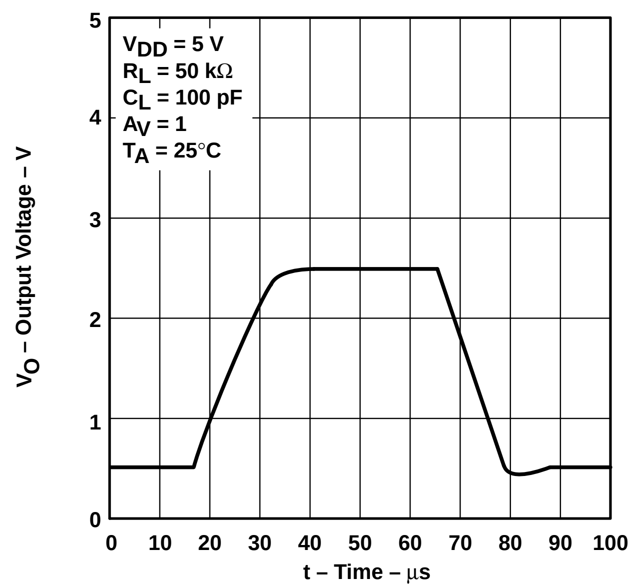


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

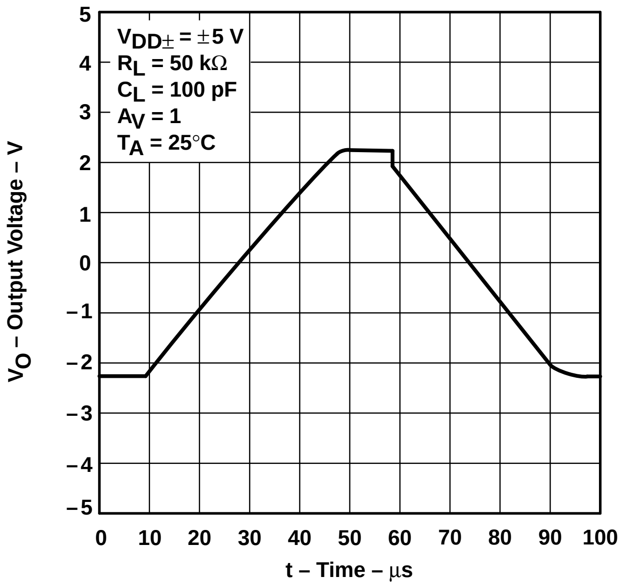


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE†

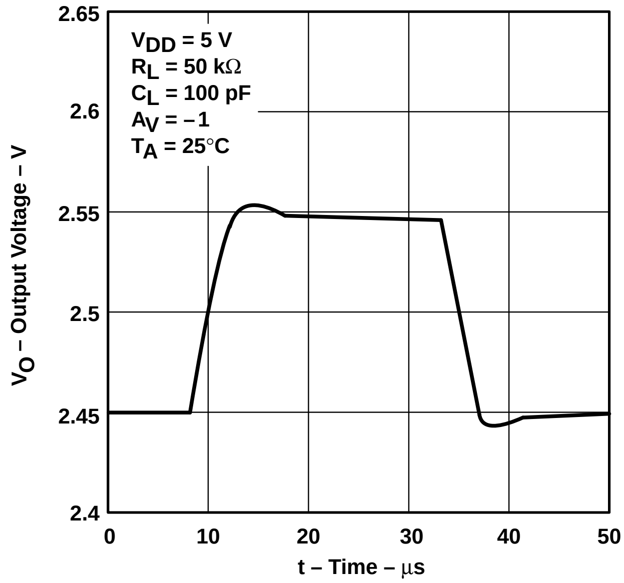


Figure 41

INVERTING SMALL-SIGNAL PULSE RESPONSE

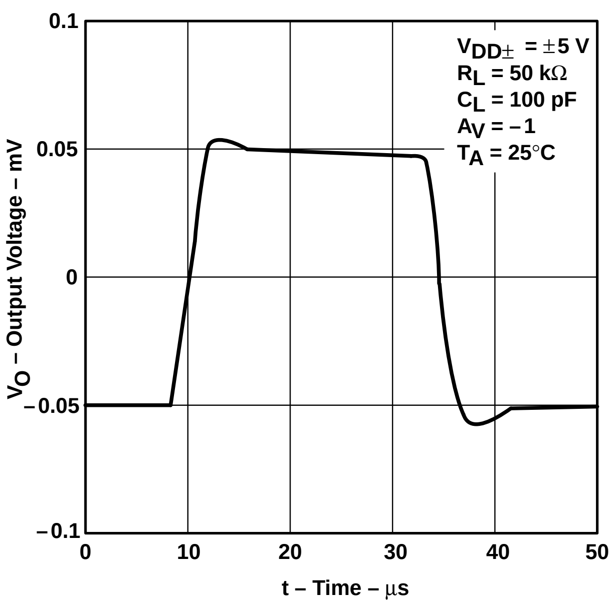


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

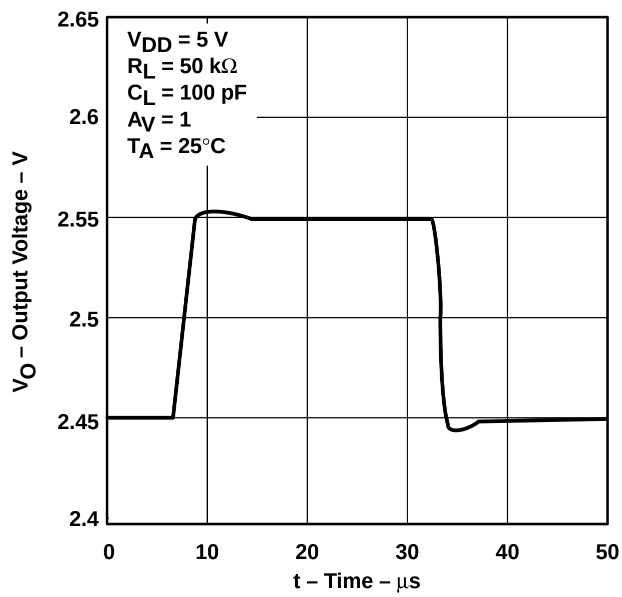


Figure 43

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

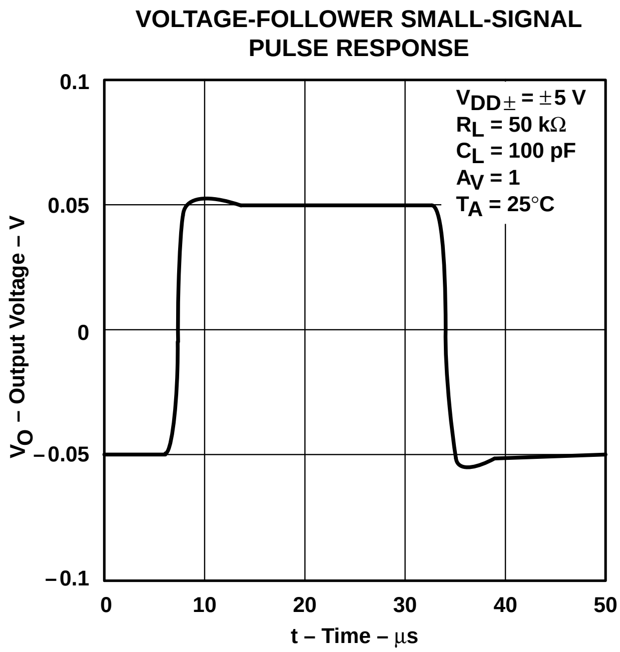


Figure 44

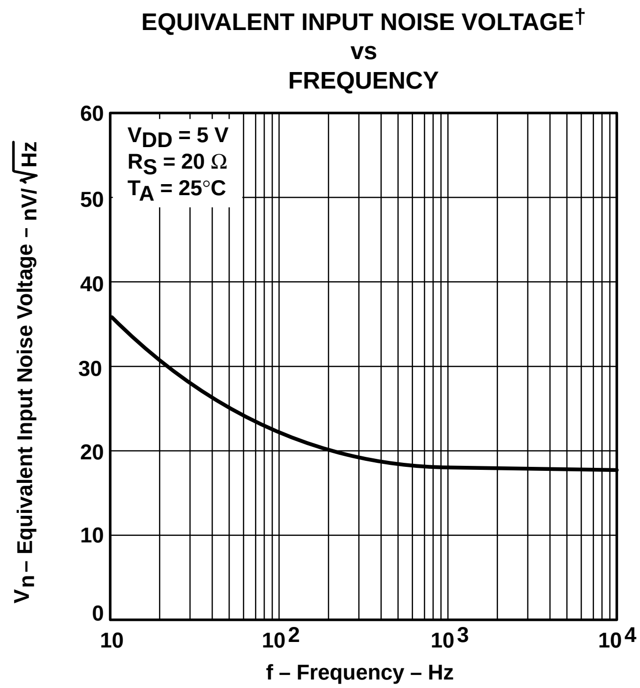


Figure 45

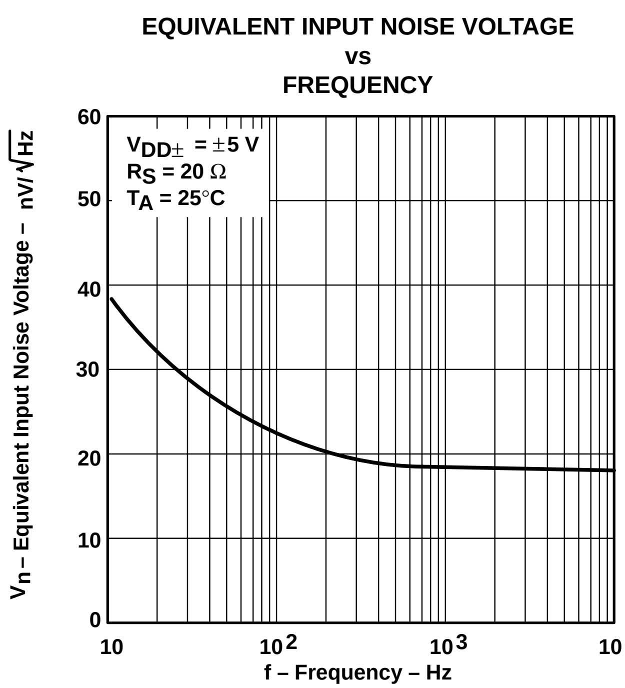


Figure 46

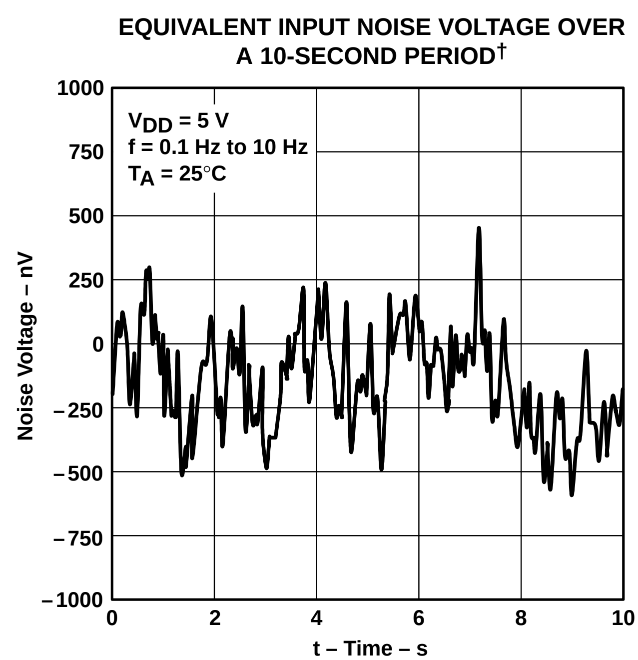


Figure 47

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

**INTEGRATED NOISE VOLTAGE
vs
FREQUENCY**

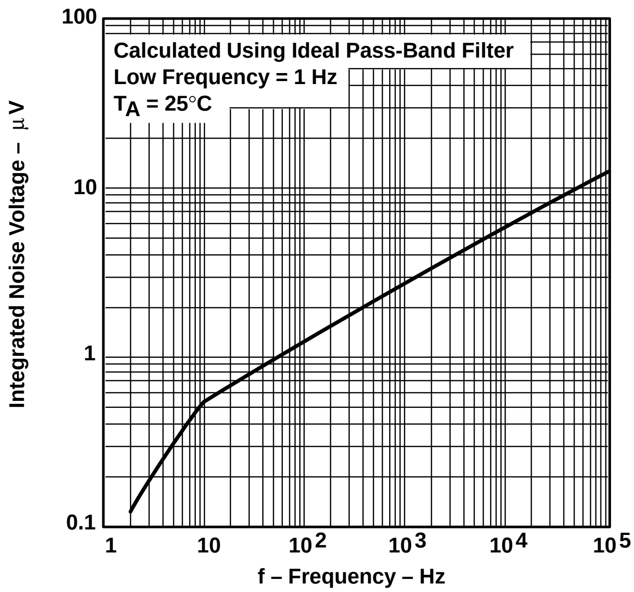


Figure 48

**TOTAL HARMONIC DISTORTION PLUS NOISE‡
vs
FREQUENCY**

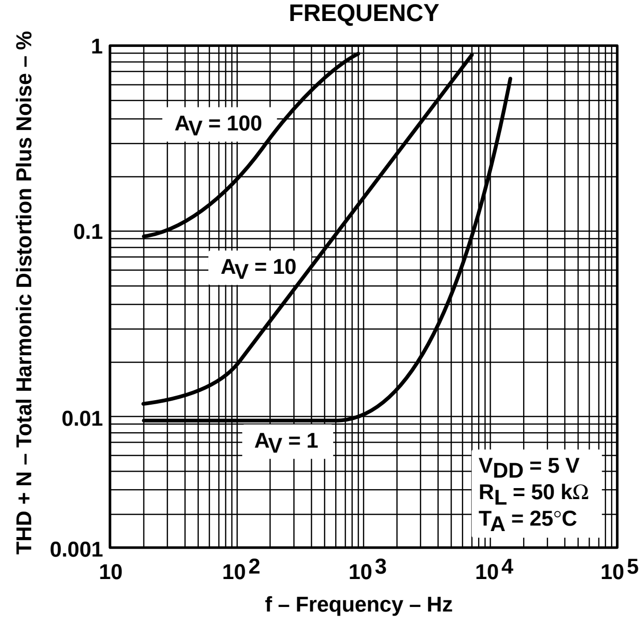


Figure 49

**GAIN-BANDWIDTH PRODUCT‡
vs
FREE-AIR TEMPERATURE**

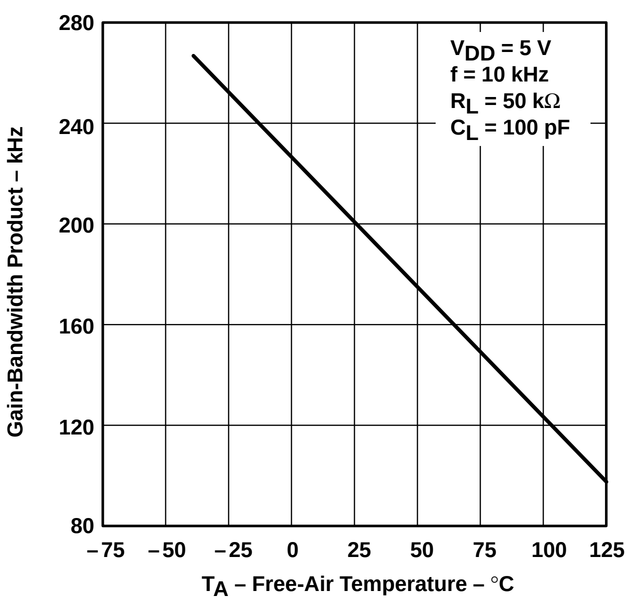


Figure 50

**GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE**

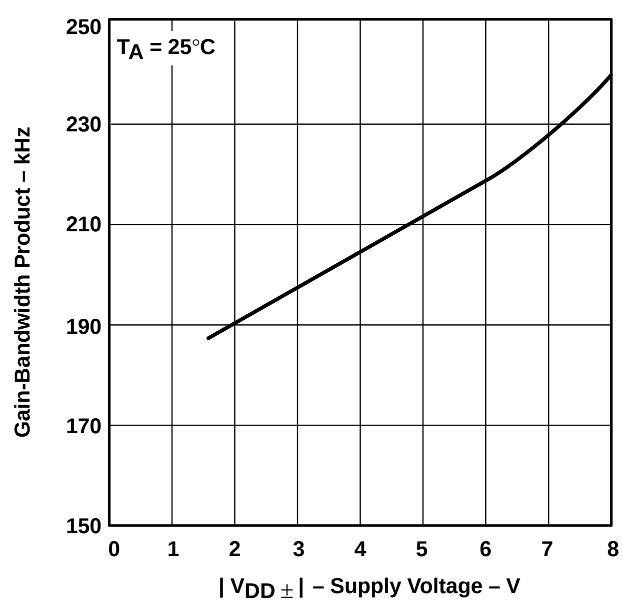


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

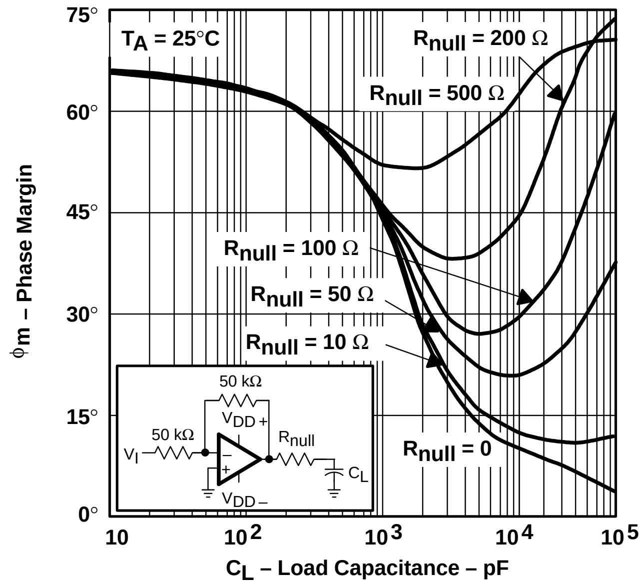


Figure 52

GAIN MARGIN vs LOAD CAPACITANCE

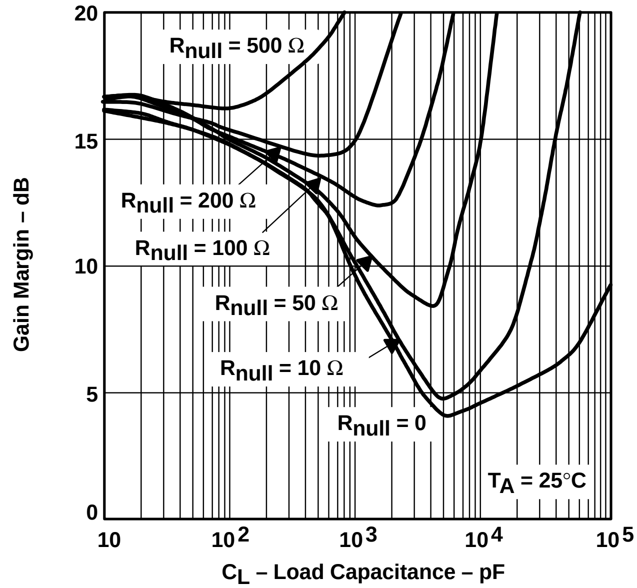


Figure 53

UNITY-GAIN BANDWIDTH† vs LOAD CAPACITANCE

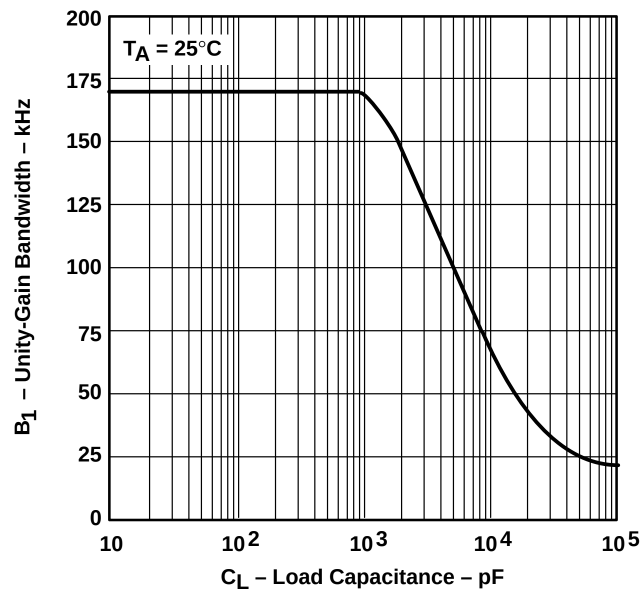


Figure 54

OVERESTIMATION OF PHASE MARGIN† vs LOAD CAPACITANCE

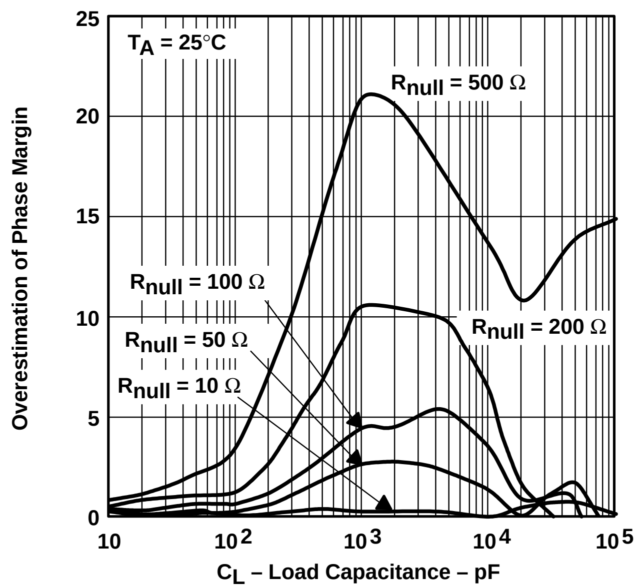


Figure 55

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 52 and Figure 53 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see NO TAG) improves the gain and phase margins when driving large capacitive loads. Figure 52 and Figure 53 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \quad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 54). To use equation (1), UGBW must be approximated from Figure 54.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 55. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 56, with equation (1) enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

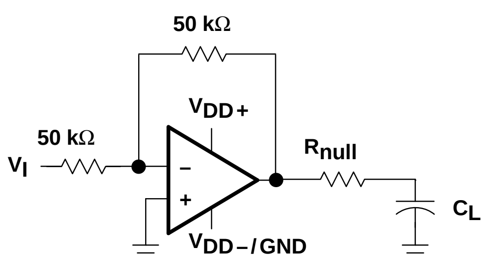


Figure 56. Series-Resistance Circuit

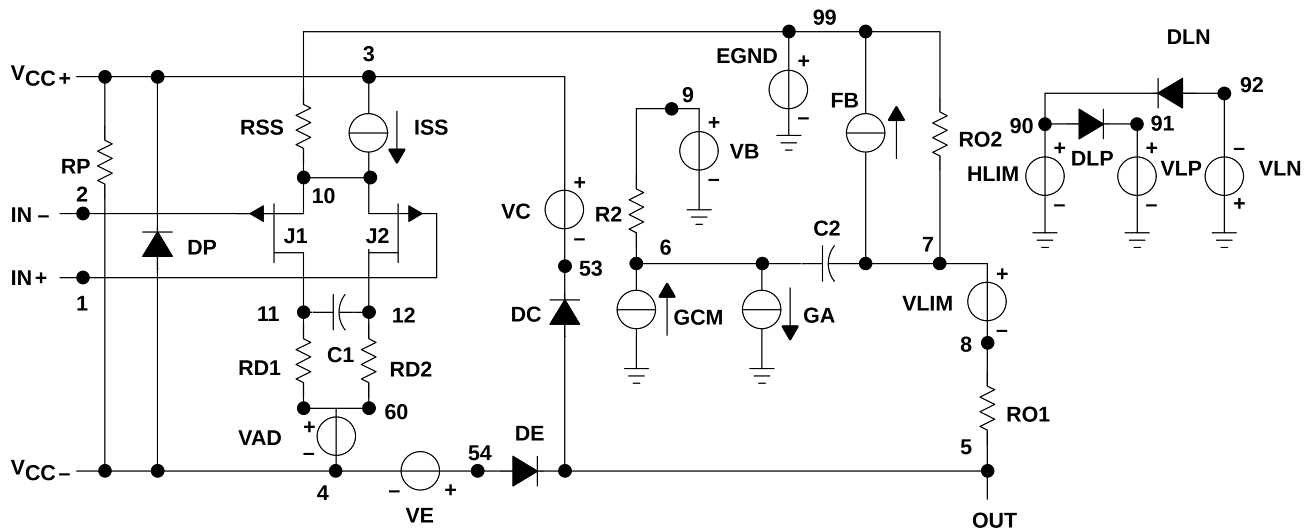
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 57 are generated using the TLC2252 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLC2252 1 2 3 4 5
  C1     11   12   6.369E–12
  C2     6    7    25.00E–12
  DC     5    53   DX
  DE     54   5    DX
  DLP    90   91   DX
  DLN    92   90   DX
  DP     4    3    DX
  EGND   99   0    POLY (2) (3,0) (4,0) 0 .5 .5
  FB     7    99   POLY (5) VB VC VE VLP
  + VLN 0 57.62E6 –60E6 60E6 60E6 –60E6
  GA     6    0    11   12 26.86E–6
  GCM    0    6    10   99 2.686E–9
  ISS    3    10   DC 3.1E–6
  HLIM   90   0    VLIM 1K
  J1     11   2    10 JX
  J2     12   1    10 JX
  R2     6    9    100.0E3
RD1    60   11   37.23E3
RD2    60   12   37.23E3
R01    8    5    84
R02    7    99   84
RP     3    4    71.43E3
RSS    10   99   64.52E6
VAD    60   4    –.5
VB     9    0    DC 0
VC     3    53   DC .605
VE     54   4    DC .605
VLIM   7    8    DC 0
VLP    91   0    DC –.235
VLN    0    92   DC 7.5
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=139E–6
+ VTO=–.05)
.ENDS
```

Figure 57. Boyle Macromodel and Subcircuit

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