- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 1 mA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C (TLC2264A)**
- **Macromodel Included**

description

The TLC2264 and TLC2264A are quadruple operational amplifiers manufactured using TI's Advanced LinCMOS™ process. These devices exhibit rail-to-rail output performance while having better input offset voltage and lower power dissipation levels than existing CMOS operational amplifiers. In addition, the noise performance (see Figure 1) has been dramatically increased for this class of low-power CMOS amplifier. Figure 1 depicts the low level of voltage noise for this CMOS amplifier, which has only 200 μA (typical) of supply current per amplifier. Also, the common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ±5 mV. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

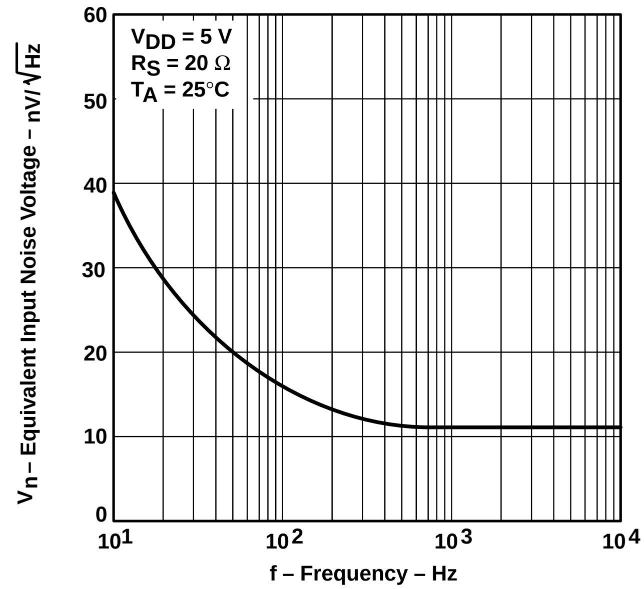


Figure 1

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)	
0°C to 70°C	2.5 mV	TLC2264CD	—	—	TLC2264CN	TLC2264CPWLE	—	TLC2262Y
–40°C to 125°C	950 μV 2.5 mV	TLC2264AID TLC2264ID	— —	— —	TLC2264AIN TLC2264IN	TLC2264AIPWLE —	— —	
–55°C to 125°C	950 μV 2.5 mV	— —	TLC2264AMFK TLC2264MFK	TLC2264AMJ TLC2264MJ	— —	— —	TLC2264AMW TLC2264MW	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2264CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

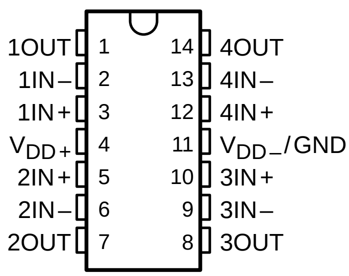
Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

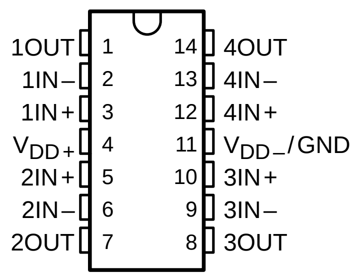
The TLC2264 and TLC2264A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the low-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices excellent choices when interfacing directly to analog-to-digital converters (ADCs). All of these features, combined with its temperature performance, make the TLC2264 family ideal for sonobuoys, remote pressure sensors, temperature control, active voltage-resistive (VR) sensors, accelerometers, portable medical applications, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Exercise care in handling these devices, as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply line transients under powered conditions. Transients greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

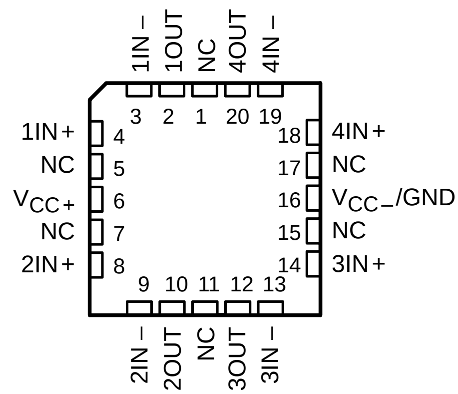
TLC2264C, TLC2264AC
TLC2264I, TLC2264AI
D, N, OR PW PACKAGE
(TOP VIEW)



TLC2264M, TLC2264AM . . . J OR W PACKAGE
(TOP VIEW)



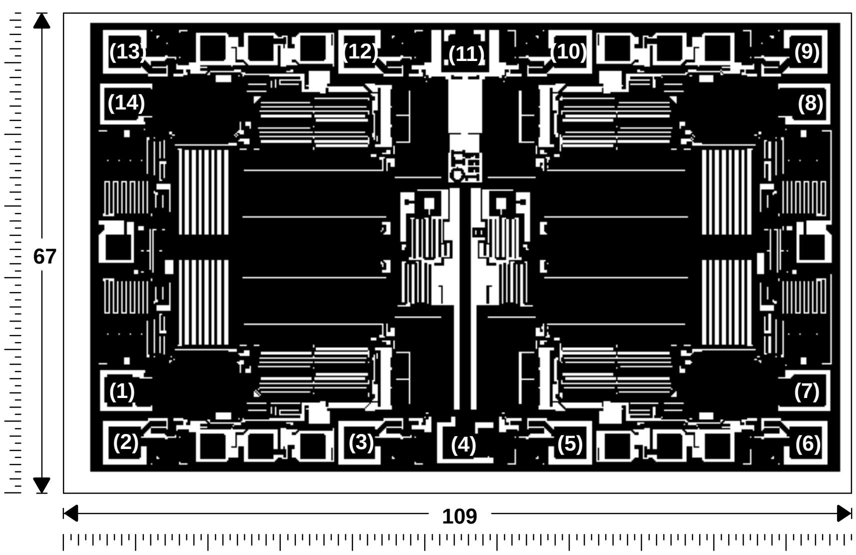
TLC2264M, TLC2264AM . . . FK PACKAGE
(TOP VIEW)

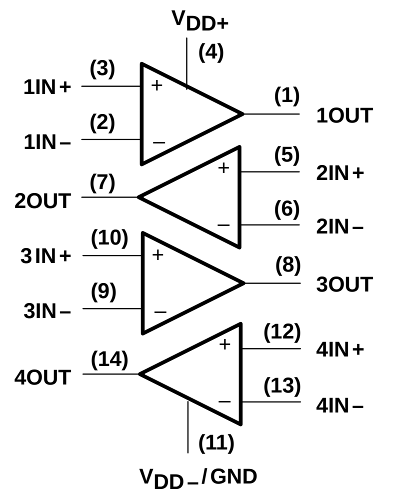


TLC2264Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2264C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

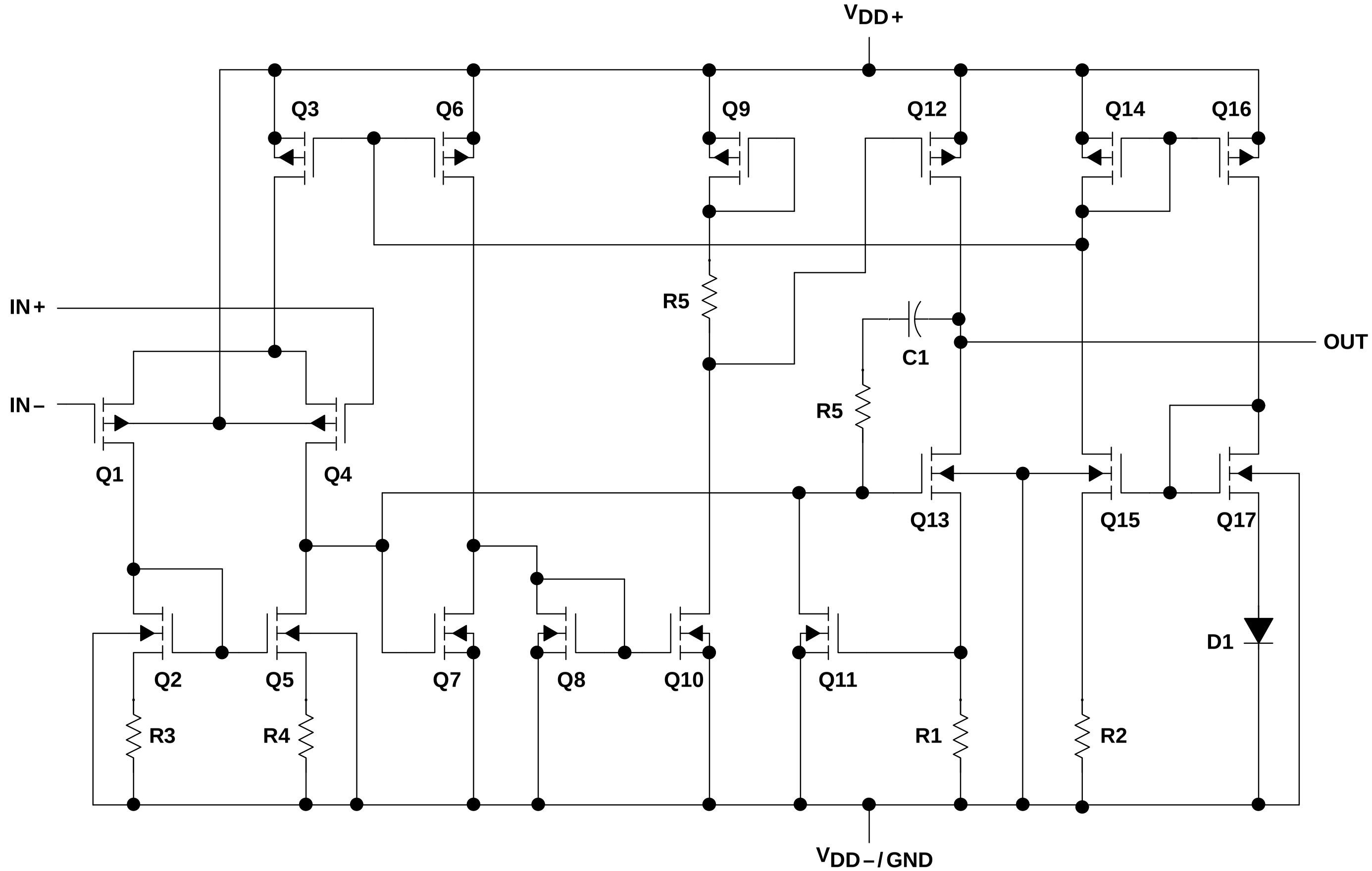
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	76
Diodes	18
Resistors	56
Capacitors	6

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1) . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . –8 V
Differential input voltage, V_{ID} (see Note 2) . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . V_{DD-} –0.3 V to V_{DD+}
Input current, I_I (each input) . . . ±5 mA
Output current, I_O . . . ±50 mA
Total current into V_{DD+} . . . ±50 mA
Total current out of V_{DD-} . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . unlimited
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . 0°C to 70°C
I suffix . . . –40°C to 125°C
M suffix . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, and PW packages . . . 260°C
FK, J, and W packages . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows when input is brought below V_{DD-} – 0.3 V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	190 mW
FK	1375 mW	11.0 mW/°C	—	275 mW
J	1375 mW	11.0 mW/°C	—	275 mW
N	1150 mW	9.2 mW/°C	736 mW	230 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW
W	700 mW	5.5 mW/°C	—	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V_{DD-}	V_{DD+} –1.5	V
Operating free-air temperature, T_A	0	70	–40	125	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, $V_{DD\pm}$ = ±2.5 V, V_O = 0, R_S = 50 Ω	25°C		300	2500	μV
			Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99		V
		I_{OH} = −100 μA	25°C	4.85	4.94		
			Full range	4.82			
		I_{OH} = −400 μA	25°C	4.70	4.85		
			Full range	4.60			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15	
			Full range			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3	
			Full range			0.3	
		V_{IC} = 2.5 V, I_{OL} = 4 mA	25°C		0.7	1	
			Full range			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 50 kΩ‡	25°C	80	170		V/mV
			Full range	55			
		V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 MΩ‡	25°C		550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		dB
			Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		dB
			Full range	80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	25°C		0.8	1	mA
			Full range			1	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4		µs
			To 0.01%			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	$V_O = 0$,	25°C		300	2500	μV
				Full range			3000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			100	
I_{IB}	Input bias current			25°C		1		pA
				Full range			100	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	$R_S = 50\ \Omega$	25°C	−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$		25°C		4.99		V
		$I_O = -100\ \mu A$		25°C	4.85	4.94		
				Full range	4.82			
		$I_O = -400\ \mu A$		25°C	4.7	4.85		
				Full range	4.6			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_O = 50\ \mu A$	25°C		−4.99		V
		$V_{IC} = 0$,	$I_O = 500\ \mu A$	25°C	−4.85	−4.91		
				Full range	−4.85			
		$V_{IC} = 0$,	$I_O = 1$ mA	25°C	−4.7	−4.8		
				Full range	−4.7			
		$V_{IC} = 0$,	$I_O = 4$ mA	25°C	−4	−4.3		
				Full range	−3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 50\ k\Omega$	25°C	80	200		V/mV
				Full range	55			
			$R_L = 1\ M\Omega$	25°C		1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$	25°C		220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$,	$R_S = 50\ \Omega$	25°C	75	88		dB
				Full range	75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = 0$,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$,	No load	25°C		0.85	1	mA
				Full range			1	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264C MIN	TLC2264C TYP	TLC2264C MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 1.9$ V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		V/µs
				Full range	0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, f = 20 kHz, R_L = 50 kΩ	A_V = 1	25°C		0.014%		
			A_V = 10			0.024%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		70		kHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1		µs
			To 0.01%			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°		
	Gain margin			25°C		11		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264I			TLC2264AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20$ µA	25°C		4.99			4.99		V
		$I_{OH} = -100$ µA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_{OH} = -400$ µA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50$ µA	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V, $I_{OL} = 500$ µA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 4$ mA	25°C		0.8	1		0.7	1	
			Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 50$ kΩ‡	25°C	80	100		80	170		V/mV
			Full range	50			50			
		$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 1$ MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5$ V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264I			TLC2264AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2		V
			Full range	–5 to 3.5			–5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$	25°C		4.99			4.99		V
		$I_O = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		–4.99			–4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	–4.85	–4.91		–4.85	–4.91		
			Full range	–4.85			–4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	–4	–4.3		–4	–4.3		
			Full range	–3.8			–3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 50\ k\Omega$	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$V_O = \pm 4$ V, $R_L = 1\ M\Omega$	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.85	1		0.85	1	mA
			Full range			1			1	

† Full range is – 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264I			TLC2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9$ V, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3$ V, $R_L = 50$ kΩ, f = 20 kHz	$A_V = 1$	25°C		0.014%			0.014%		
			$A_V = 10$			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, $C_L = 100$ pF	$R_L = 50$ kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $R_L = 50$ kΩ,	$A_V = 1$, $C_L = 100$ pF	25°C		70			70		kHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, $R_L = 50$ kΩ, $C_L = 100$ pF	To 0.1%	25°C		7.1			7.1		μs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50$ kΩ,	$C_L = 100$ pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264M			TLC2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu A$	25°C		4.99			4.99		V
		$I_{OH} = -100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_{OH} = -400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 50\ \mu A$	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V, $I_{OL} = 500\ \mu A$	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		$V_{IC} = 2.5$ V, $I_{OL} = 4$ mA	25°C		0.8	1		0.7	1	
			Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 50\ k\Omega$‡	25°C	80	100		80	170		V/mV
			Full range	50			50			
		$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 1\ M\Omega$‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5$ V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264M			TLC2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 55°C to 125°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2264M			TLC2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		300	2500		300	950	µV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			125°C			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			125°C			500			500	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO} \rvert \le 5$ mV	25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2		V
			Full range	–5 to 3.5			–5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_O = –20\ \mu A$	25°C		4.99			4.99		V
		$I_O = –100\ \mu A$	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		$I_O = –400\ \mu A$	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
$V_{OM–}$	Maximum negative peak output voltage	$V_{IC} = 0$, $I_O = 50\ \mu A$	25°C		–4.99			–4.99		V
		$V_{IC} = 0$, $I_O = 500\ \mu A$	25°C	–4.85	–4.91		–4.85	–4.91		
			Full range	–4.85			–4.85			
		$V_{IC} = 0$, $I_O = 4$ mA	25°C	–4	–4.3		–4	–4.3		
			Full range	–3.8			–3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4$ V, $R_L = 50\ k\Omega$	25°C	80	200		80	200		V/mV
			Full range	50			50			
		$V_O = \pm 4$ V, $R_L = 1\ M\Omega$	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, $A_V = 10$	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = –5$ V to 2.7 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	88		75	88		dB
			Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2$ V to ± 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	$V_O = 0$, No load	25°C		0.85	1		0.85	1	mA
			Full range			1			1	

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264M			TLC2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm2$ V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_O = \pm2.3$ V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		70			70		kHz
t_s	Settling time	$A_V = -1$, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		µs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −55°C to 125°C.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLC2264Y MIN	TLC2264Y TYP	TLC2264Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω			300	2500	µV
I_{IO}	Input offset current					0.5	100	pA
I_{IB}	Input bias current					1	100	pA
V_{ICR}	Common-mode input voltage range	| V_{IO} | ≤ 5 mV,	R_S = 50 Ω		0 to 4	–0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = –20 µA				4.99		V
		I_{OH} = –100 µA			4.85	4.94		
		I_{OH} = –400 µA			4.7	4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA			0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA			0.8	1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†		80	170		V/mV
			R_L = 1 MΩ†			550		
$r_{i(d)}$	Differential input resistance					10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance					10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V,	R_S = 50 Ω	70	83		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V,	V_{IC} = V_{DD}/2,	No load	80	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load			0.8	1	mA

† Referenced to 2.5 V

electrical characteristics at $V_{DD\pm} = \pm5$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLC2264Y MIN	TLC2264Y TYP	TLC2264Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$	$R_S = 50\ \Omega$,			300	2500	µV
I_{IO}	Input offset current	$V_{IC} = 0$, $V_O = 0$	$R_S = 50\ \Omega$,			0.5	100	pA
I_{IB}	Input bias current	$V_{IC} = 0$, $V_O = 0$	$R_S = 50\ \Omega$,			1	100	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	$R_S = 50\ \Omega$		−5 to 4	−5.3 to 4.2		V
V_{OM+}	Maximum positive peak output voltage	$I_O = -20\ \mu A$				4.99		V
		$I_O = -100\ \mu A$			4.85	4.94		
		$I_O = -400\ \mu A$			4.7	4.85		
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$,	$I_{OL} = 50\ \mu A$			−4.99		V
		$V_{IC} = 0$,	$I_{OL} = 500\ \mu A$		−4.85	−4.91		
		$V_{IC} = 0$,	$I_{OL} = 4$ mA		−3.8	−4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm4$ V	$R_L = 50\ k\Omega$		80	200		V/mV
			$R_L = 1\ M\Omega$			1000		
$r_{i(d)}$	Differential input resistance					10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance					10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V,	$V_O = 0$,	$R_S = 50\ \Omega$	75	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm2.2$ V to ±8 V,	$V_{IC} = 0$,	No load	80	95		dB
I_{DD}	Supply current (four amplifiers)	$V_O = 0$,	No load			0.85	1	mA

TYPICAL CHARACTERISTICS

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V_{OM-}	Maximum negative peak output voltage	vs Output current	15
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	16
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	17 18
V_O	Output voltage	vs Differential input voltage	19,20
	Differential gain	vs Load resistance	21
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	22, 23 24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	28 29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	30, 31 32
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	33 34
SR	Slew rate	vs Load capacitance vs Free-air temperature	35 36
V_O	Large-signal pulse response	vs Time	37, 38, 39, 40
V_O	Small-signal pulse response	vs Time	41, 42, 43, 44
V_n	Equivalent input noise voltage	vs Frequency	45, 46
	Input noise voltage	Over a 10-second period	47
	Integrated noise voltage	vs Frequency	48
THD + N	Total harmonic distortion plus noise	vs Frequency	49
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	50 51
ϕ_m	Phase margin	vs Frequency vs Load capacitance	22, 23 52
A_m	Gain margin	vs Load capacitance	53
B_1	Unity-gain bandwidth	vs Load capacitance	54
	Overestimation of phase margin	vs Load capacitance	55

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC2264
INPUT OFFSET VOLTAGE**

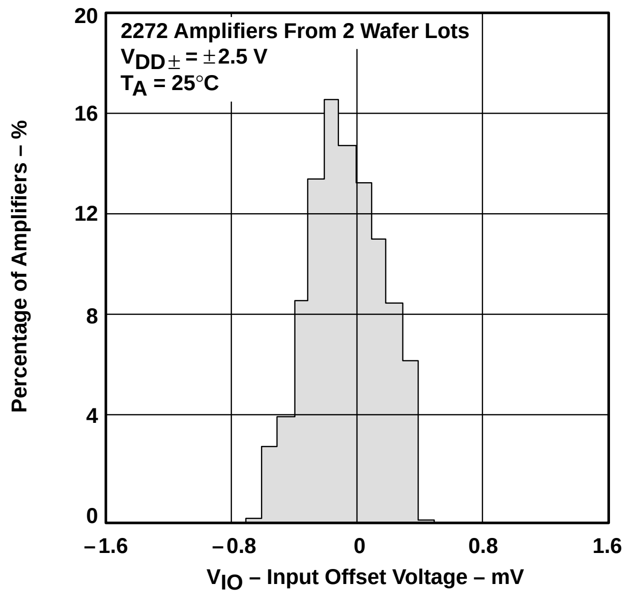


Figure 2

**DISTRIBUTION OF TLC2264
INPUT OFFSET VOLTAGE**

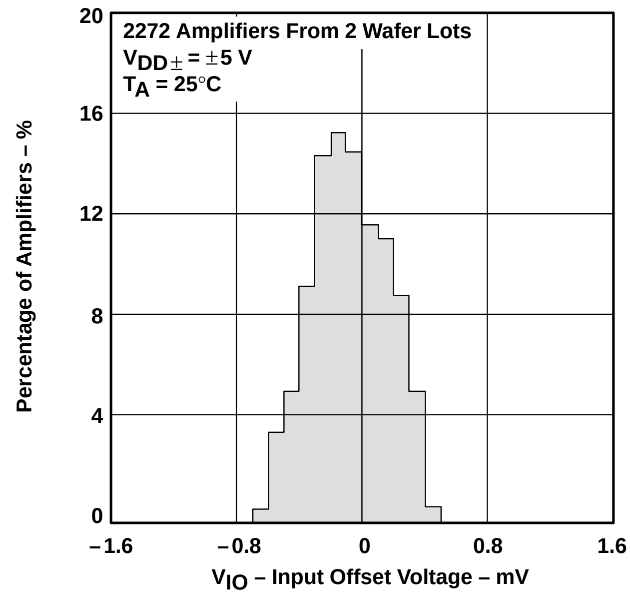


Figure 3

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

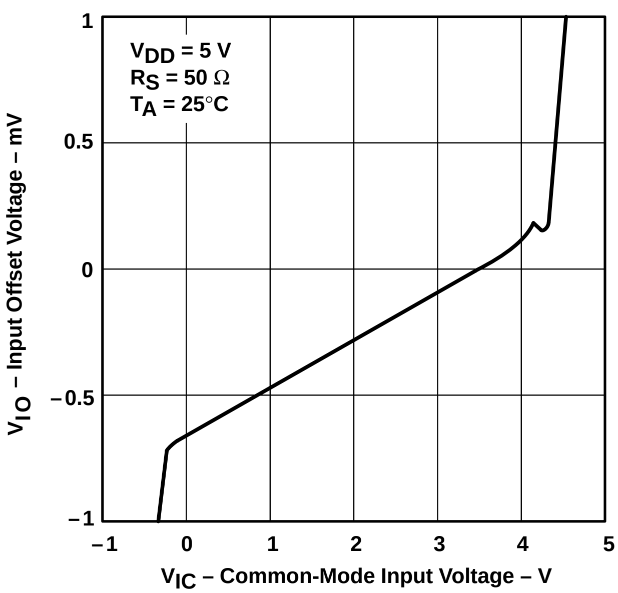


Figure 4

**INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

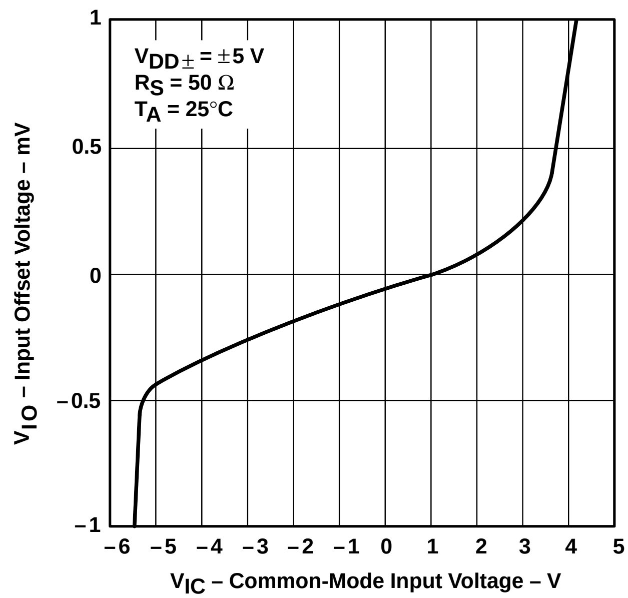


Figure 5

† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

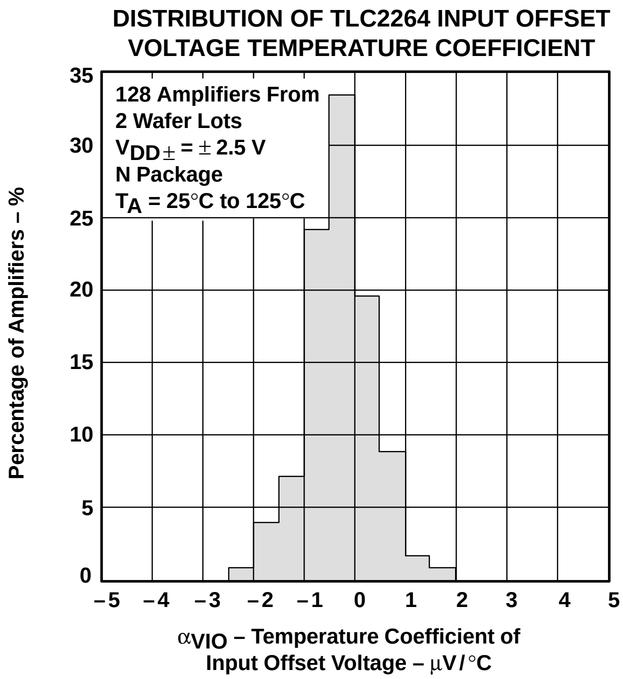


Figure 6

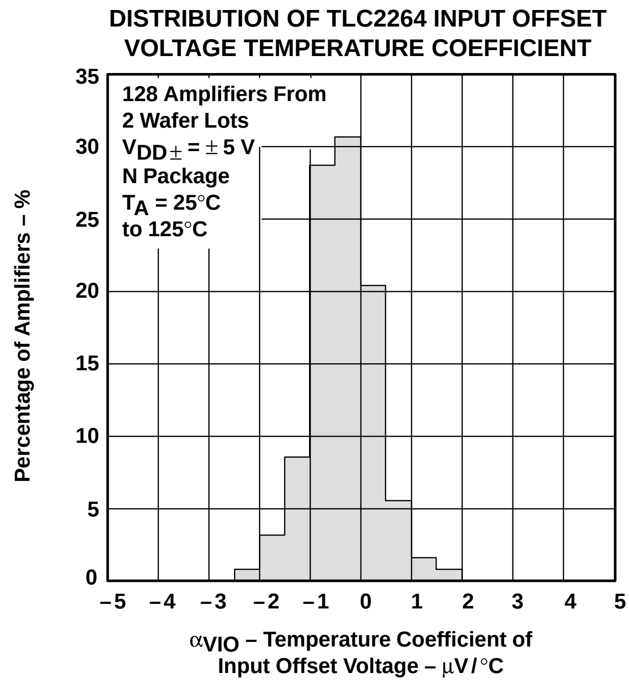


Figure 7

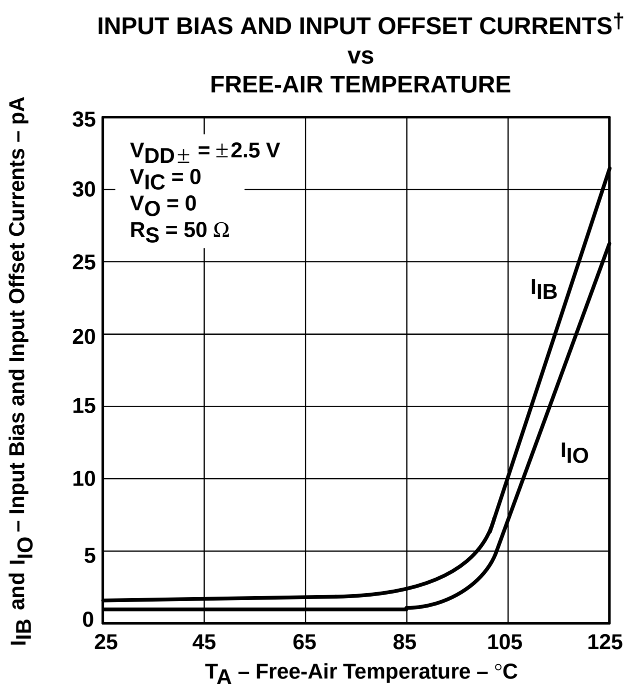


Figure 8

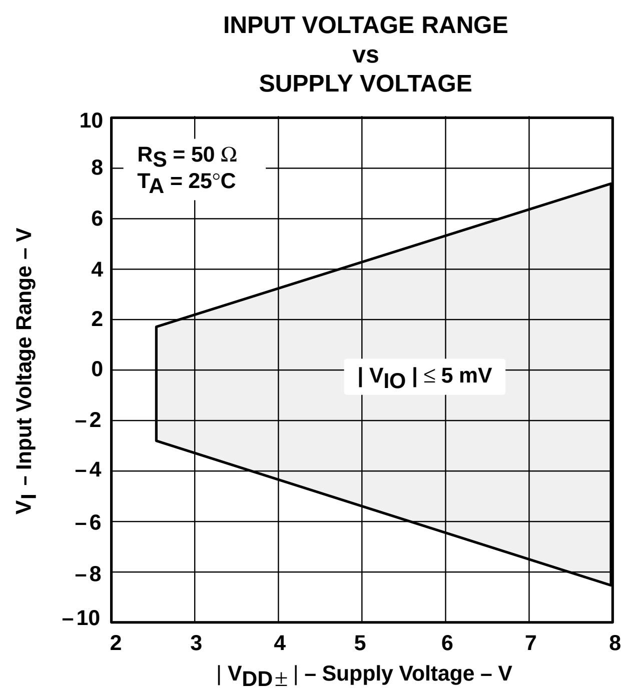


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

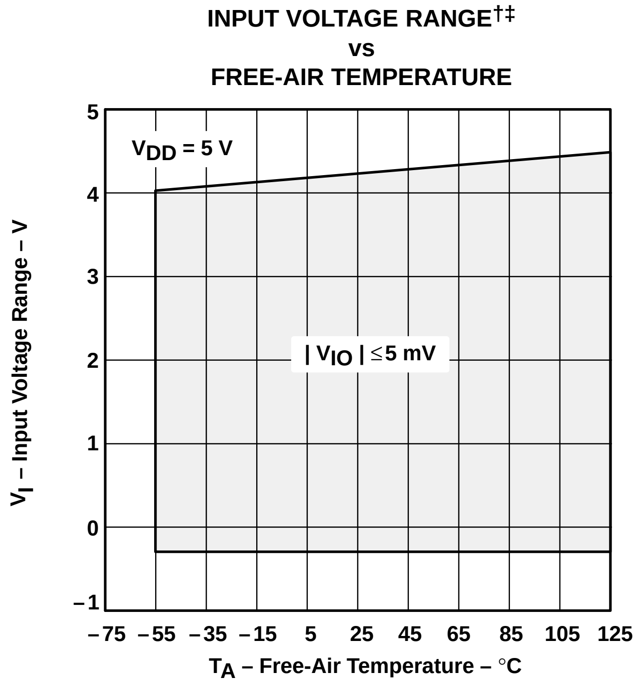


Figure 10

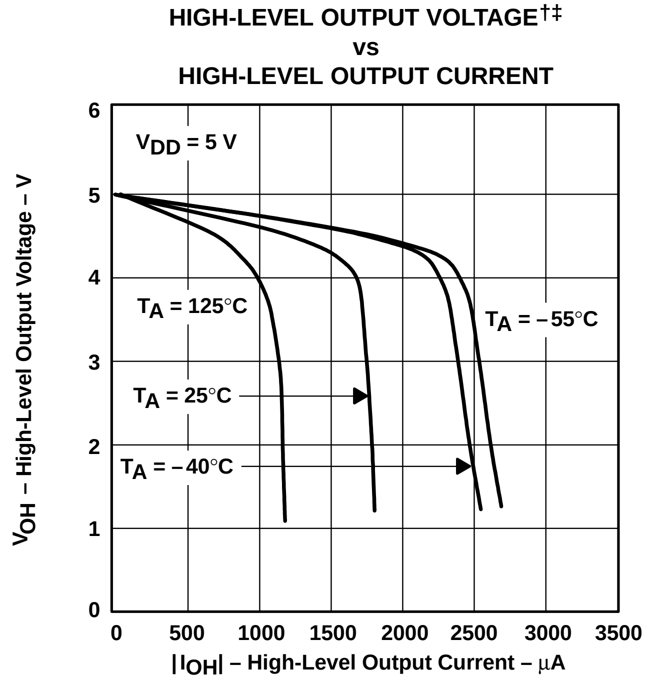


Figure 11

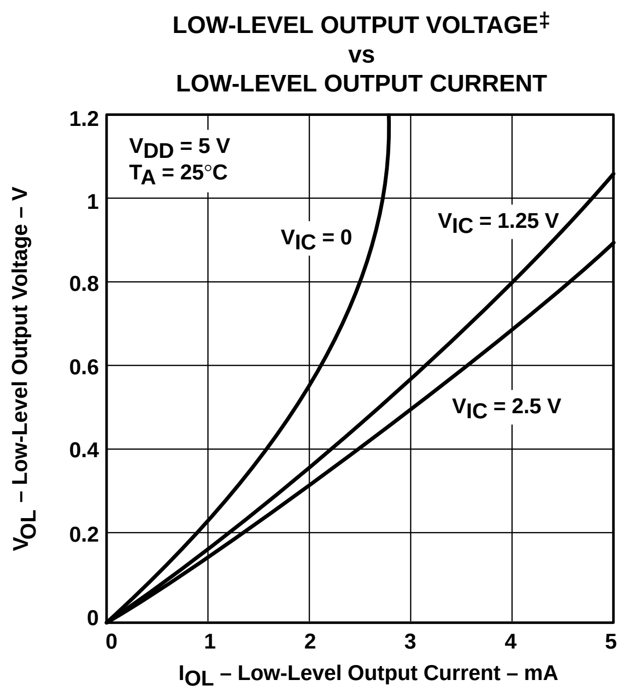


Figure 12

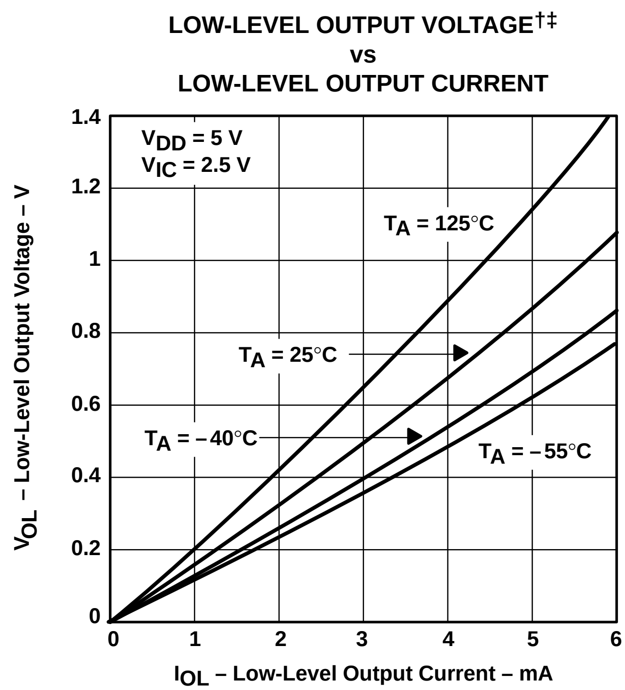


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE† vs OUTPUT CURRENT

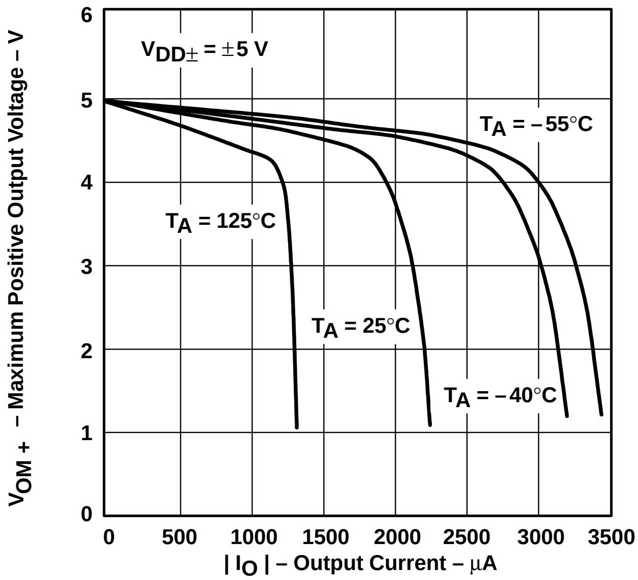


Figure 14

MAXIMUM NEGATIVE OUTPUT VOLTAGE† vs OUTPUT CURRENT

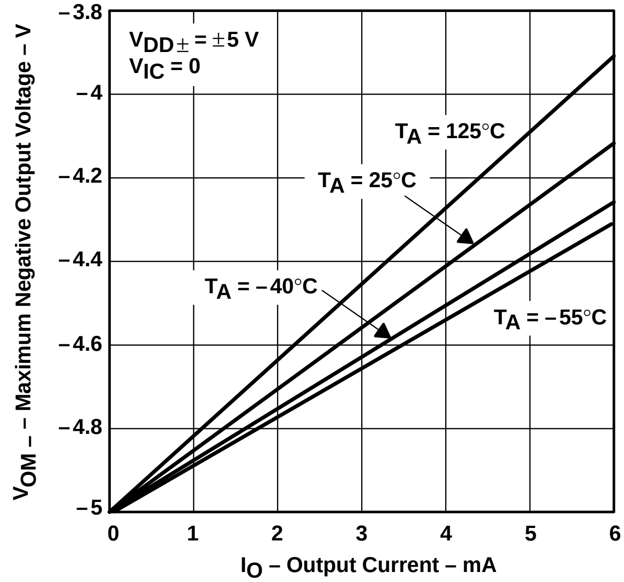


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡ vs FREQUENCY

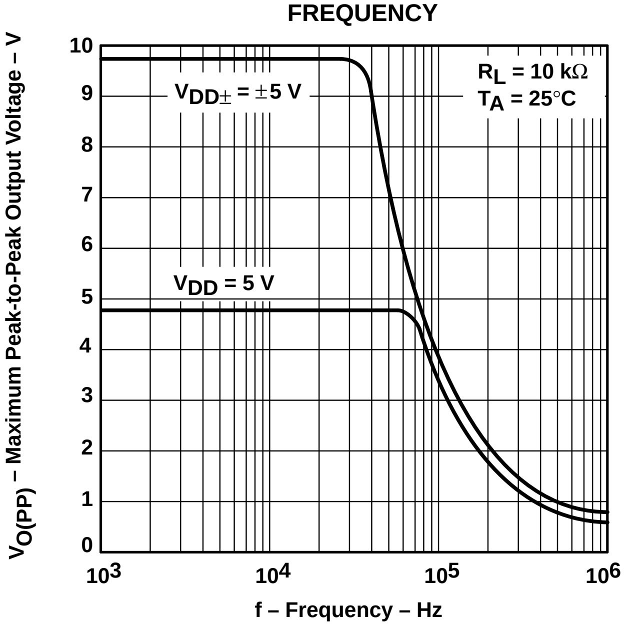


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

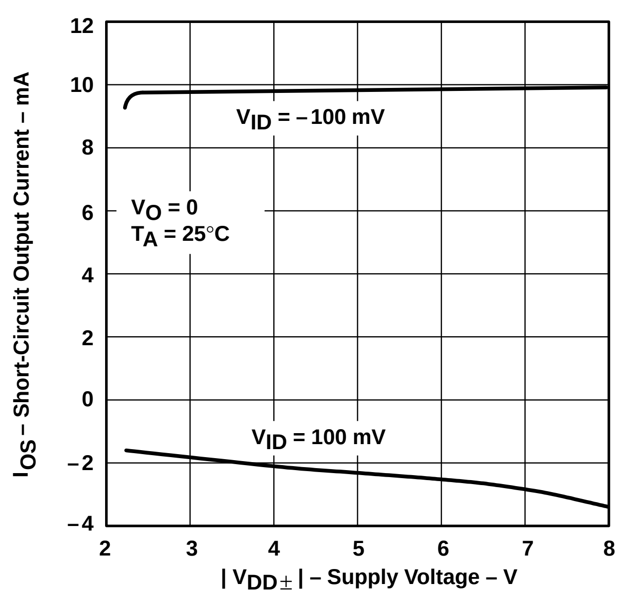


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

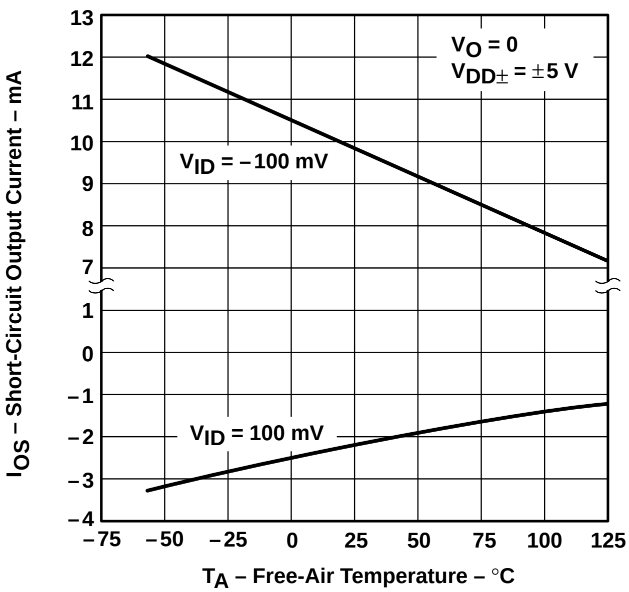


Figure 18

OUTPUT VOLTAGE‡ vs DIFFERENTIAL INPUT VOLTAGE

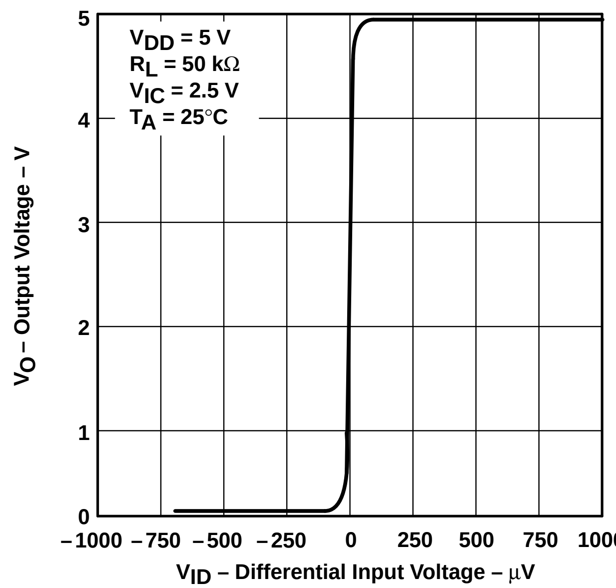


Figure 19

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

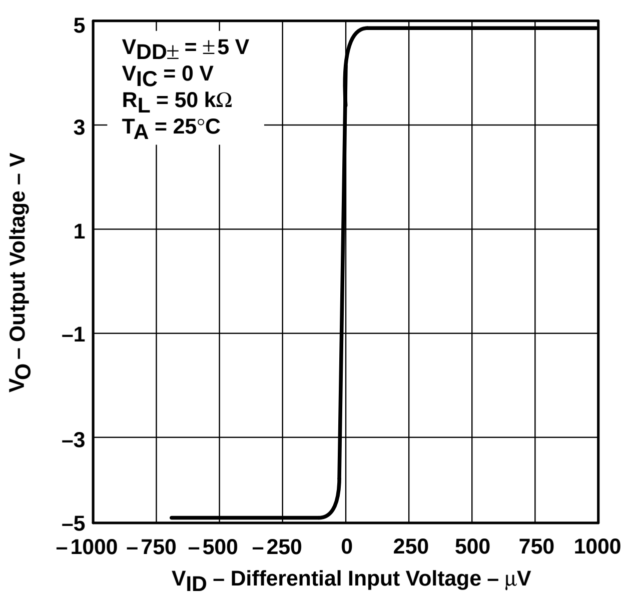


Figure 20

DIFFERENTIAL GAIN‡ vs LOAD RESISTANCE

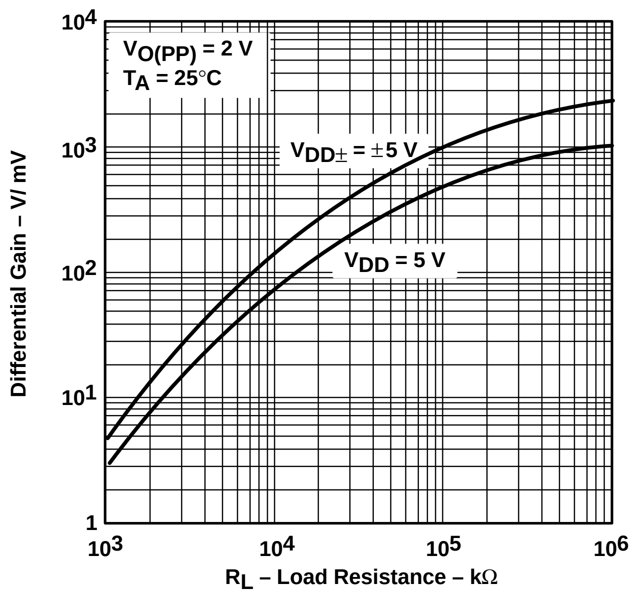
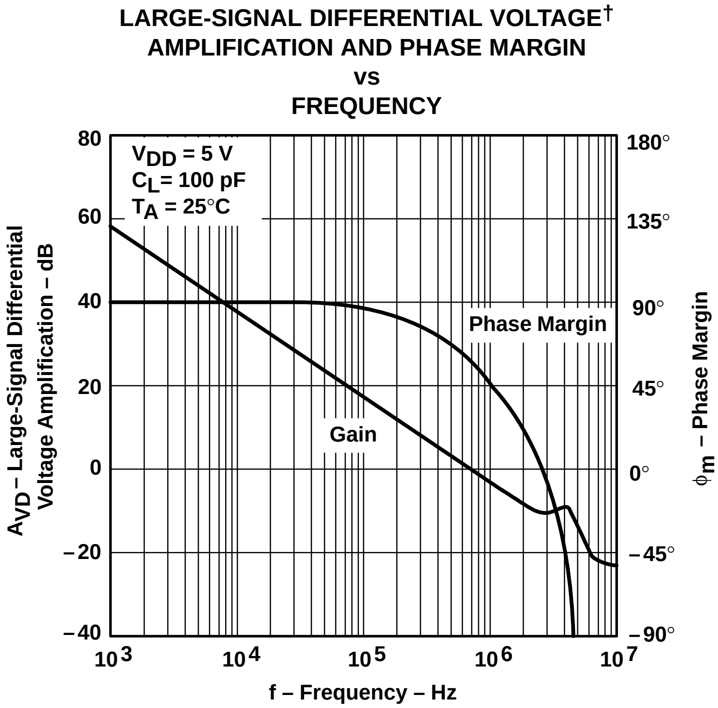


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 22

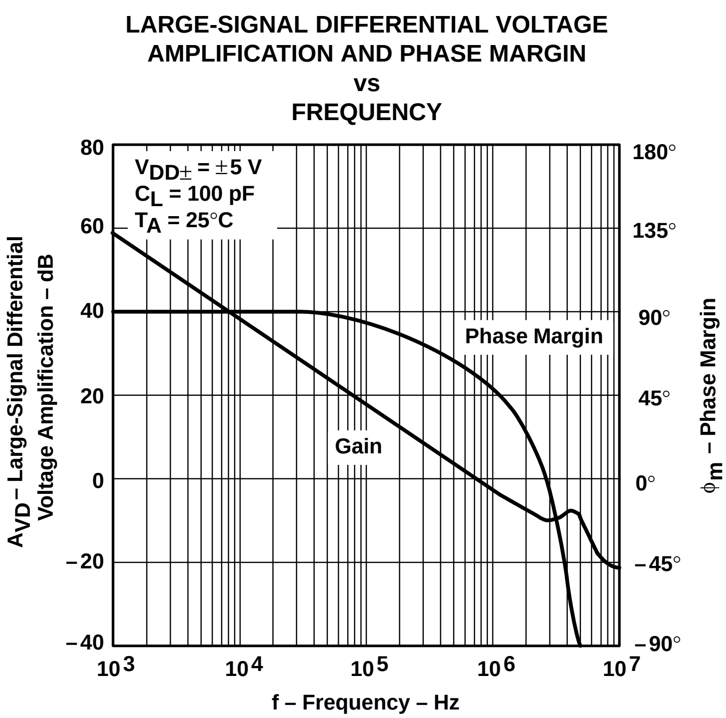


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL†‡ VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

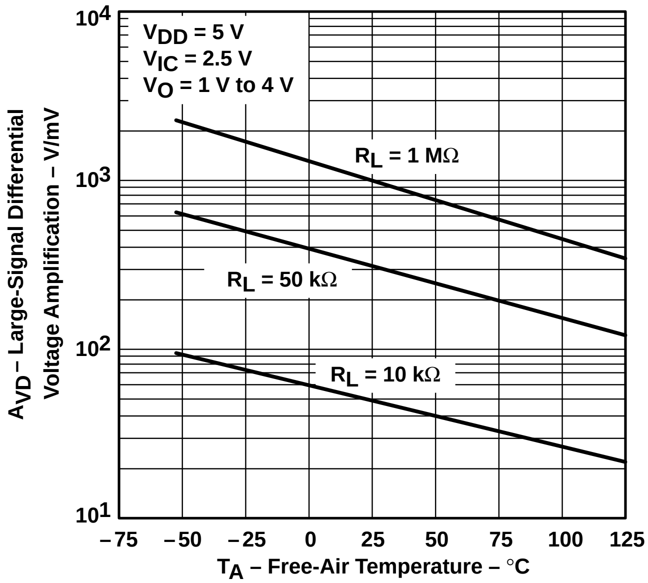


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

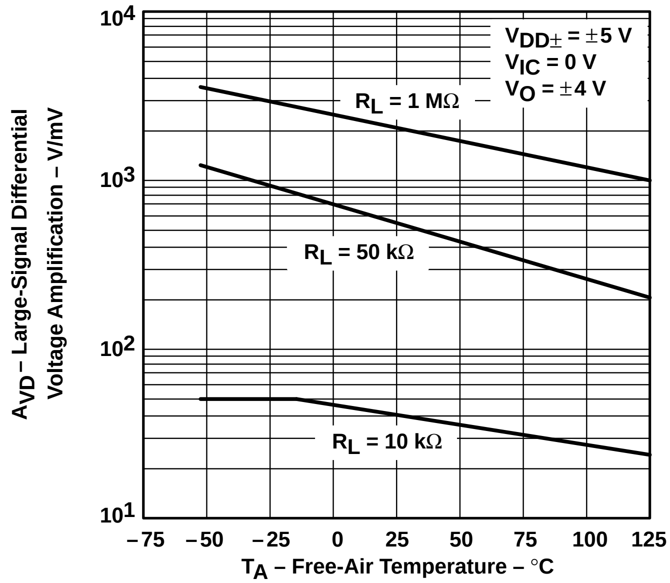


Figure 25

OUTPUT IMPEDANCE‡ vs FREQUENCY

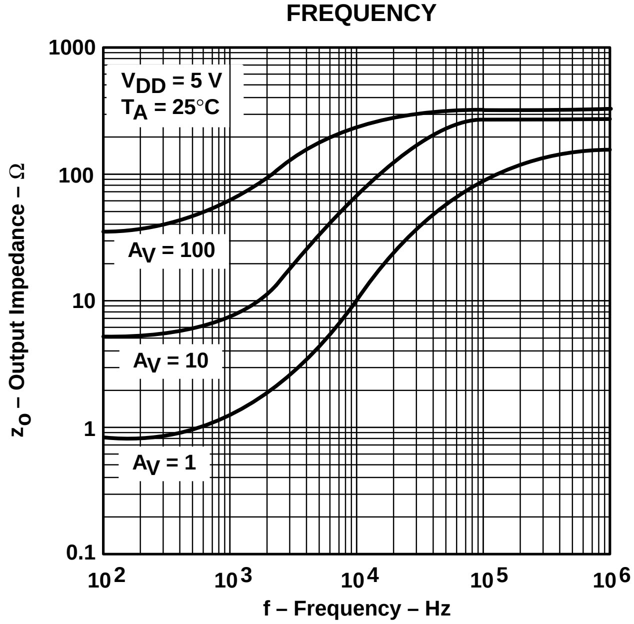


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

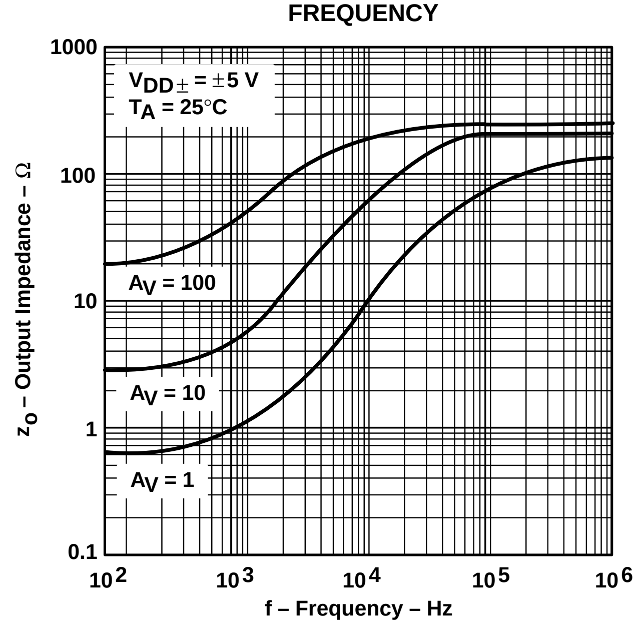


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

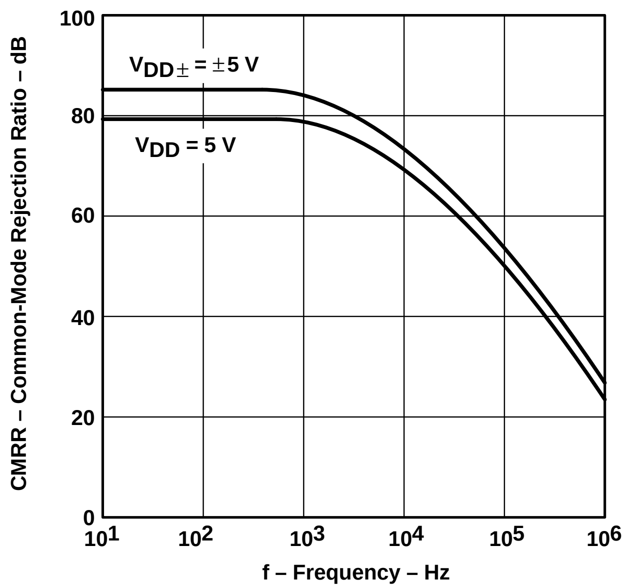


Figure 28

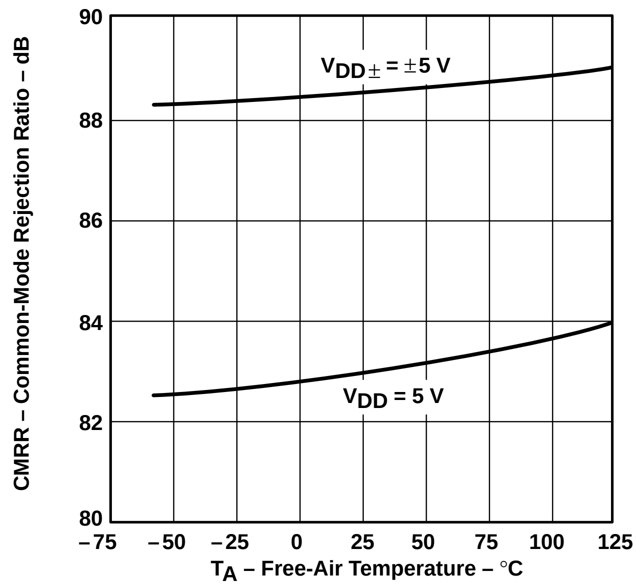


Figure 29

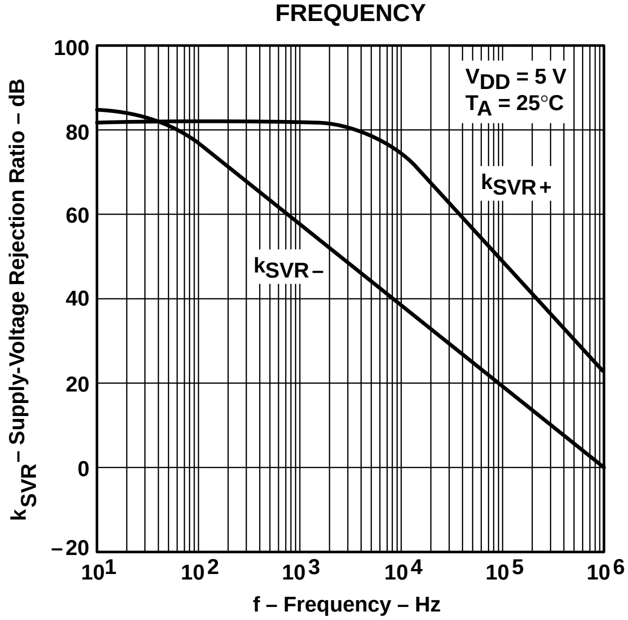


Figure 30

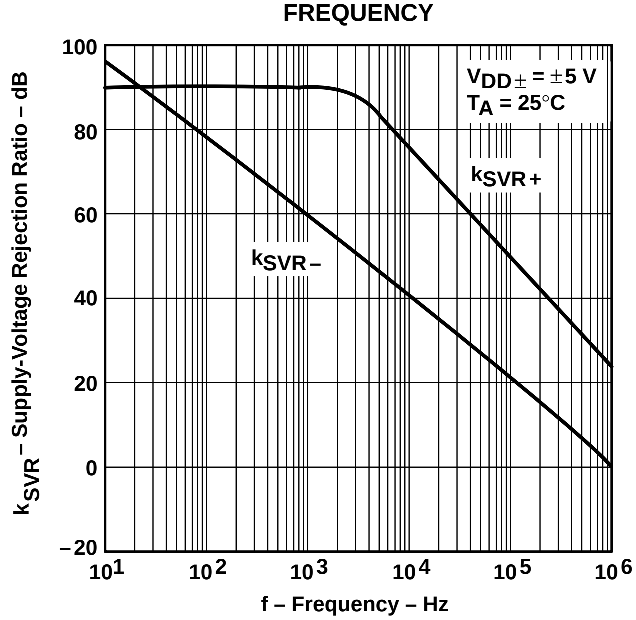


Figure 31

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V
‡ .Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

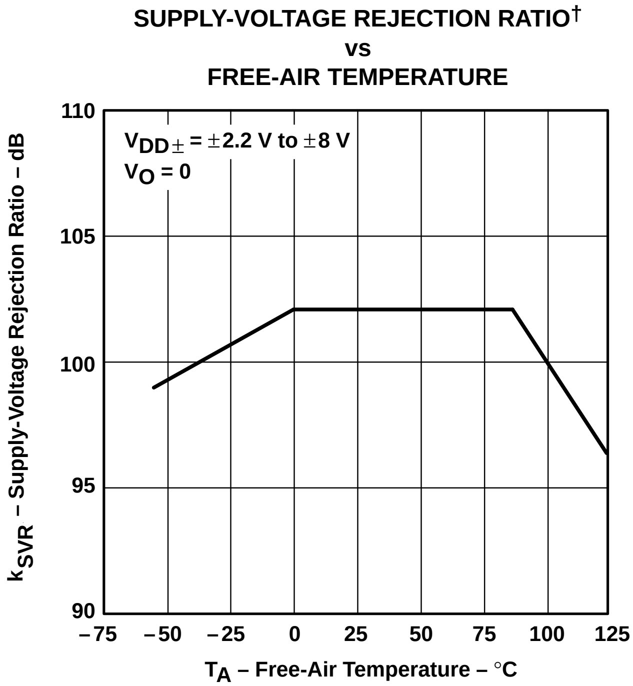


Figure 32

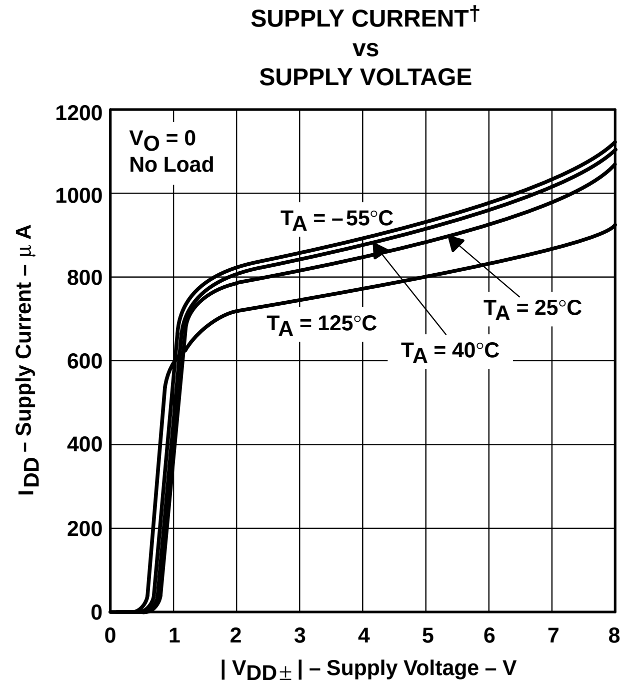


Figure 33

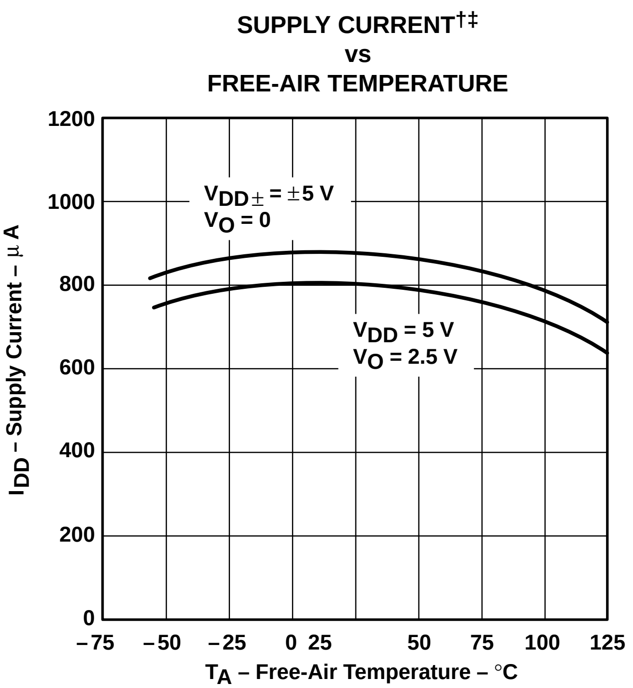


Figure 34

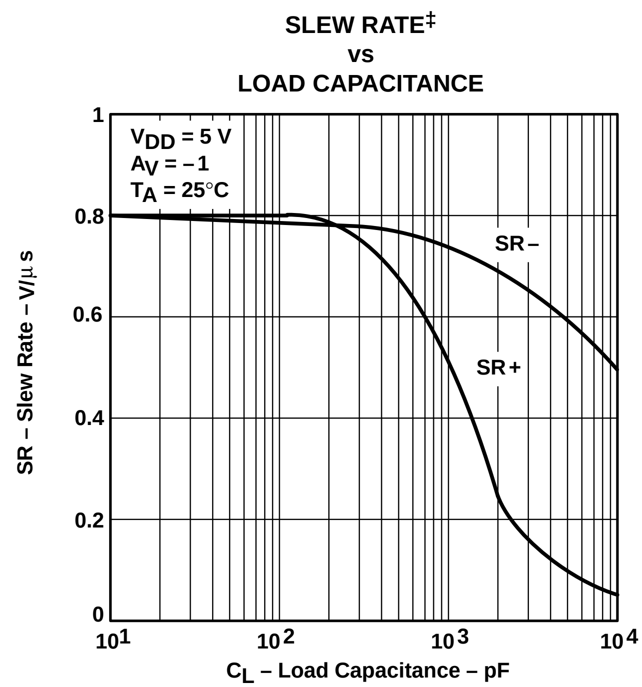


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS†

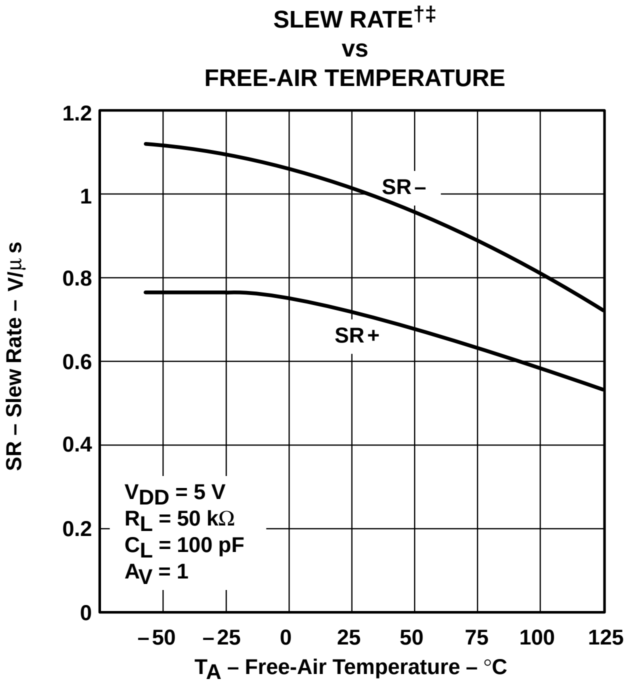


Figure 36

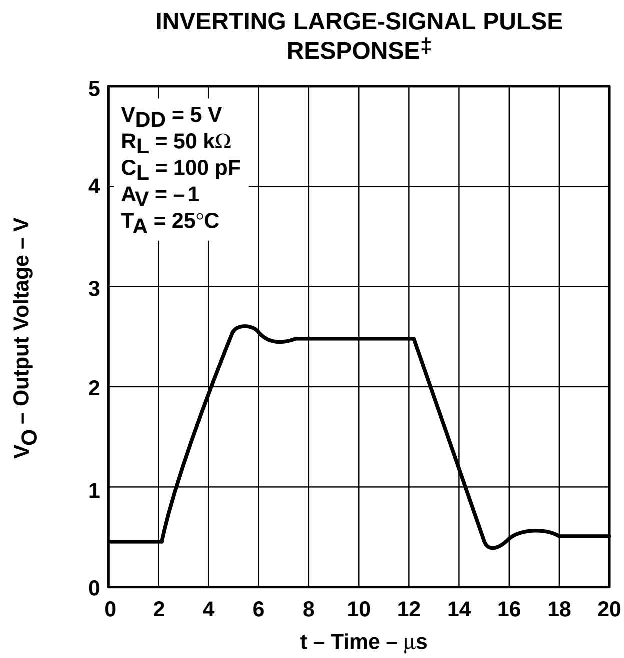


Figure 37

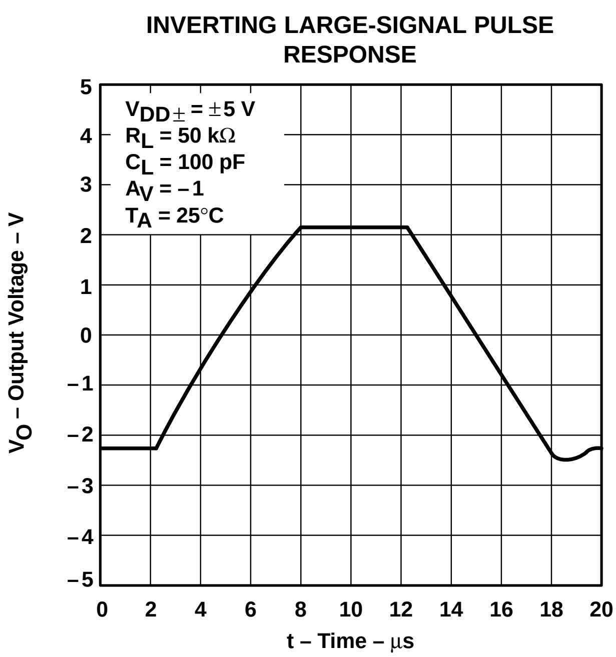


Figure 38

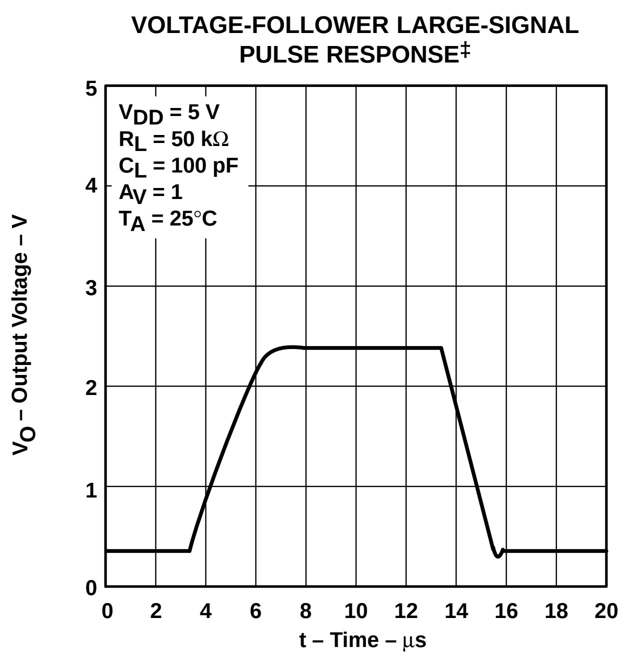


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

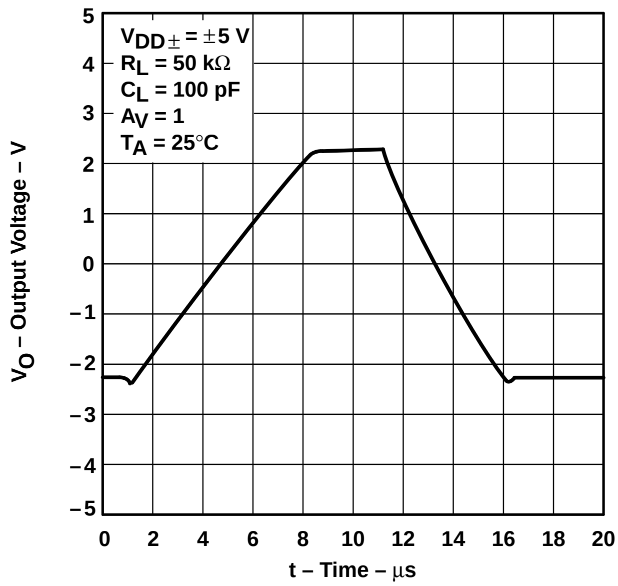


Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE†

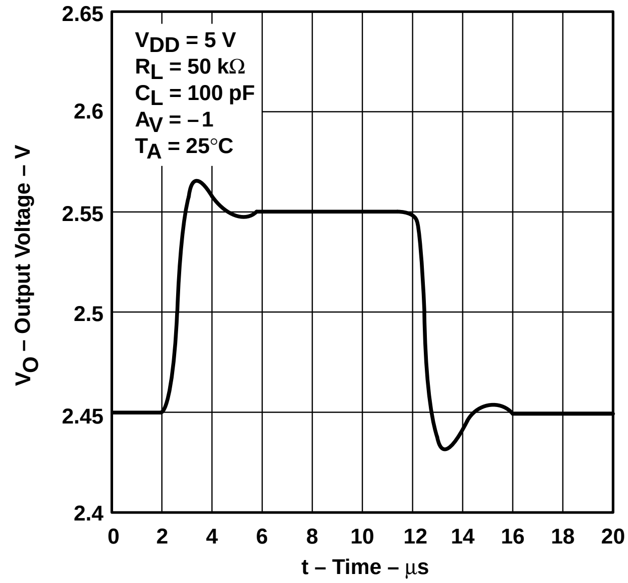


Figure 41

INVERTING SMALL-SIGNAL PULSE RESPONSE

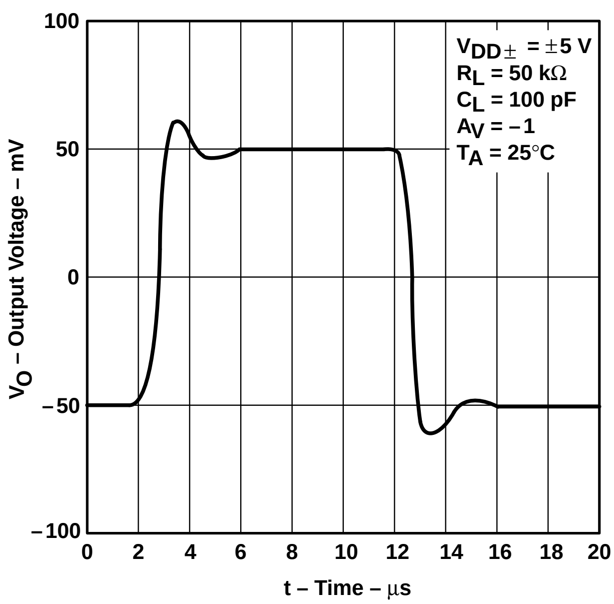


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

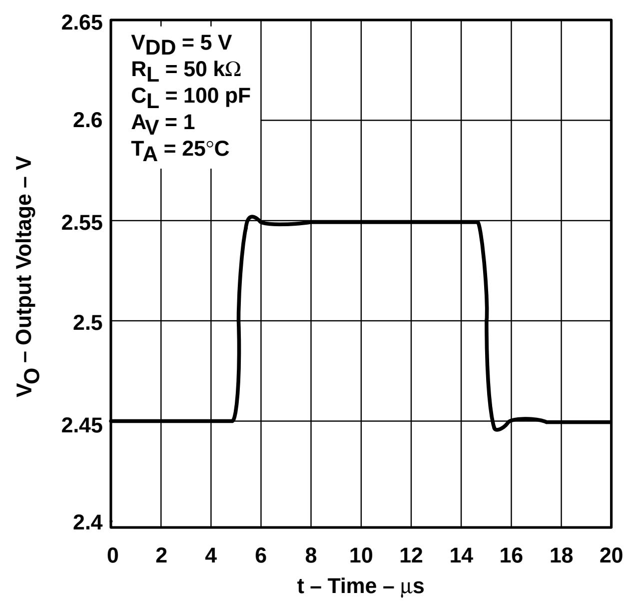


Figure 43

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

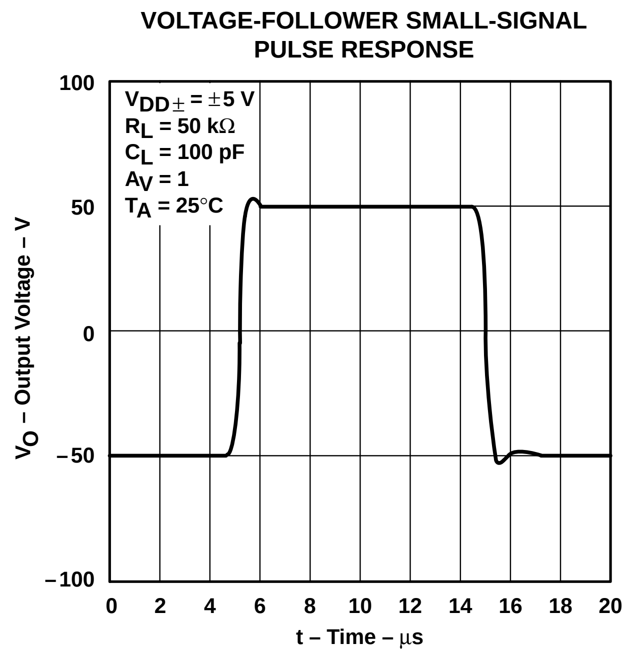


Figure 44

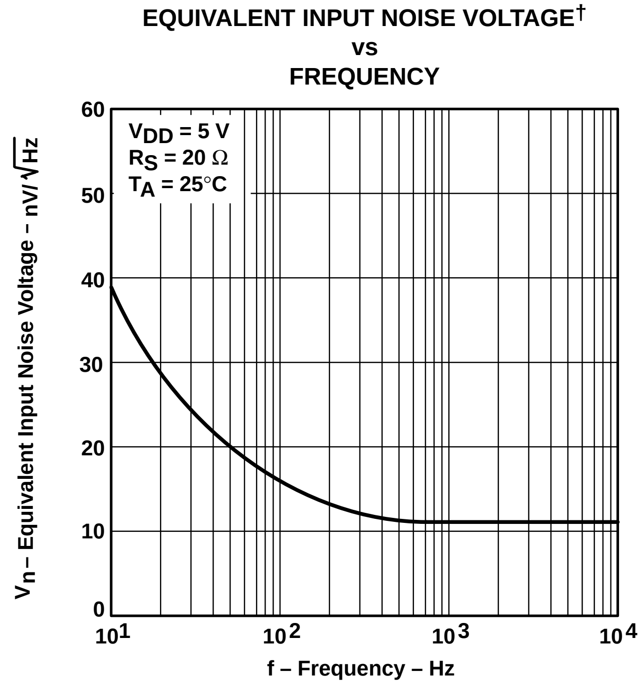


Figure 45

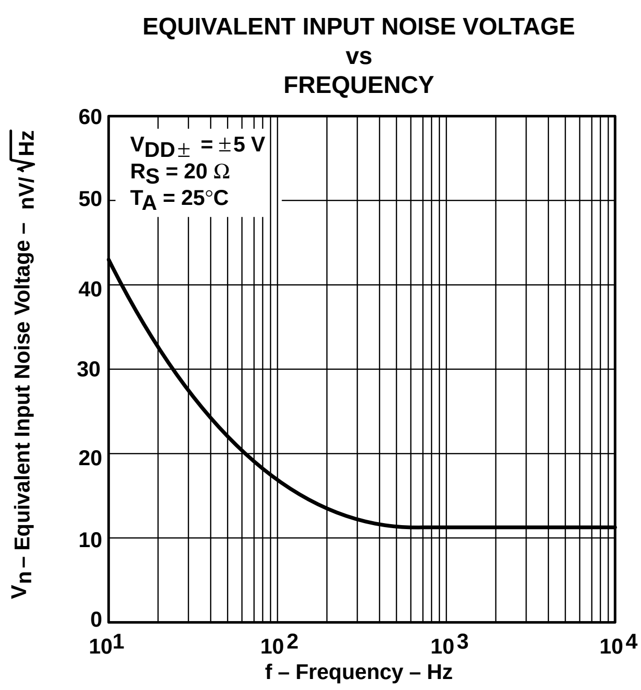


Figure 46

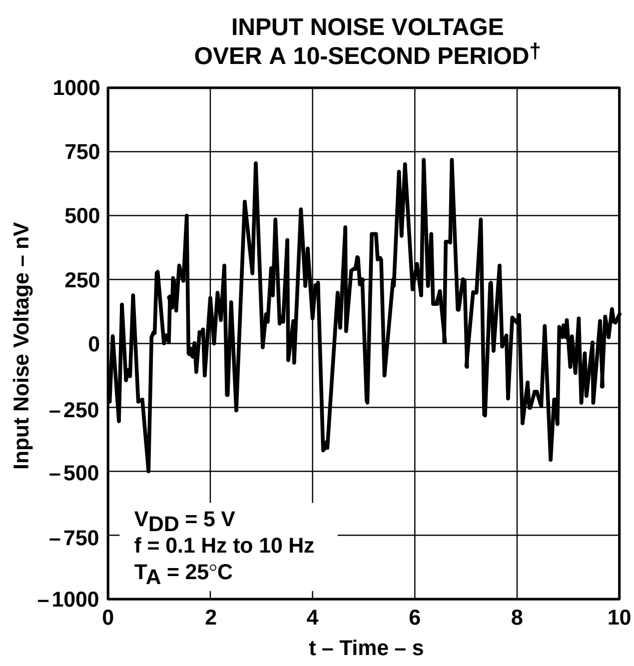


Figure 47

† For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

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TYPICAL CHARACTERISTICS†

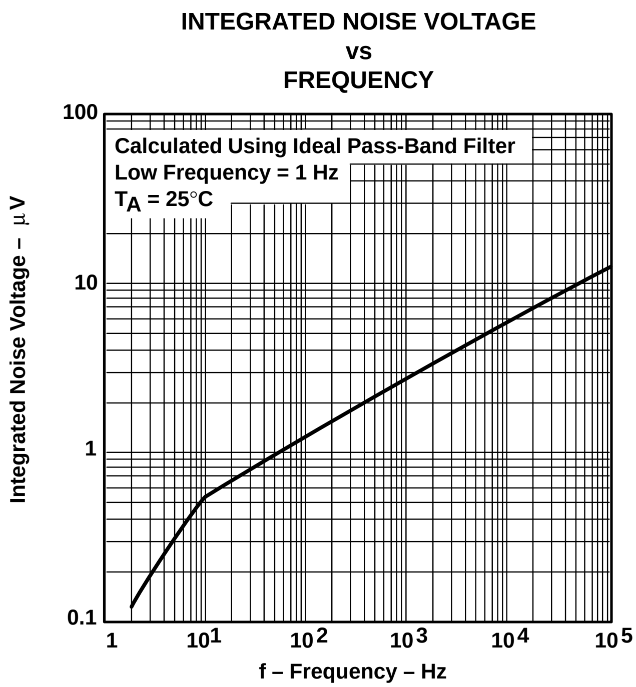


Figure 48

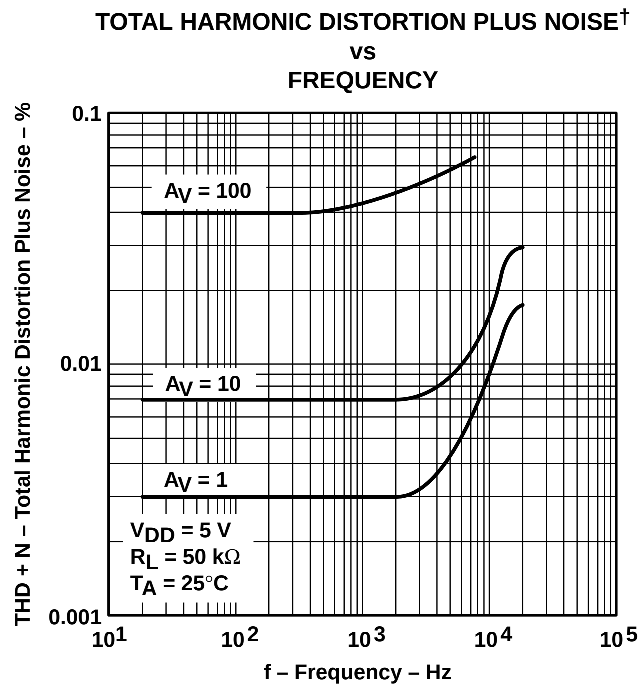


Figure 49

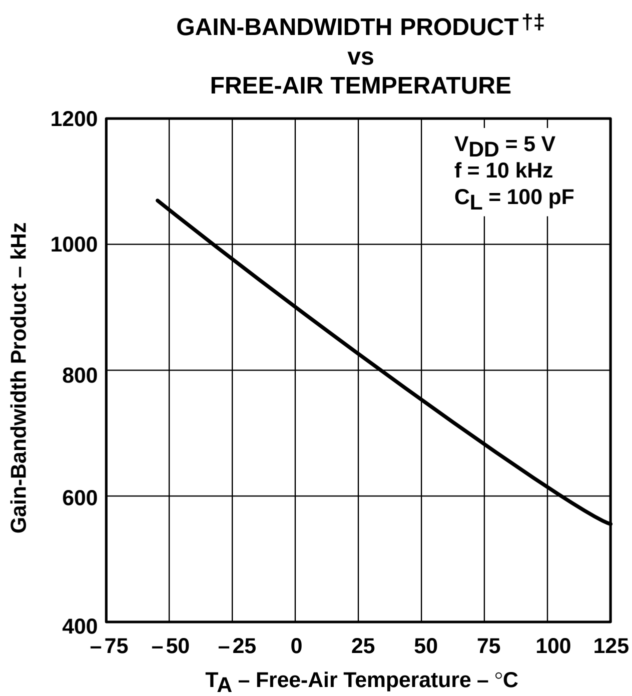


Figure 50

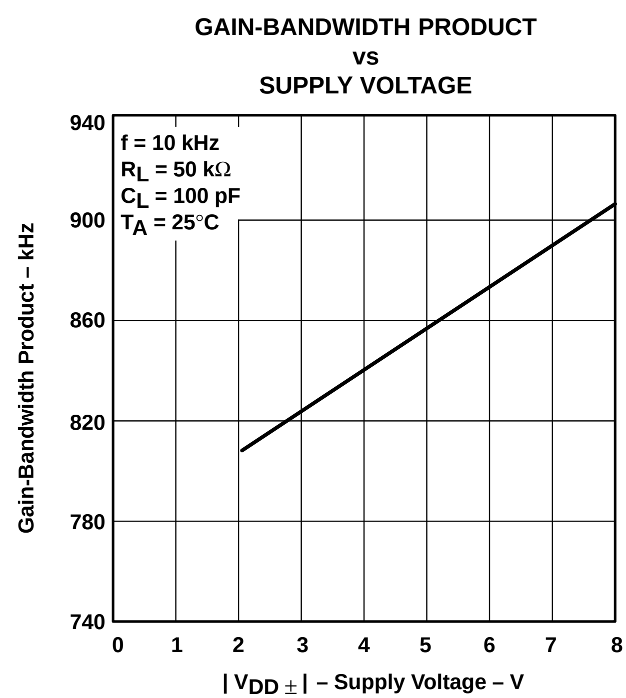


Figure 51

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

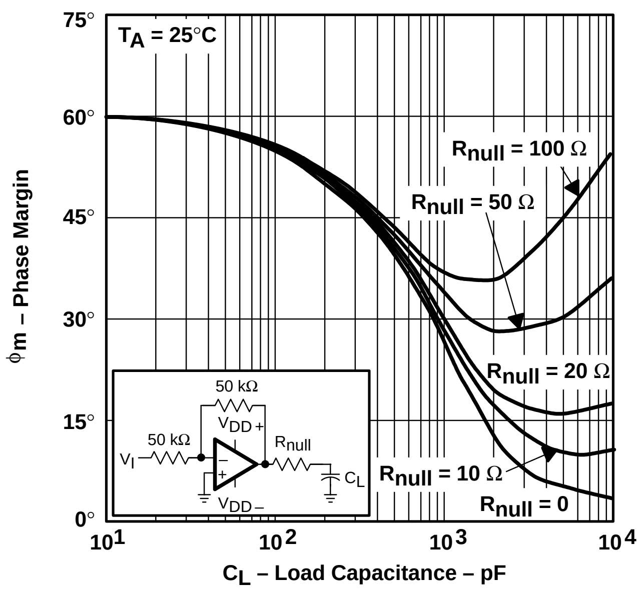


Figure 52

GAIN MARGIN vs LOAD CAPACITANCE

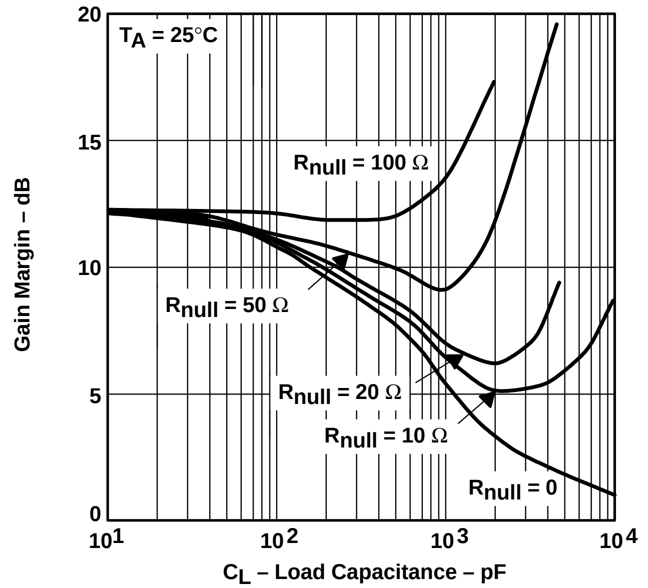


Figure 53

UNITY-GAIN BANDWIDTH† vs LOAD CAPACITANCE

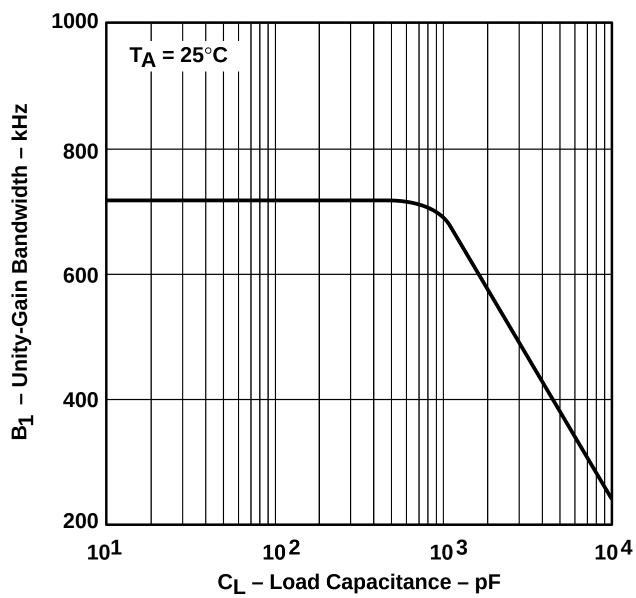


Figure 54

OVERESTIMATION OF PHASE MARGIN† vs LOAD CAPACITANCE

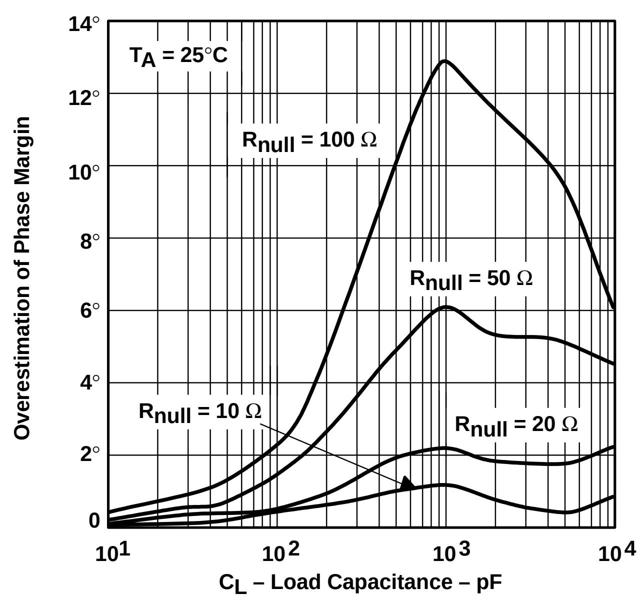


Figure 55

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC2264 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 52 and Figure 53 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 56) improves the gain and phase margins when driving large capacitive loads. Figure 52 and Figure 53 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function, and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance multiplied by the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\Theta_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \quad (1)$$

where:

$\Delta\Theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain-bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 54). To use equation (1), UGBW must be approximated from Figure 54.

Using equation (1) alone overestimates the improvement in phase margin as illustrated in Figure 55. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

where:

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

For the TLC2264, the pole associated with the load is typically 6 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 60 MHz, at C_L = 1000 pF, use 600 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone [equation (1)]. Equation (3) approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of equation (1) to better approximate the improvement in phase margin.

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\Theta_{m2} = \tan^{-1}\left[\frac{UGBW}{\left(F \times P_2\right)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \tag{3}$$

Where:

$\Delta\Theta_{m2}$ = reduction in phase margin
UGBW = unity-gain-bandwidth frequency
F = factor from equation (2)
P_2 = unadjusted pole (60 MHz @ 10 pF, 6 MHz @ 100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

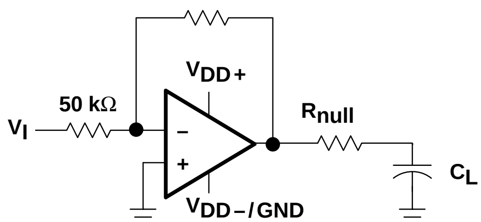


Figure 56. Series-Resistance Circuit

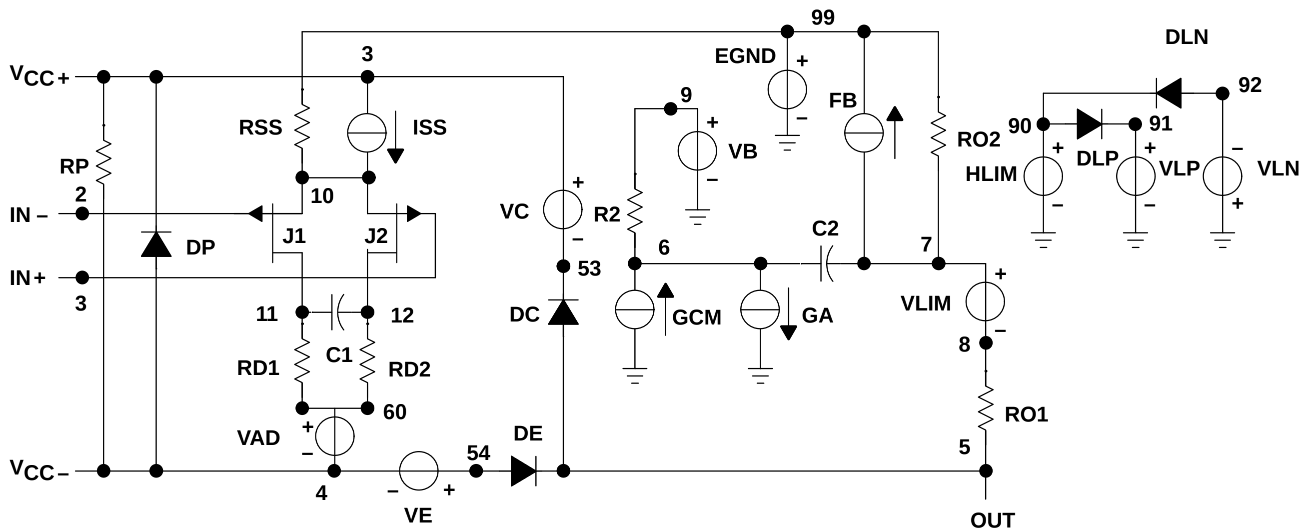
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 57 are generated using the TLC2264 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLC2262 1 2 3 4 5
         C1      11    12    3.560E–12
         C2      6     7     15.00E–12
         DC      5     53    DX
         DE      54    5     DX
         DLP     90    91    DX
         DLN     92    90    DX
         DP      4     3     DX
         EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
         FB      7     99    POLY (5) VB VC VE VLP
         + VLN 0 21.04E6 –30E6 30E6 30E6 –30E6
         GA      6     0     11    12 47.12E–6
         GCM     0     6     10    99 4.9E–9
         ISS     3     10    DC 8.250E–6
         HLIM    90    0     VLIM 1K
         J1      11    2     10 JX
         J2      12    1     10 JX
         R2      6     9     100.0E3
RD1      60    11    21.22E3
RD2      60    12    21.22E3
R01      8     5     120
R02      7     99    120
RP       3     4     26.04E3
RSS      10    99    24.24E6
VAD      60    4     –.6
VB       9     0     DC 0
VC       3     53    DC .65
VE       54    4     DC .65
VLIM     7     8     DC 0
VLP      91    0     DC 1.4
VLN      0     92    DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=281E–6
+ VTO=–.065)
.ENDS
```

Figure 57. Boyle Macromodel and Subcircuit

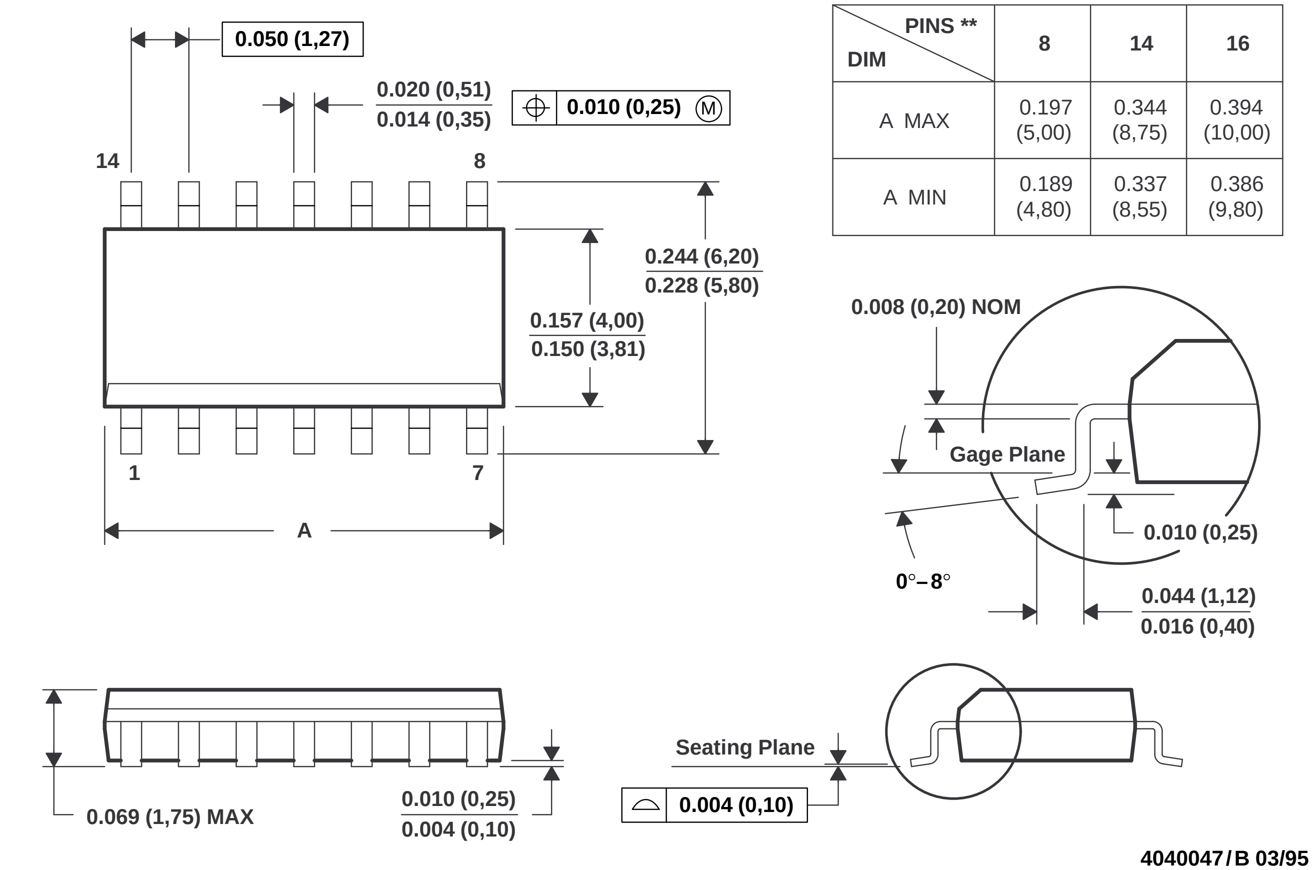
PSpice and *Parts* are trademarks of MicroSim Corporation.

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

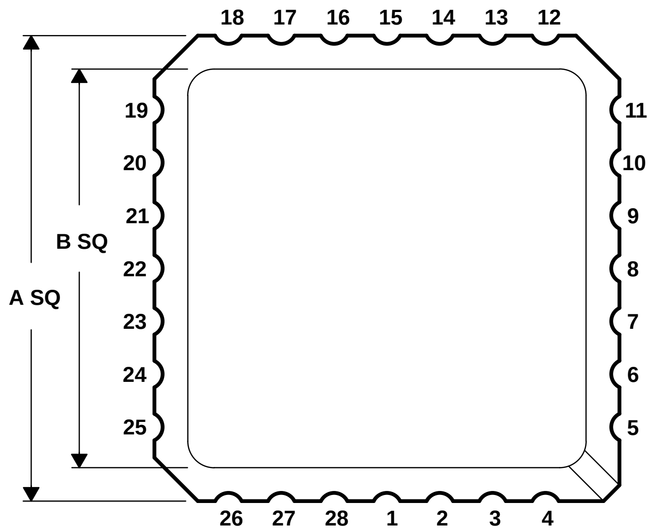


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

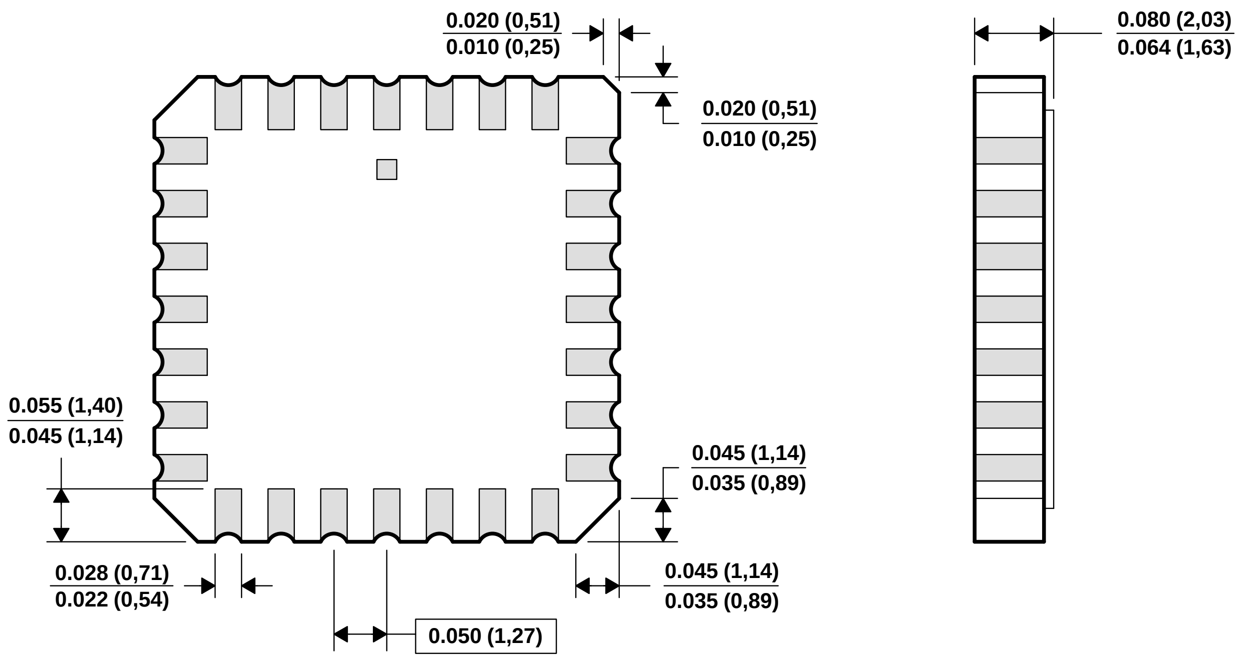
MECHANICAL INFORMATION

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



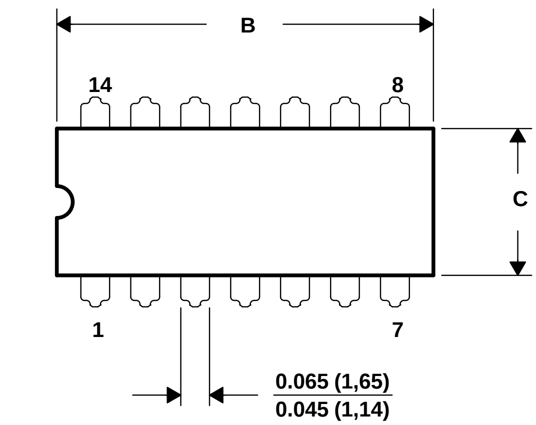
4040140 / C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

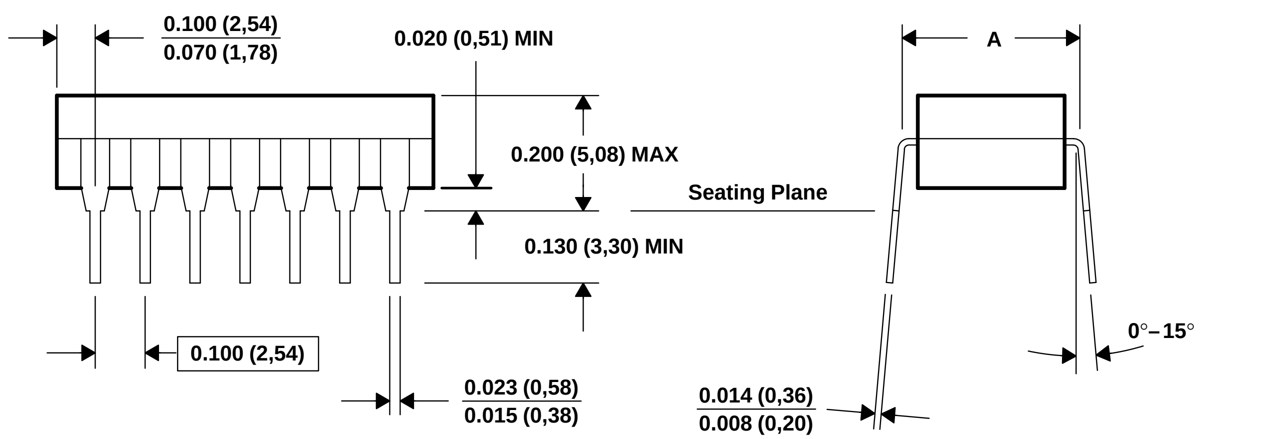
MECHANICAL INFORMATION

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	——	0.930 (23,62)	——
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	——



4040083/B 04/95

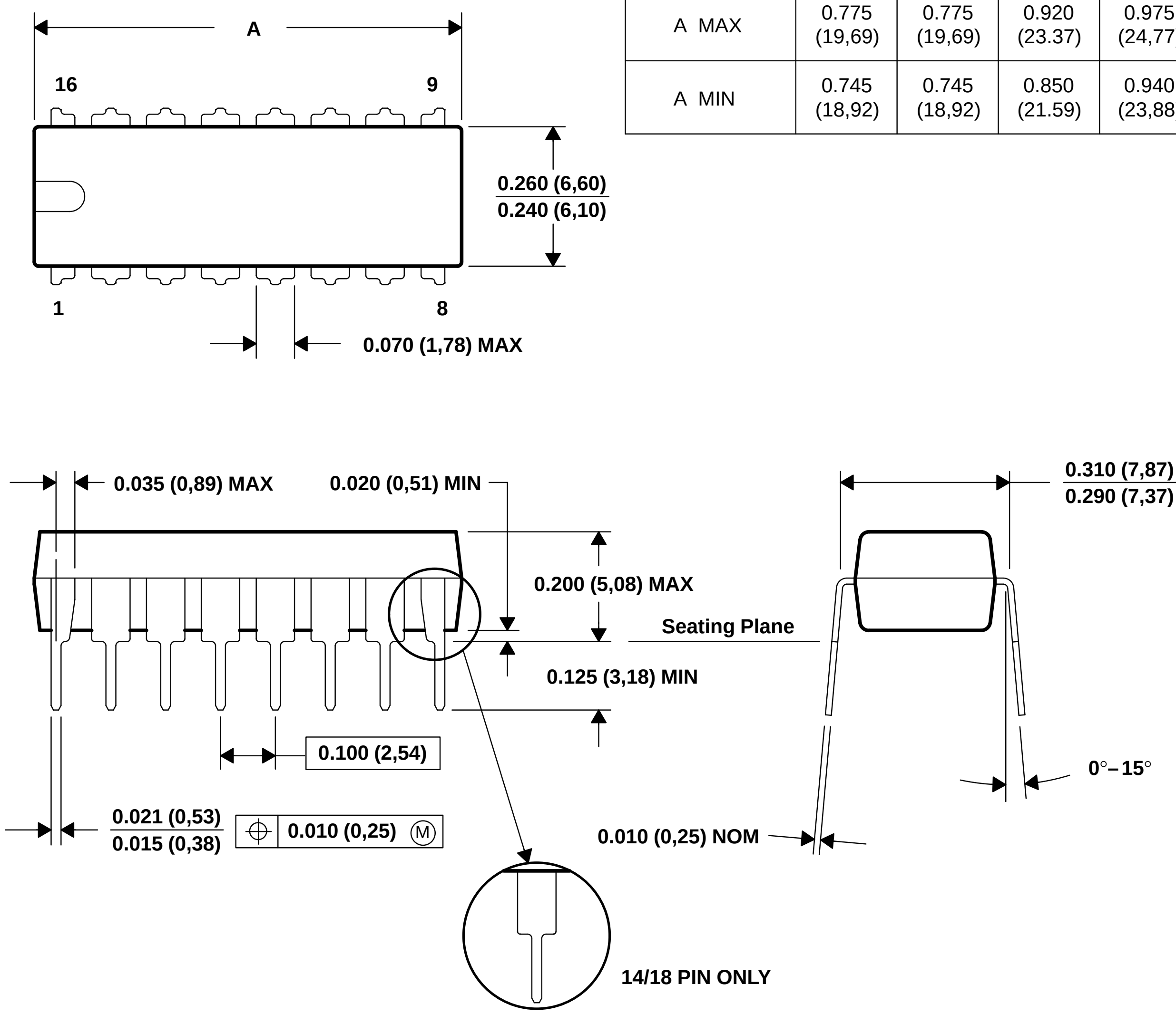
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

MECHANICAL INFORMATION

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

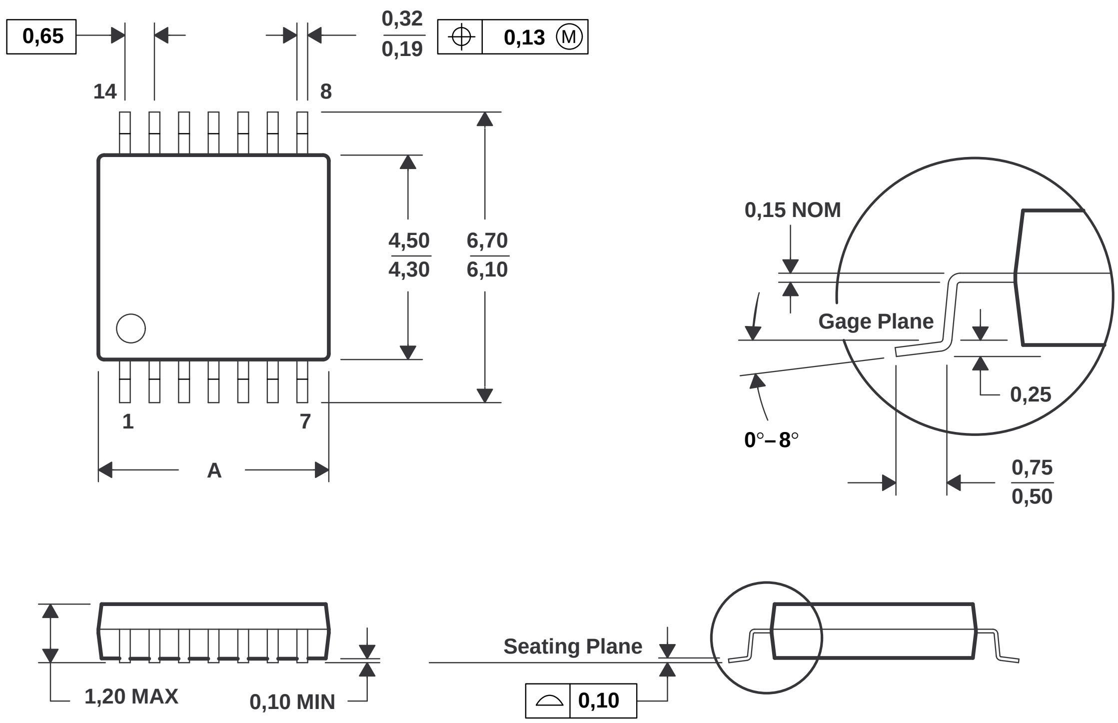


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



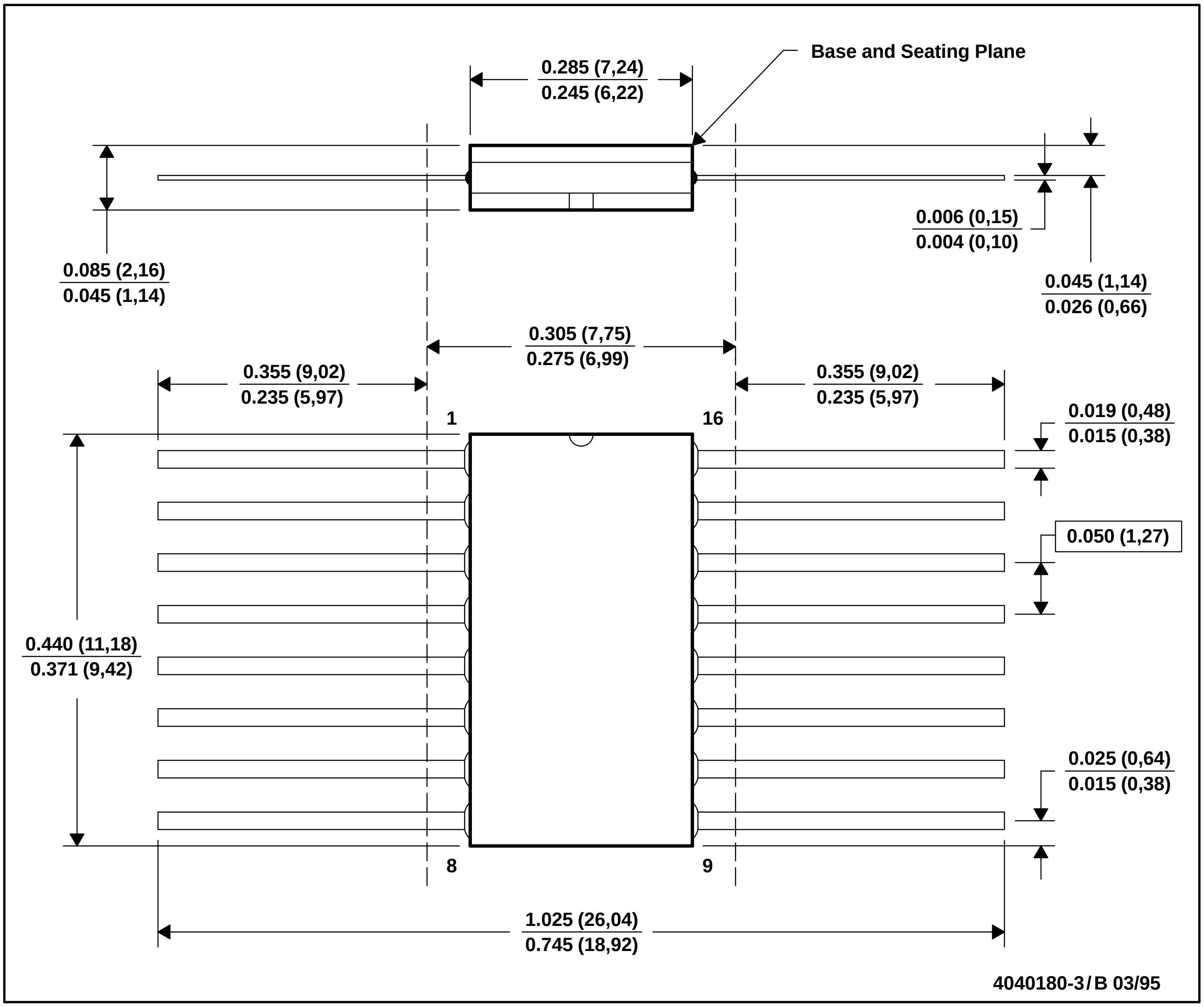
PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL INFORMATION

W (R-GDFP-F16) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC