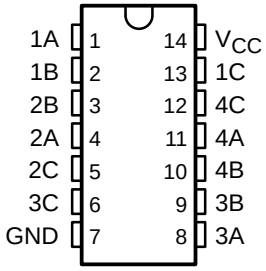
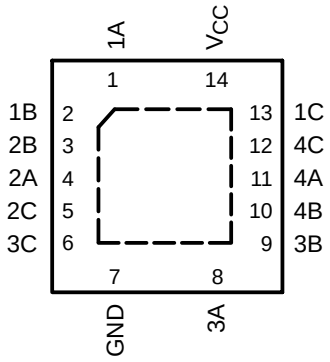
- **2-V to 5.5-V $V_{CC}$ Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**SN54LV4066A . . . J OR W PACKAGE**
**SN74LV4066A . . . D, DB, DGV, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN74LV4066A . . . RGY PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description/ordering information

This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V $V_{CC}$ operation.

These switches are designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

**ORDERING INFORMATION**

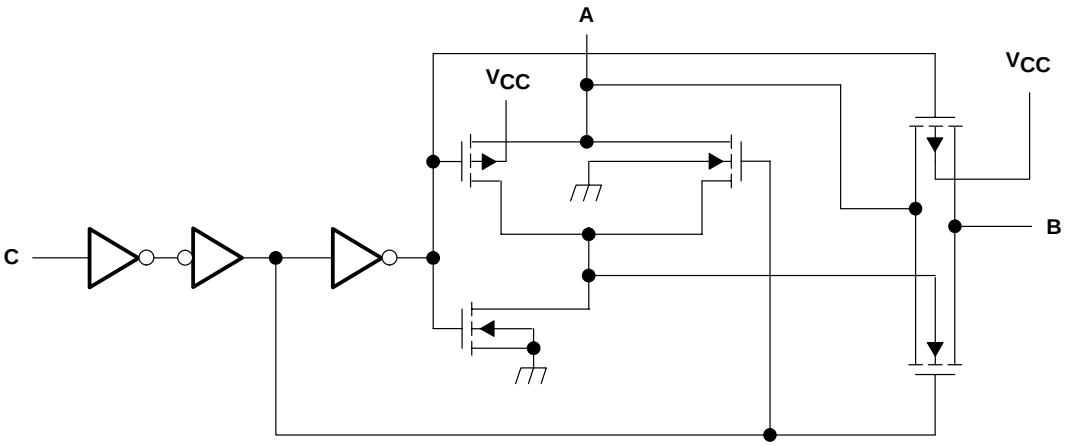
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Tube | SN74LV4066AN | SN74LV4066AN |
| | QFN – RGY | Tape and reel | SN74LV4066ARGYR | LW066A |
| | SOIC – D | Tube | SN74LV4066AD | LV4066A |
| | | Tape and reel | SN74LV4066ADR | |
| | SOP – NS | Tape and reel | SN74LV4066ANSR | 74LV4066A |
| | SSOP – DB | Tape and reel | SN74LV4066ADBR | LW066A |
| | TSSOP – PW | Tape and reel | SN74LV4066APWR | LW066A |
| | TVSOP – DGV | Tape and reel | SN74LV4066ADGVR | LW066A |
| –55°C to 125°C | CDIP – J | Tube | SNJ54LV4066AJ | SNJ54LV4066AJ |
| | CFP – W | Tube | SNJ54LV4066AW | SNJ54LV4066AW |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each switch)**

| INPUT CONTROL (C) | SWITCH |
|---|---|
| L | OFF |
| H | ON |

## logic diagram (positive logic)




One of Four Switches

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Switch I/O voltage range, $V_{IO}$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Control-input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
I/O diode current, $I_{IOK}$ ($V_{IO}$ < 0 or $V_{IO}$ > $V_{CC}$) . . . . . ±50 mA
On-state switch current, $I_T$ ($V_{IO}$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 86°C/W
(see Note 3): DB package . . . . . 96°C/W
(see Note 3): DGV package . . . . . 127°C/W
(see Note 3): N package . . . . . 80°C/W
(see Note 3): NS package . . . . . 76°C/W
(see Note 3): PW package . . . . . 113°C/W
(see Note 4): RGY package . . . . . 47°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 5)

| | | | SN54LV4066A | | SN74LV4066A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2† | 5.5 | 2† | 5.5 | V |
| $V_{IH}$ | High-level input voltage, control inputs | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC} \times 0.7$ | | $V_{CC} \times 0.7$ | | |
| $V_{IL}$ | Low-level input voltage, control inputs | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | |
| $V_I$ | Control input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_{IO}$ | Input/output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54LV4066A | | SN74LV4066A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $r_{on}$ | On-state switch resistance | $I_T$ = –1 mA, $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$ (see Figure 1) | 2.3 V | | 38 | 180 | | 225 | | 225 | Ω |
| | | | 3 V | | 29 | 150 | | 190 | | 190 | |
| | | | 4.5 V | | 21 | 75 | | 100 | | 100 | |
| $r_{on(p)}$ | Peak on-state resistance | $I_T$ = –1 mA, $V_I$ = $V_{CC}$ to GND, $V_C$ = $V_{IH}$ | 2.3 V | | 143 | 500 | | 600 | | 600 | Ω |
| | | | 3 V | | 57 | 180 | | 225 | | 225 | |
| | | | 4.5 V | | 31 | 100 | | 125 | | 125 | |
| $\Delta r_{on}$ | Difference in on-state resistance between switches | $I_T$ = –1 mA, $V_I$ = $V_{CC}$ to GND, $V_C$ = $V_{IH}$ | 2.3 V | | 6 | 30 | | 40 | | 40 | Ω |
| | | | 3 V | | 3 | 20 | | 30 | | 30 | |
| | | | 4.5 V | | 2 | 15 | | 20 | | 20 | |
| $I_I$ | Control input current | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{S(off)}$ | Off-state switch leakage current | $V_I$ = $V_{CC}$ and $V_O$ = GND, or $V_I$ = GND and $V_O$ = $V_{CC}$, $V_C$ = $V_{IL}$ (see Figure 2) | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{S(on)}$ | On-state switch leakage current | $V_I$ = $V_{CC}$ or GND, $V_C$ = $V_{IH}$ (see Figure 3) | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | | | 20 | | 20 | µA |
| $C_{ic}$ | Control input capacitance | | | | 1.5 | | | | | | pF |
| $C_{io}$ | Switch input/output capacitance | | | | 5.5 | | | | | | pF |
| $C_F$ | Feed-through capacitance | | | | 0.5 | | | | | | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN54LV4066A | | SN74LV4066A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | A or B | B or A | $C_L$ = 15 pF, (see Figure 4) | | 1.2 | 10 | | 16 | | 16 | ns |
| $t_{PZH}$ $t_{PZL}$ | Switch turn-on time | C | A or B | $C_L$ = 15 pF, $R_L$ = 1 kΩ (see Figure 5) | | 3.3 | 15 | | 20 | | 20 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Switch turn-off time | C | A or B | $C_L$ = 15 pF, $R_L$ = 1 kΩ (see Figure 5) | | 6 | 15 | | 23 | | 23 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | A or B | B or A | $C_L$ = 50 pF, (see Figure 4) | | 2.6 | 12 | | 18 | | 18 | ns |
| $t_{PZH}$ $t_{PZL}$ | Switch turn-on time | C | A or B | $C_L$ = 50 pF, $R_L$ = 1 kΩ (see Figure 5) | | 4.2 | 25 | | 32 | | 32 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Switch turn-off time | C | A or B | $C_L$ = 50 pF, $R_L$ = 1 kΩ (see Figure 5) | | 9.6 | 25 | | 32 | | 32 | ns |



### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN54LV4066A | | SN74LV4066A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | A or B | B or A | $C_L$ = 15 pF, (see Figure 4) | | 0.8 | 6 | | 10 | | 10 | ns |
| $t_{PZH}$ $t_{PZL}$ | Switch turn-on time | C | A or B | $C_L$ = 15 pF, $R_L$ = 1 kΩ (see Figure 5) | | 2.3 | 11 | | 15 | | 15 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Switch turn-off time | C | A or B | $C_L$ = 15 pF, $R_L$ = 1 kΩ (see Figure 5) | | 4.5 | 11 | | 15 | | 15 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | A or B | B or A | $C_L$ = 50 pF, (see Figure 4) | | 1.5 | 9 | | 12 | | 12 | ns |
| $t_{PZH}$ $t_{PZL}$ | Switch turn-on time | C | A or B | $C_L$ = 50 pF, $R_L$ = 1 kΩ (see Figure 5) | | 3 | 18 | | 22 | | 22 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Switch turn-off time | C | A or B | $C_L$ = 50 pF, $R_L$ = 1 kΩ (see Figure 5) | | 7.2 | 18 | | 22 | | 22 | ns |

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN54LV4066A | | SN74LV4066A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | A or B | B or A | $C_L$ = 15 pF, (see Figure 4) | | 0.3 | 4 | | 7 | | 7 | ns |
| $t_{PZH}$ $t_{PZL}$ | Switch turn-on time | C | A or B | $C_L$ = 15 pF, $R_L$ = 1 kΩ (see Figure 5) | | 1.6 | 7 | | 10 | | 10 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Switch turn-off time | C | A or B | $C_L$ = 15 pF, $R_L$ = 1 kΩ (see Figure 5) | | 3.2 | 7 | | 10 | | 10 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | A or B | B or A | $C_L$ = 50 pF, (see Figure 4) | | 0.6 | 6 | | 8 | | 8 | ns |
| $t_{PZH}$ $t_{PZL}$ | Switch turn-on time | C | A or B | $C_L$ = 50 pF, $R_L$ = 1 kΩ (see Figure 5) | | 2.1 | 12 | | 16 | | 16 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Switch turn-off time | C | A or B | $C_L$ = 50 pF, $R_L$ = 1 kΩ (see Figure 5) | | 5.1 | 12 | | 16 | | 16 | ns |



## analog switch characteristics over operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| Frequency response (switch on) | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (sine wave) $20\log_{10}(V_O/V_I)$ = –3 dB (see Figure 6) | | 2.3 V | | 30 | | MHz |
| | | | | | 3 V | | 35 | | |
| | | | | | 4.5 V | | 50 | | |
| Crosstalk (between any switches) | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (sine wave) (see Figure 7) | | 2.3 V | | –45 | | dB |
| | | | | | 3 V | | –45 | | |
| | | | | | 4.5 V | | –45 | | |
| Crosstalk (control input to signal output) | C | A or B | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (square wave) (see Figure 8) | | 2.3 V | | 15 | | mV |
| | | | | | 3 V | | 20 | | |
| | | | | | 4.5 V | | 50 | | |
| Feed-through attenuation (switch off) | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (see Figure 9) | | 2.3 V | | –40 | | dB |
| | | | | | 3 V | | –40 | | |
| | | | | | 4.5 V | | –40 | | |
| Sine-wave distortion | A or B | B or A | $C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 1 kHz (sine wave) (see Figure 10) | $V_I$ = 2 $V_{p-p}$ | 2.3 V | | 0.1 | | % |
| | | | | $V_I$ = 2.5 $V_{p-p}$ | 3 V | | 0.1 | | |
| | | | | $V_I$ = 4 $V_{p-p}$ | 4.5 V | | 0.1 | | |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 10 MHz | 4.5 | pF |

## PARAMETER MEASUREMENT INFORMATION

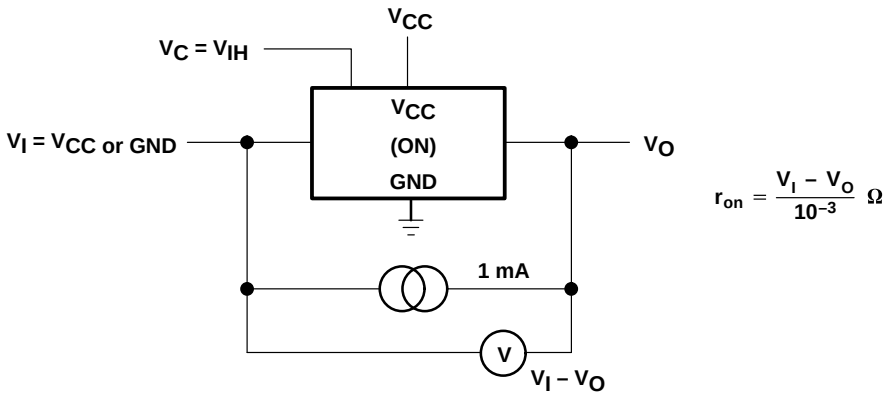
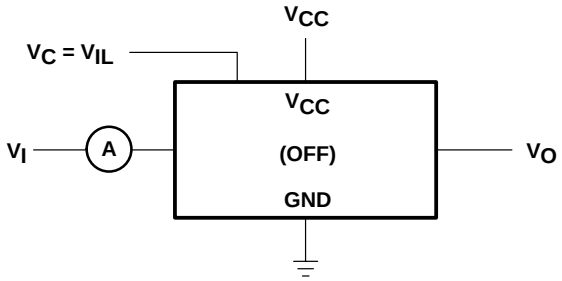



**Figure 1. On-State Resistance Test Circuit**




**Condition 1: $V_I$ = 0, $V_O$ = $V_{CC}$**
**Condition 2: $V_I$ = $V_{CC}$, $V_O$ = 0**

**Figure 2. Off-State Switch Leakage-Current Test Circuit**

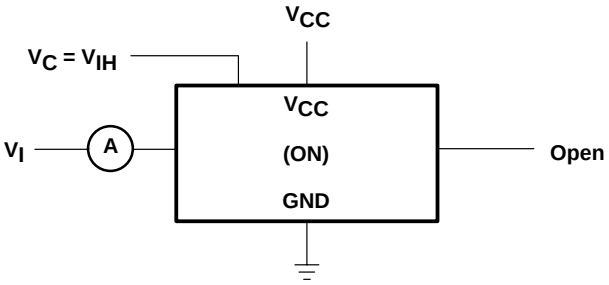



**Figure 3. On-State Leakage-Current Test Circuit**

## PARAMETER MEASUREMENT INFORMATION

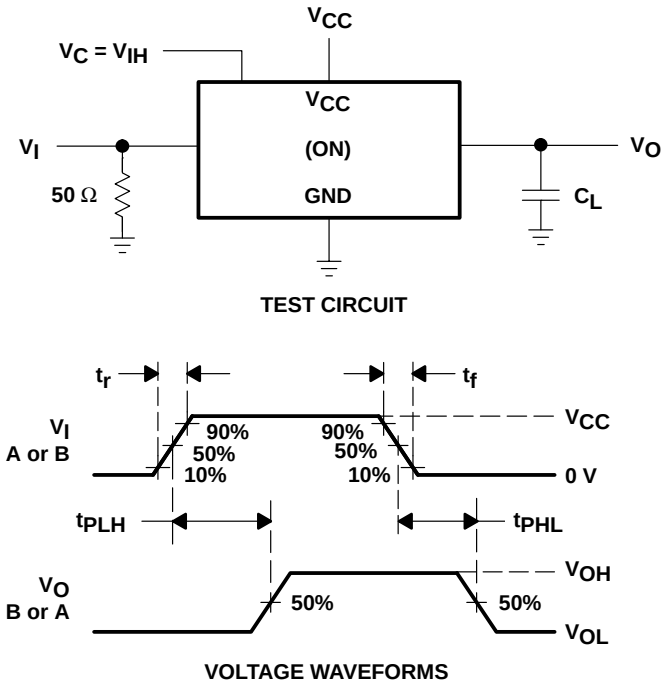
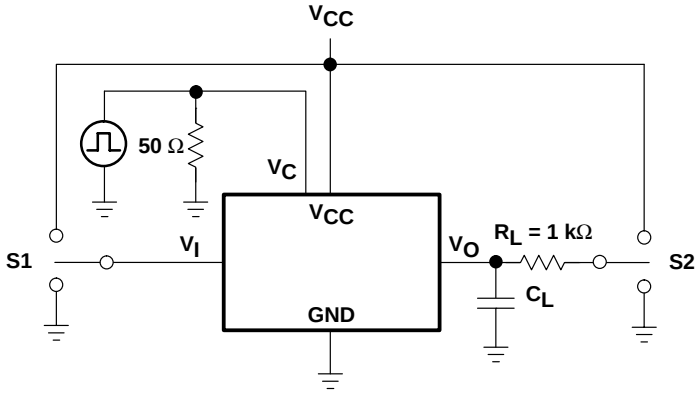


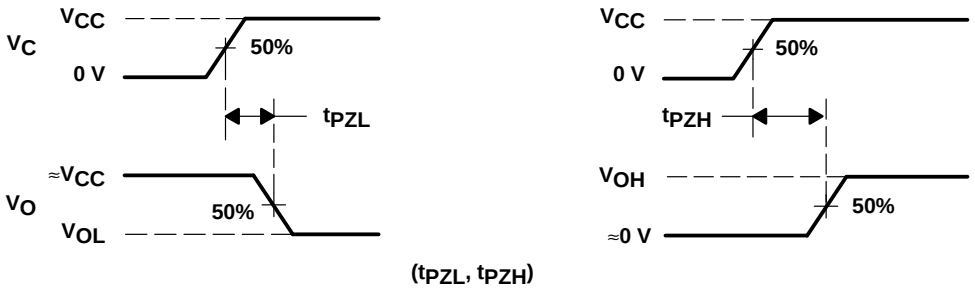

**Figure 4. Propagation Delay Time, Signal Input to Signal Output**

## PARAMETER MEASUREMENT INFORMATION

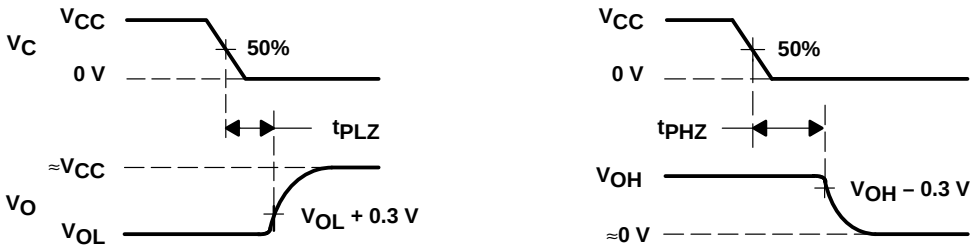



| TEST | S1 | S2 |
|---|---|---|
| $t_{PZL}$ | GND | $V_{CC}$ |
| $t_{PZH}$ | $V_{CC}$ | GND |
| $t_{PLZ}$ | GND | $V_{CC}$ |
| $t_{PHZ}$ | $V_{CC}$ | GND |

TEST CIRCUIT




($t_{PZL}$, $t_{PZH}$)




($t_{PLZ}$, $t_{PHZ}$)

VOLTAGE WAVEFORMS

**Figure 5. Switching Time ($t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$), Control to Signal Output**

## PARAMETER MEASUREMENT INFORMATION

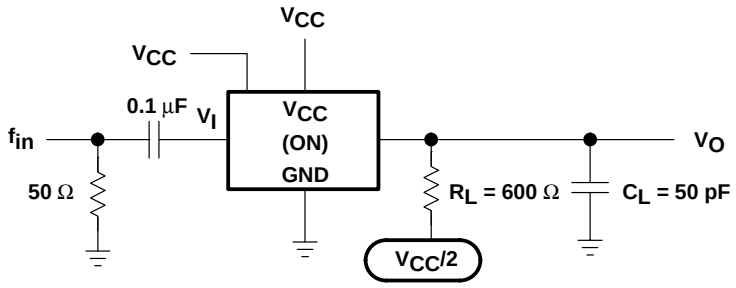



**Figure 6. Frequency Response (Switch On)**

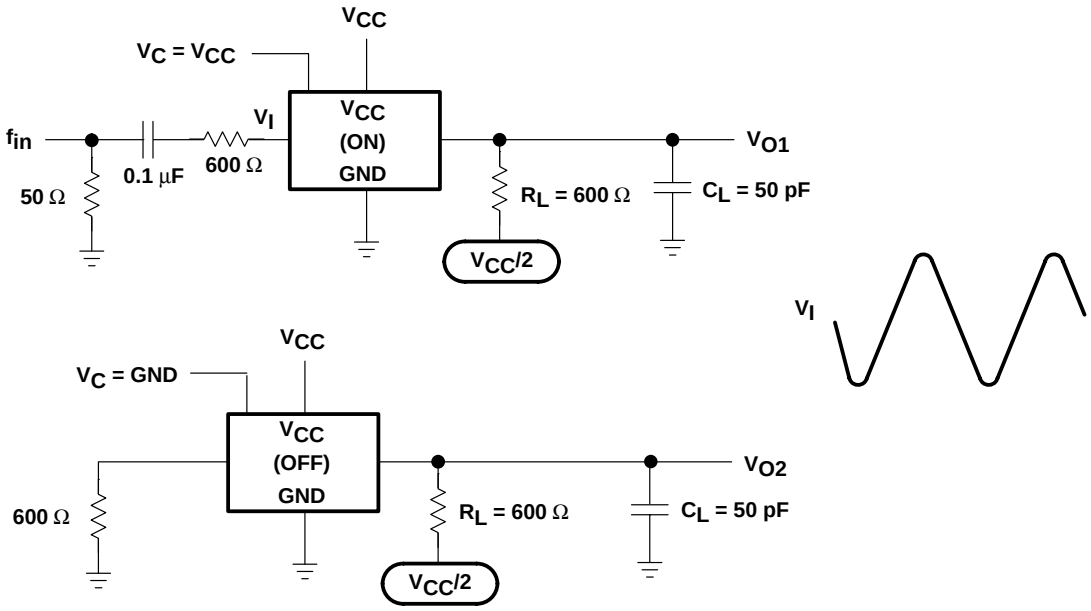



**Figure 7. Crosstalk Between Any Two Switches**

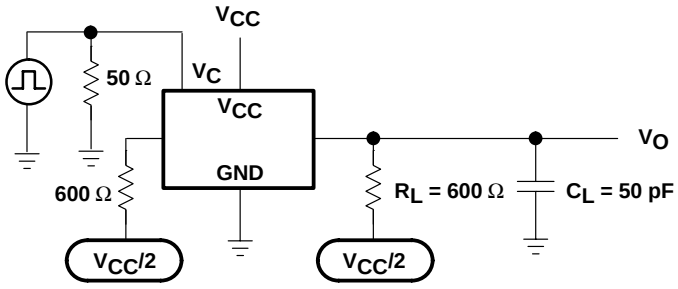



**Figure 8. Crosstalk (Control Input – Switch Output)**

## PARAMETER MEASUREMENT INFORMATION

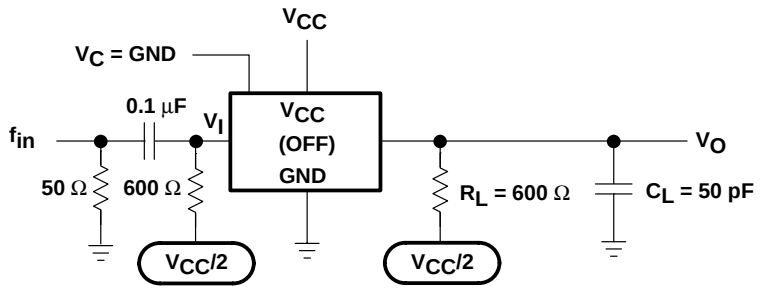



**Figure 9. Feed-Through Attenuation (Switch Off)**

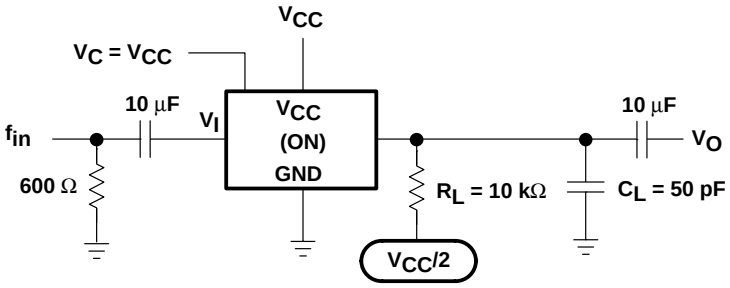
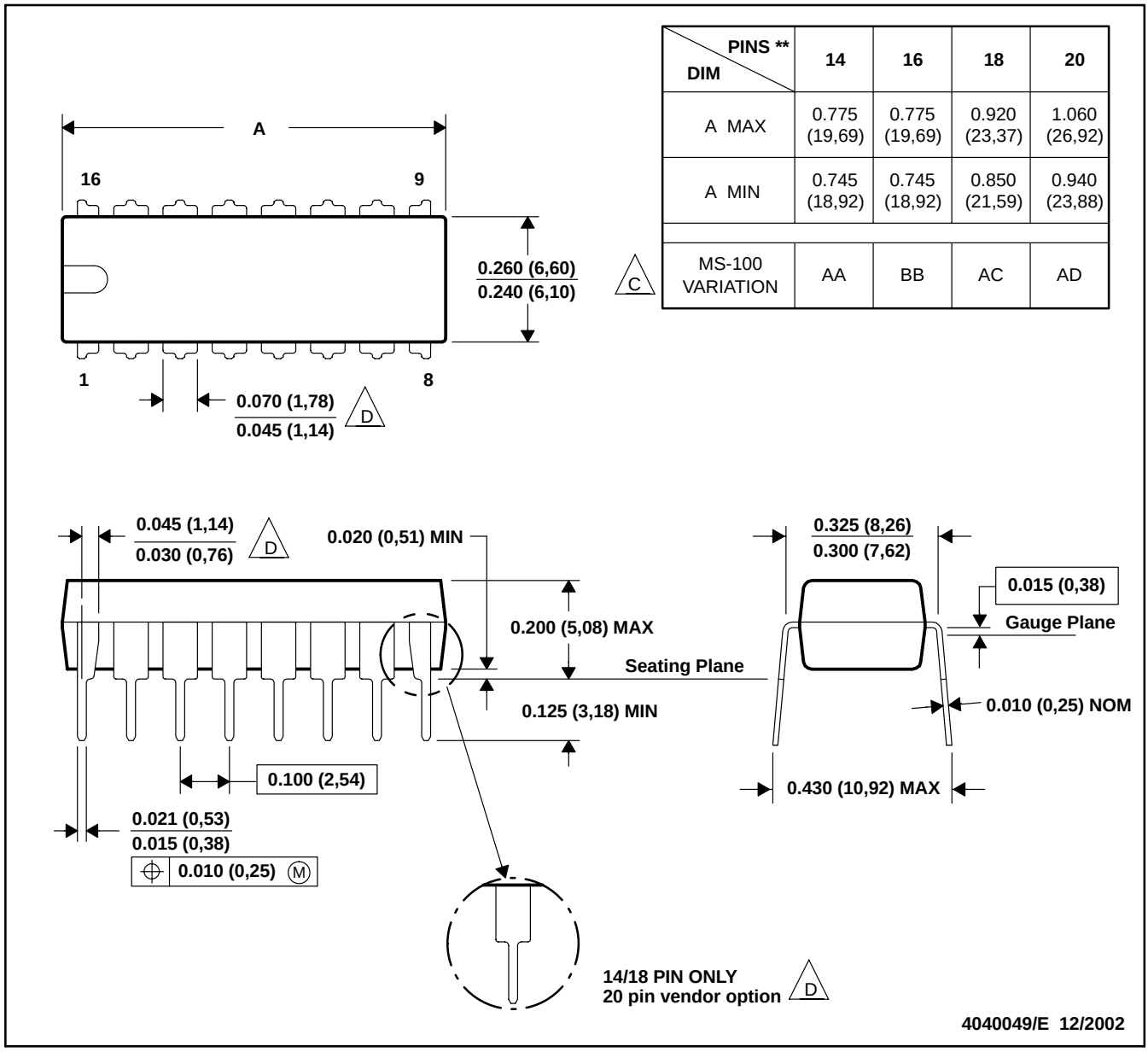



**Figure 10. Sine-Wave Distortion**

## N (R-PDIP-T**)

## PLASTIC DUAL-IN-LINE PACKAGE

**16 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-100 VARIATION | AA | BB | AC | AD |

NOTES: A. All linear dimensions are in inches (millimeters).

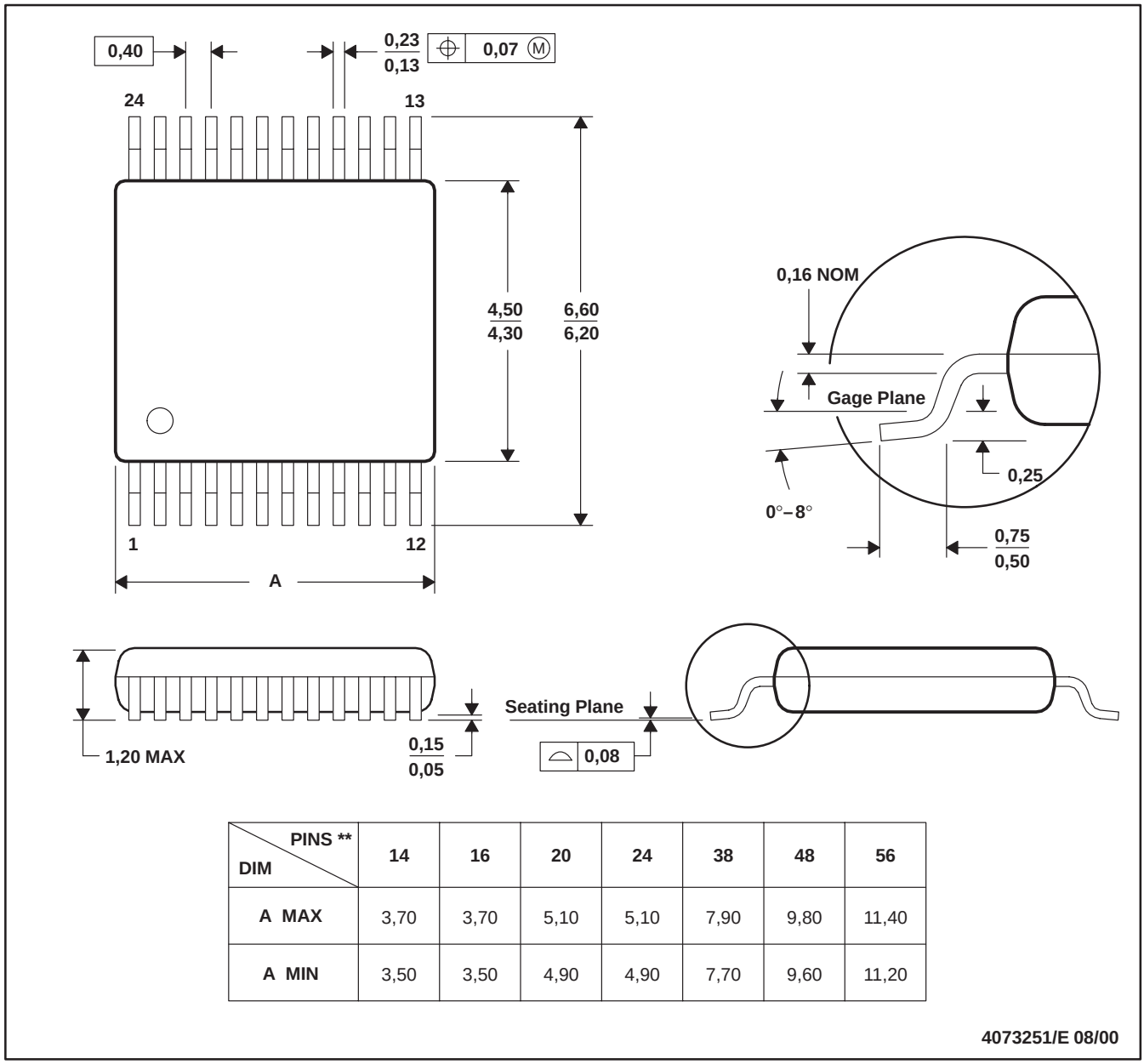
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

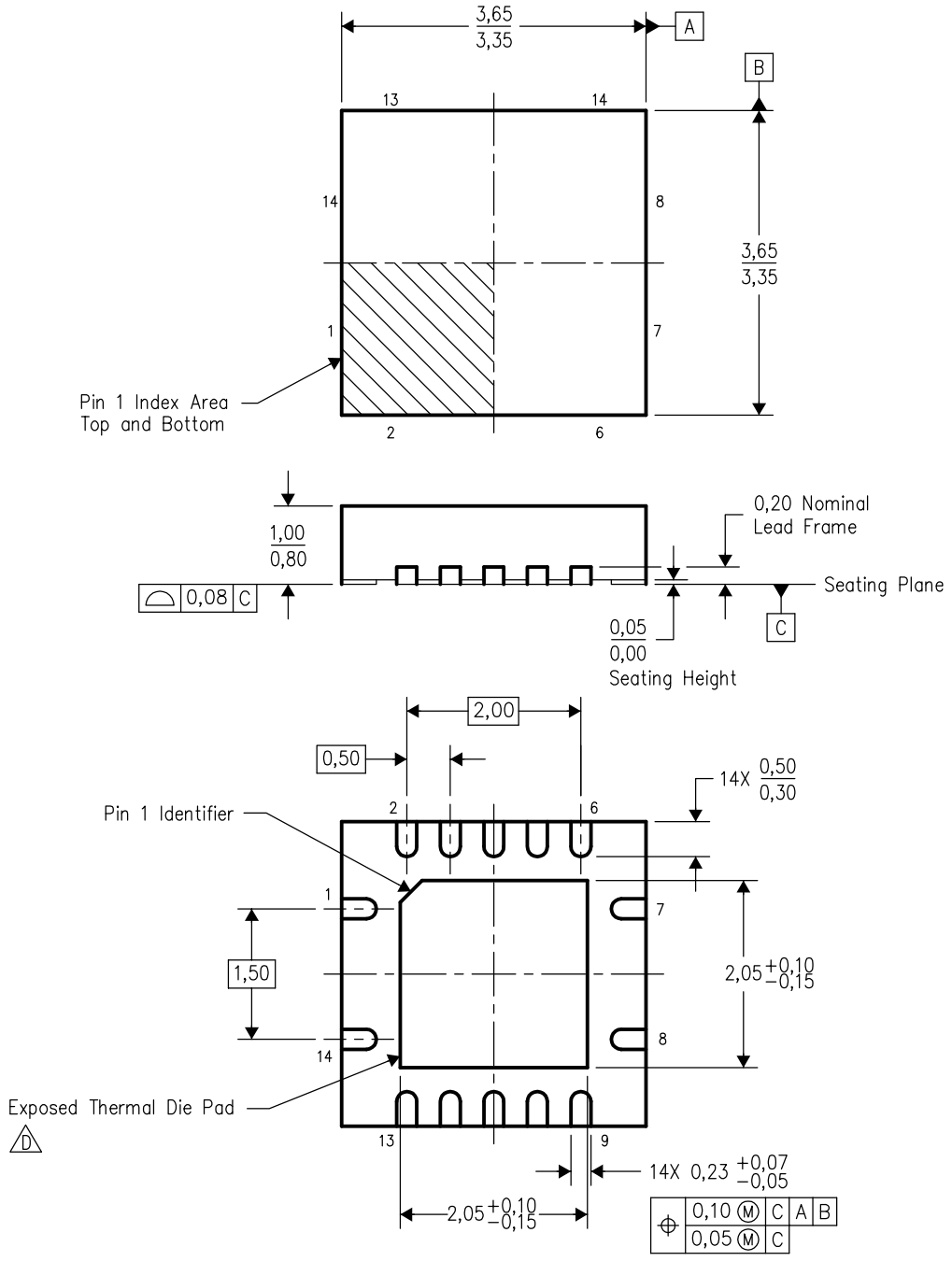



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RGY (S–PQFP–N14) PLASTIC QUAD FLATPACK



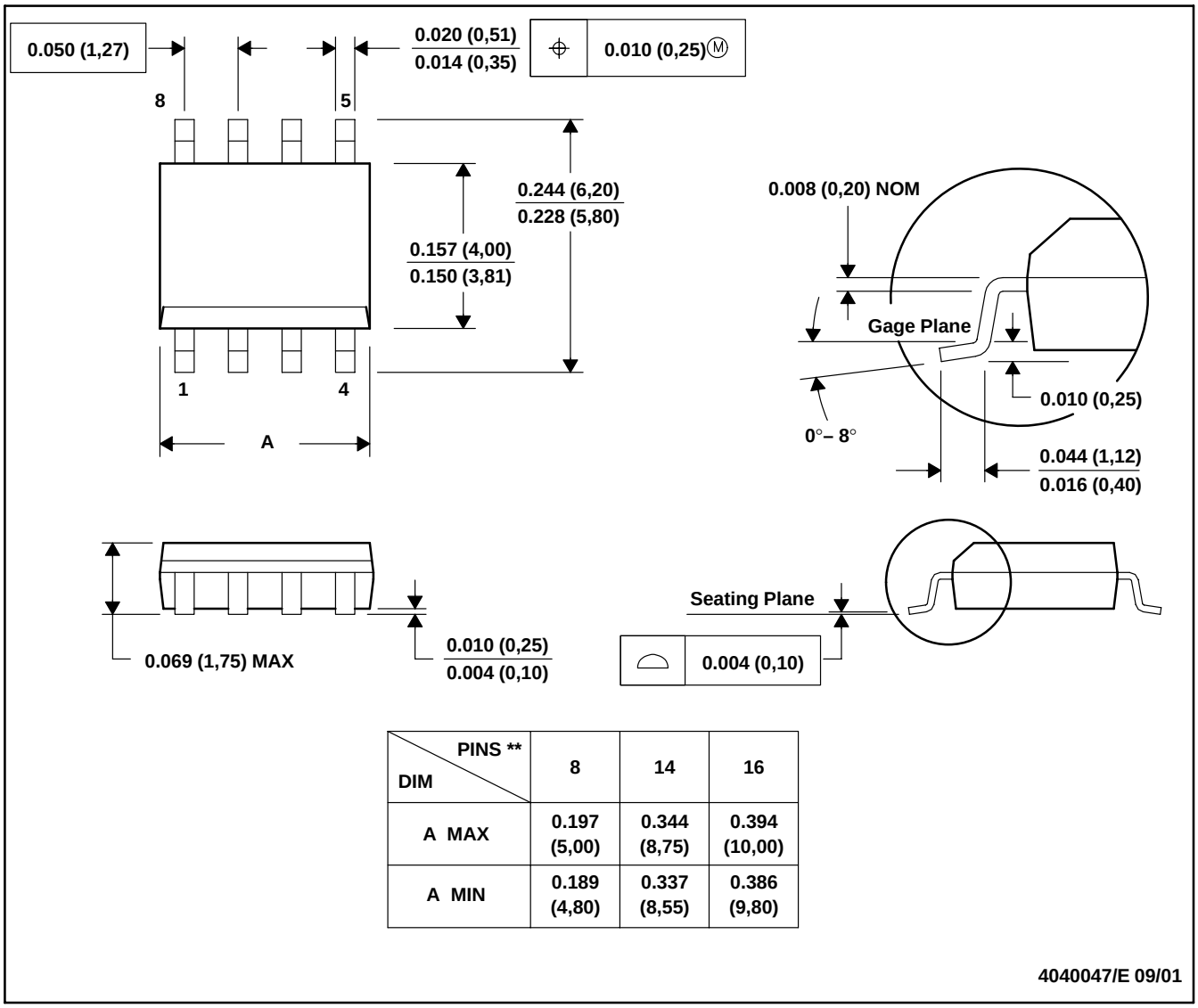

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
E. Package complies to JEDEC MO–241 variation BA.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

## D (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE PACKAGE

**8 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

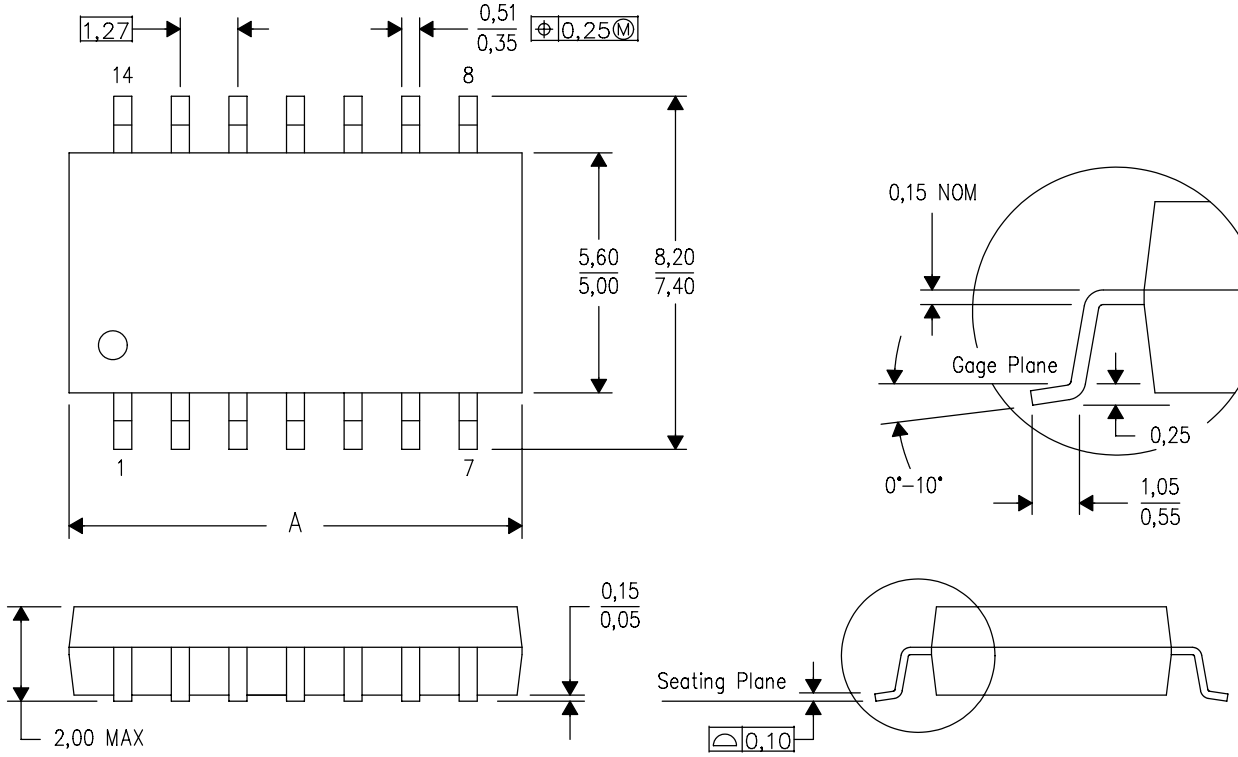
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

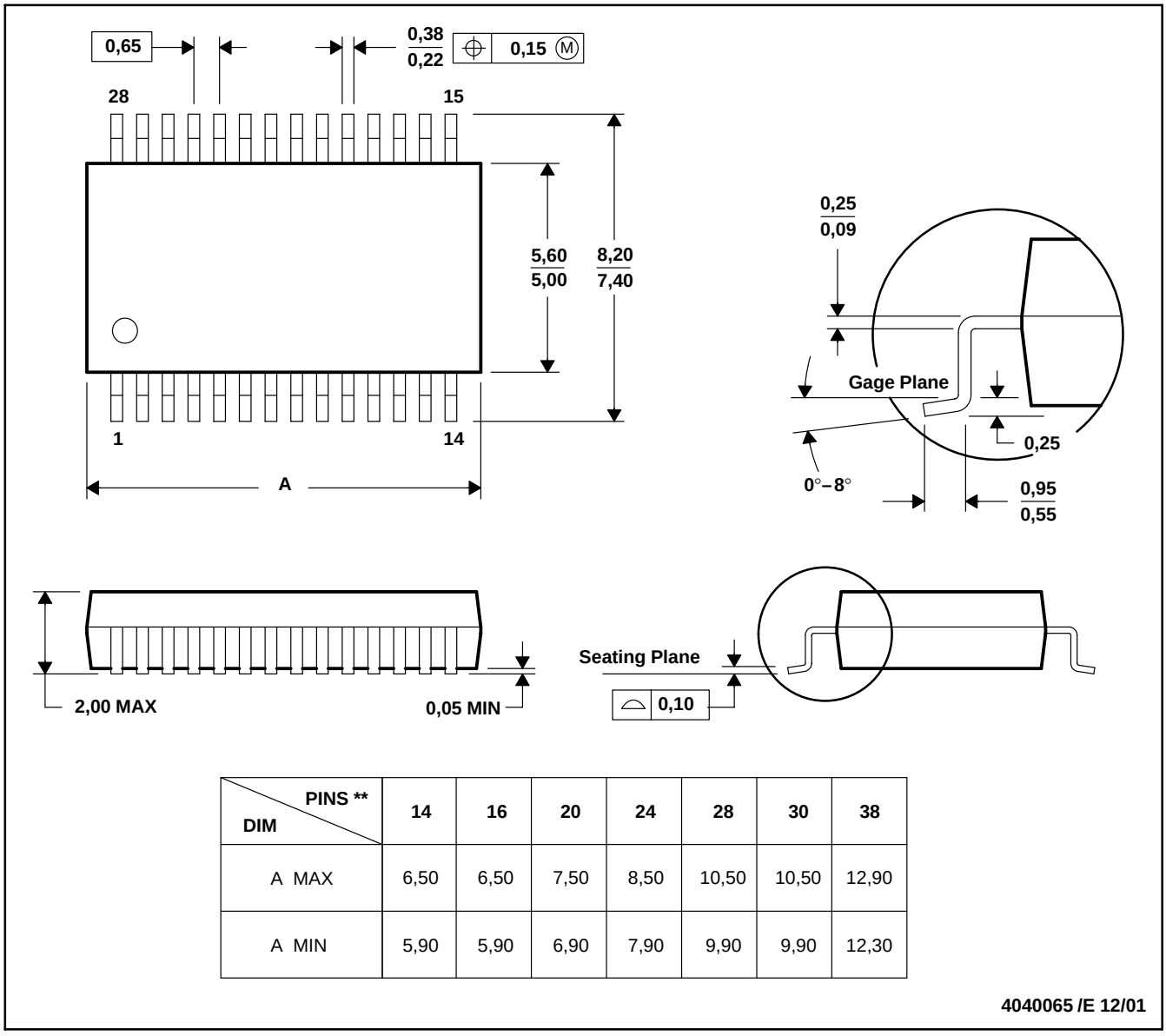
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



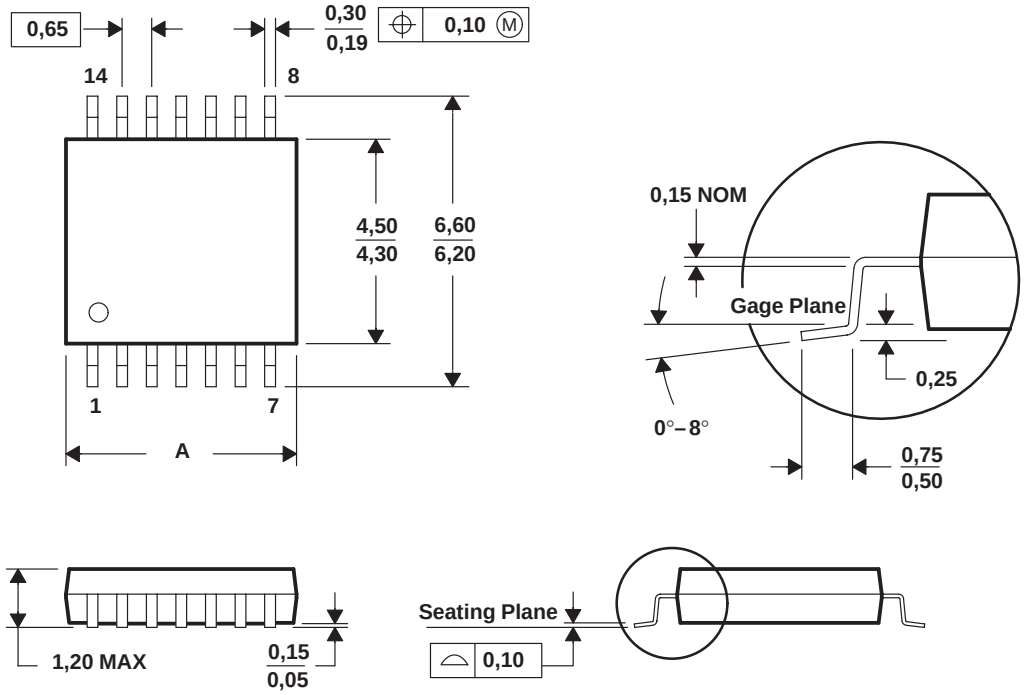

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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