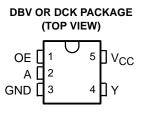
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- Operating Range of 2 V to 5.5 V
- Max t_{pd} of 6 ns at 5 V
- Low Power Consumption, 10-μA Max I_{CC}
- ◆ ±8-mA Output Drive at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17



description/ordering information

The SN74AHC1G126 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION

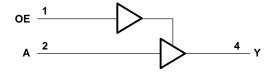
TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
	SOT (SOT-23) – DBV Reel of 3000 SN74AHC1G126DBVR		A26	
4000 1- 0500	301 (301-23) - DBV	Reel of 250	SN74AHC1G126DBVT	A26_
-40°C to 85°C	SOT (SC-70) – DCK		SN74AHC1G126DCKR	AN
	301 (30-70) - DCK	Reel of 250	SN74AHC1G126DCKT	AIN_

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPU	JTS	OUTPUT
OE	Α	Υ
Н	Н	Н
Н	L	L
L	Χ	Z

logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[‡]The actual top-side marking has one additional character that designates the assembly/test site.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 5.5 V	3.85		
	$ V_{CC} = 2 \text{ V} $ Low-level input voltage $ V_{CC} = 3 \text{ V} $			0.5	
V_{IL}				0.9	V
		V _{CC} = 5.5 V		1.65	
VI	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 2 V		-50	μΑ
IOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	IIIA
		V _{CC} = 2 V		50	μΑ
IOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	A
		$V_{CC} = 5 V \pm 0.5 V$		8	mA
A+/A>-	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	
Δt/Δv	Input transition rise or fall rate $V_{CC} = 5 \text{ V} \pm 0.8$			20	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	METER TEST CONDITIONS VCC	Voc	T _A = 25°C		;	MIN MAX	UNIT	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	WAX	UNIT
		2 V	1.9	2		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		
Voн		4.5 V	4.4	4.5		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48	2.48	
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
	I _{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
V _{OL}		4.5 V			0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44	
lį	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ
loz	$V_I = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Ci	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
Co	$V_O = V_{CC}$ or GND	5 V		10				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T _A = 25°	С	MINI	MIN MAX		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN TYP	MAX	IVIIIN	IVIAA	UNIT	
^t PLH	А	Y	C _L = 15 pF	5.6	8	1	9.5	ns	
^t PHL	A	ī	CL = 15 pr	5.6	8	1	9.5	115	
^t PZH	OF.	Y	C: - 15 pF	5.4	8	1	9.5	ns	
t _{PZL}	OE_	ī	C _L = 15 pF	5.4	8	1	9.5	115	
^t PHZ	OE	Y	0: 45 = 5	7	9.7	1	11.5	20	
^t PLZ	OL	ī	C _L = 15 pF	7	9.7	1	11.5	ns	
^t PLH	А	Y	C 50 pF	8.1	11.5	1	13	ns	
^t PHL	A	A Y $C_L = 50 \text{ pF}$	8.1	11.5	1	13	115		
^t PZH	OF.	Y	C _L = 50 pF	7.9	11.5	1	13	20	
t _{PZL}	OE	1	OL = 50 PF	7.9	11.5	1	13	ns	
^t PHZ	OE	V	C: - 50 pE	9.5	13.2	1	15	20	
^t PLZ		Y	Y	C _L = 50 pF	9.5	13.2	1	15	ns

SN74AHC1G126 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

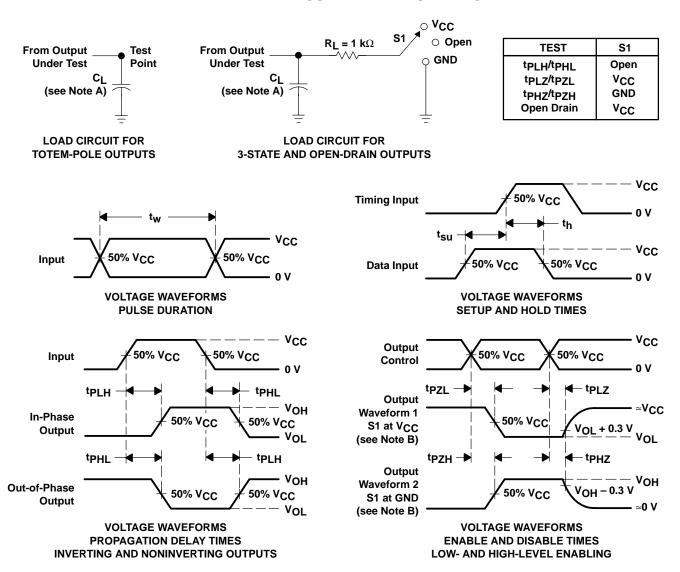
PARAMETER	FROM	TO LO	LOAD	T,	Վ = 25°C	;	MIN MAX	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	CAPACITANCE MIN TYP		MAX	IVIIIV	IVIAA	UNII	
^t PLH	А	Y	C _I = 15 pF		3.8	5.5	1	6.5	ns	
t _{PHL}	A	ı	OL = 13 pr		3.8	5.5	1	6.5	115	
^t PZH	OE	Y	C _L = 15 pF		3.6	5.1	1	6	ns	
^t PZL	OE	OE CL = 15 pr	τ		3.6	5.1	1	6	115	
^t PHZ	OE	Y	C _L = 15 pF		4.6	6.8	1	8	ns	
^t PLZ		ī	OL = 15 pr		4.6	6.8	1	8	115	
^t PLH	А	Y	C: - 50 pF		5.3	7.5	1	8.5	ns	
^t PHL	A		σ_ = σο βι	T CL = 50 pr	5.3	7.5	1	8.5	115	
^t PZH	OF.	Y	C: - 50 pF		5.1	7.1	1	8	20	
^t PZL	OE	Ť		C _L = 50 pF		5.1	7.1	1	8	ns
^t PHZ	OE	Y	C. 50 pF		6.1	8.8	1	10	ns	
t _{PLZ}	OE .	r	C _L = 50 pF		6.1	8.8	1	10	115	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

ĺ		PARAMETER	TEST C	ONDITIONS	TYP	UNIT
Ī	C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF



PARAMETER MEASUREMENT INFORMATION



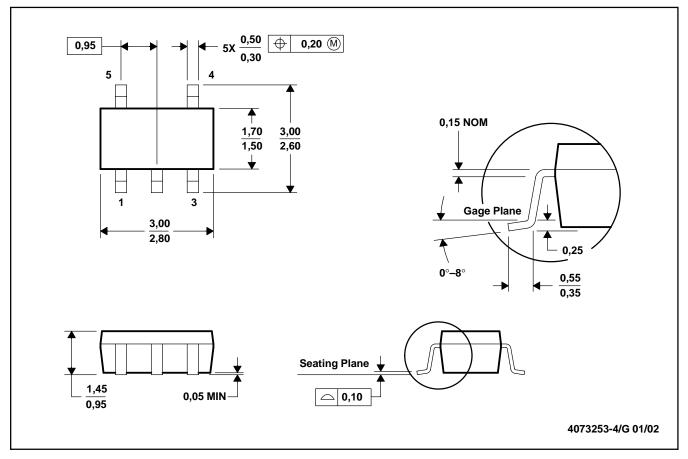
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE

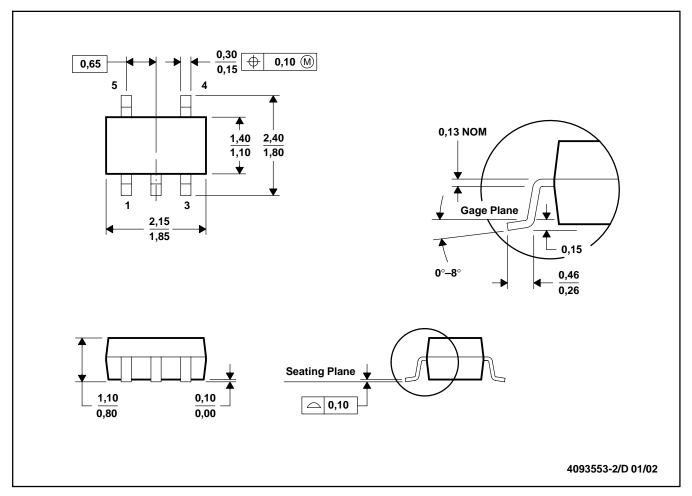


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-178

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

D. Falls within JEDEC MO-203

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