

TL081, TL081A, TL081B, TL082, TL082A, TL082B TL084, TL084A, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- High Input Impedance . . . JFET-Input Stage
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ μ s Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description/ordering information

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION

T_J	V_{IOmax} AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	15 mV	PDIP (P)	Tube of 50	TL081CP	TL081CP
			Tube of 50	TL082CP	TL082CP
		PDIP (N)	Tube of 25	TL084CN	TL084CN
		SOIC (D)	Tube of 75	TL081CD	TL081C
			Reel of 2500	TL081CDR	
			Tube of 75	TL082CD	TL082C
			Reel of 2500	TL082CDR	
			Tube of 50	TL084CD	TL084C
			Reel of 2500	TL084CDR	
		SOP (PS)	Reel of 2000	TL081CPSR	T081
			Reel of 2000	TL082CPSR	T082
		SOP (NS)	Reel of 2000	TL084CNSR	TL084
		TSSOP (PW)	Tube of 150	TL082CPW	T082
			Reel of 2000	TL082CPWR	
			Tube of 90	TL084CPW	T084
			Reel of 2000	TL084CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

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description/ordering information (continued)

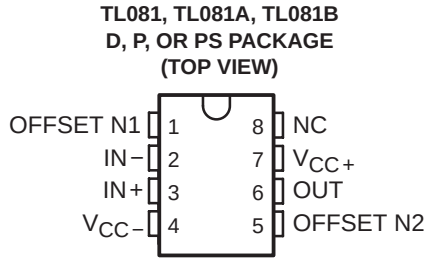
ORDERING INFORMATION

T_J	V_{IOmax} AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (P)	Tube of 50	TL081ACP	TL081ACP
			Tube of 50	TL082ACP	TL082ACP
		PDIP (N)	Tube of 25	TL084ACN	TL084ACN
		SOIC (D)	Tube of 75	TL081ACD	081AC
			Reel of 2500	TL081ACDR	
			Tube of 75	TL082ACD	082AC
			Reel of 2500	TL082ACDR	
			Tube of 50	TL084ACD	TL084AC
			Reel of 2500	TL084ACDR	
		SOP (PS)	Reel of 2000	TL082ACPSR	T082A
		SOP (NS)	Reel of 2000	TL084ACNSR	TL084A
	3 mV	PDIP (P)	Tube of 50	TL081BCP	TL081BCP
			Tube of 50	TL082BCP	TL082BCP
		PDIP (N)	Tube of 25	TL084BCN	TL084BCN
		SOIC (D)	Tube of 75	TL081BCD	081BC
			Reel of 2500	TL081BCDR	
			Tube of 75	TL082BCD	082BC
			Reel of 2500	TL082BCDR	
			Tube of 50	TL084BCD	TL084BC
			Reel of 2500	TL084BCDR	
–40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL081IP	TL081IP
			Tube of 50	TL082IP	TL082IP
		PDIP (N)	Tube of 25	TL084IN	TL081IN
		SOIC (D)	Tube of 75	TL081ID	TL081I
			Reel of 2500	TL081IDR	
			Tube of 75	TL082ID	TL082I
			Reel of 2500	TL082IDR	
			Tube of 50	TL084ID	TL084I
			Reel of 2500	TL084IDR	
		TSSOP (PW)	Reel of 2000	TL082IPWR	Z082
–40°C to 125°C	9 mV	SOIC (D)	Tube of 50	TL084QD	TL084QD
			Reel of 2500	TL084QDR	
–55°C to 125°C	9 mV	CDIP (J)	Tube of 25	TL084MJ	TL084MJ
		LCCC (FK)	Reel of 55	TL084FK	TL084FK
	6 mV	CDIP (JG)	Tube of 50	TL082MJG	TL082MJG
		LCCC (FK)	Tube of 55	TL082MFK	TL082MFK

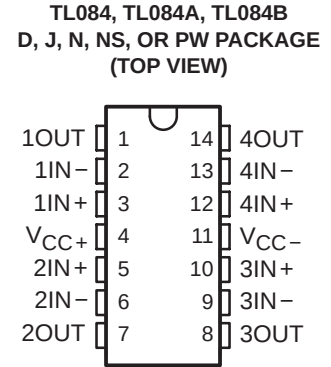
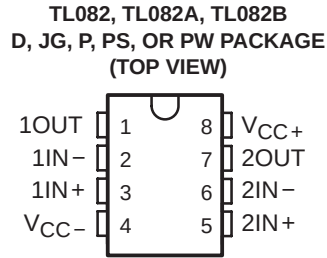
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TL081, TL081A, TL081B, TL082, TL082A, TL082B TL084, TL084A, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

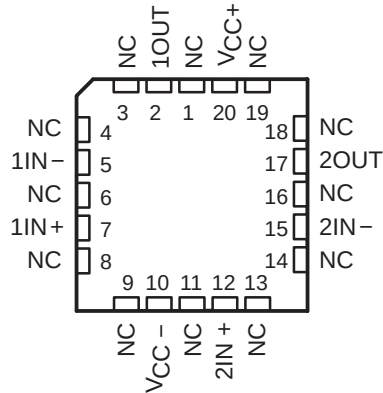
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NC – No internal connection

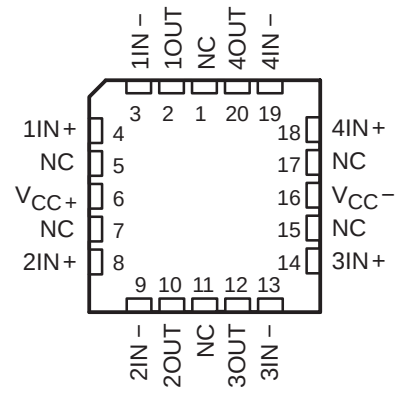


**TL082M . . . FK PACKAGE
(TOP VIEW)**



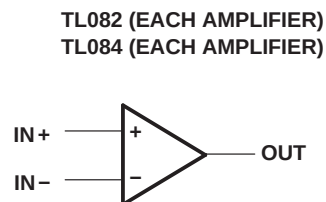
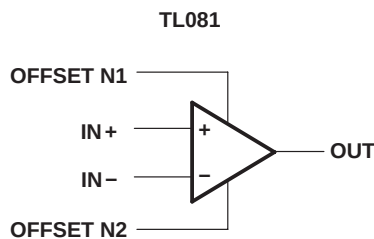
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**TL084M . . . FK PACKAGE
(TOP VIEW)**



NC – No internal connection

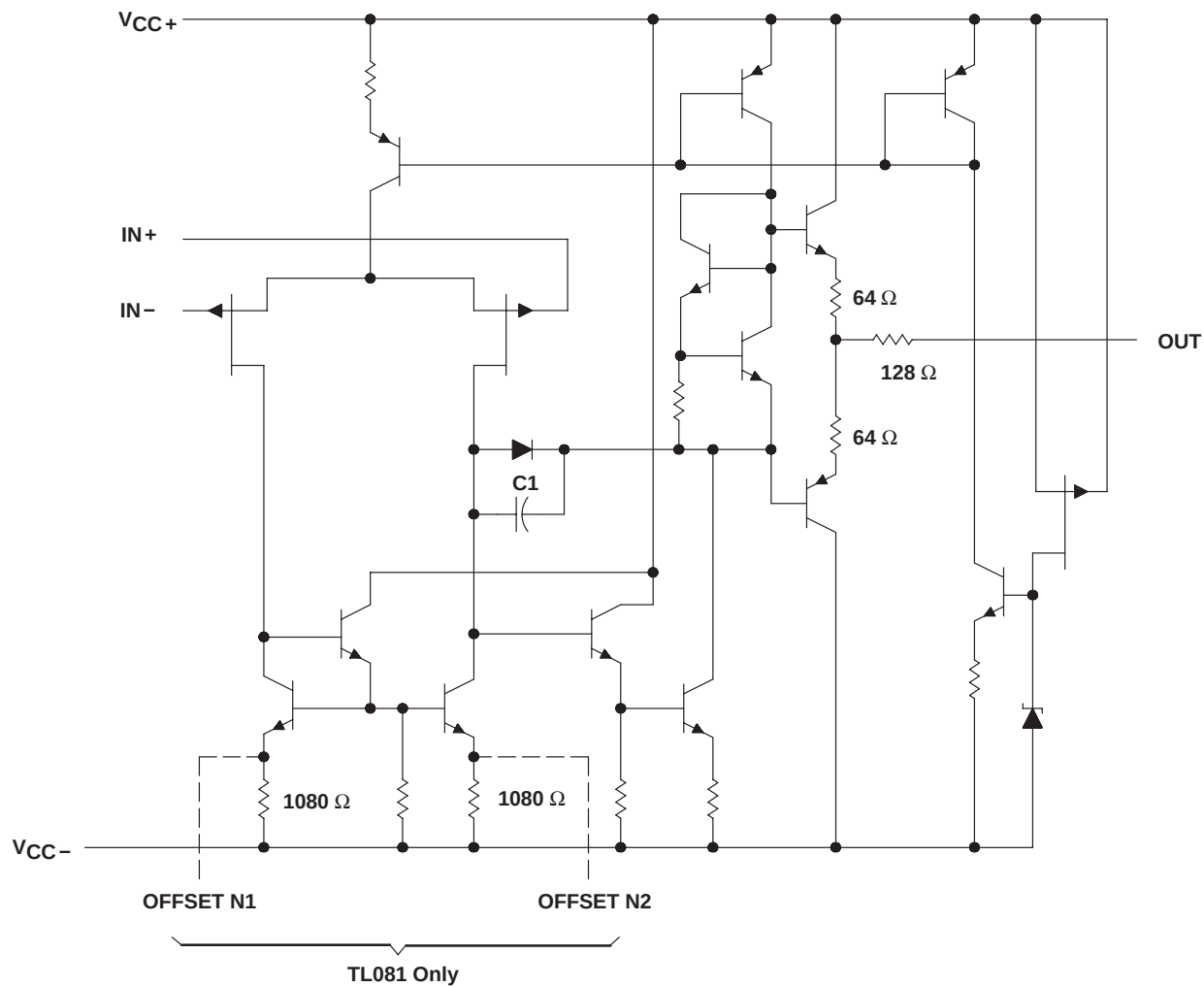
symbols



TL081, TL081A, TL081B, TL082, TL082A, TL082B TL084, TL084A, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

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schematic (each amplifier)



Component values shown are nominal.

**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

		TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	18	V
Supply voltage V_{CC-} (see Note 1)		–18	–18	–18	–18	V
Differential input voltage, V_{ID} (see Note 2)		± 30	± 30	± 30	± 30	V
Input voltage, V_I (see Notes 1 and 3)		± 15	± 15	± 15	± 15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	Unlimited	
Continuous total power dissipation		See Dissipation Rating Table				
Operating free-air temperature range, T_A		0 to 70	–40 to 85	–40 to 125	–55 to 125	°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6)	D package (8-pin)	97	97			°C/W
	D package (14-pin)	86	86			
	N package (14-pin)	76	76			
	NS package (14-pin)	80				
	P package (8-pin)	85	85			
	PS package (8-pin)	95	95			
	PW package (8-pin)	149				
	PW package (14-pin)	113	113			
Operating virtual junction temperature		150	150	150	150	°C
Case temperature for 60 seconds, T_C	FK package				260	°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J or JG package				300	°C
Storage temperature range, T_{stg}		–65 to 150	–65 to 150	–65 to 150	–65 to 150	°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .

2. Differential voltages are at $IN+$ with respect to $IN-$.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

5. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW



TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
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electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A [†]	TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081I TL082I TL084I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage V _O = 0 R _S = 50 Ω	25°C Full range	3	15	20	3	3	6	2	2	3	3	3	6	mV
α _{VIO}	Temperature coefficient of input offset voltage V _O = 0 R _S = 50 Ω	Full range		18			18			18			18		μV/°C
I _{IO}	Input offset current [‡] V _O = 0	25°C Full range	5	200		5	5	100	5	5	100	5	5	100	pA
I _{IB}	Input bias current [‡] V _O = 0	25°C Full range	30	400	10	30	30	200	30	30	200	30	30	200	nA
V _{ICR}	Common-mode input voltage range	25°C	±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		V
V _{OM}	Maximum peak output voltage swing	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	R _L = 10 kΩ	Full range	±10	±12		±10	±12		±10	±12		±10	±12		
	R _L ≥ 10 kΩ														
A _{VD}	Large-signal differential voltage amplification	25°C	25	200		25	200		50	200		50	200		V/mV
	V _O = ±10 V, R _L ≥ 2 kΩ	Full range	15			25			25			25			
B ₁	Unity-gain bandwidth	25°C		3			3			3			3		MHz
r _i	Input resistance	25°C		10 ¹²			10 ¹²			10 ¹²			10 ¹²		Ω
CMRR	Common-mode rejection ratio	25°C	70	86		75	86		75	86		75	86		dB
KSVR	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	25°C	70	86		80	86		80	86		80	86		dB
I _{CC}	Supply current (per amplifier)	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V _{O1} /V _{O2}	Crosstalk attenuation	25°C		120			120			120			120		dB

[†] All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and -40°C to 85°C for TL08_I.

[‡] Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

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electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C		3	6		3	9	mV
		Full range			9			15	
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range		18			18		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current [‡]	$V_O = 0$	25°C		5	100		5	100	pA
		125°C			20			20	nA
I_{IB} Input bias current [‡]	$V_O = 0$	25°C		30	200		30	200	pA
		125°C			50			50	nA
V_{ICR} Common-mode input voltage range		25°C	± 11	–12 to 15		± 11	–12 to 15		V
V_{OM} Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$	25°C	± 12	± 13.5		± 12	± 13.5		V
	$R_L \geq 10\text{ k}\Omega$	Full range	± 12			± 12			
	$R_L \geq 2\text{ k}\Omega$		± 10	± 12		± 10	± 12		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, R_L \geq 2\text{ k}\Omega$	25°C	25	200		25	200		V/mV
	$V_O = \pm 10\text{ V}, R_L \geq 2\text{ k}\Omega$	Full range	15			15			
B_1 Unity-gain bandwidth		25°C		3			3		MHz
r_i Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15\text{ V to } \pm 9\text{ V}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
I_{CC} Supply current (per amplifier)	$V_O = 0, \text{ No load}$	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

[†] All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

[‡] Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15\text{ V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V _I = 10 V,	R _L = 2 kΩ,	C _L = 100 pF,	See Figure 1	8*	13		V/μs
		V _I = 10 V, T _A = − 55°C to 125°C,	R _L = 2 kΩ,	C _L = 100 pF,	See Figure 1	5*			
t _r	Rise time	V _I = 20 mV, R _L = 2 kΩ, C _L = 100 pF, See Figure 1				0.05			μs
	Overshoot factor					20			%
V _n	Equivalent input noise voltage	R _S = 20 Ω	f = 1 kHz			18			nV/√Hz
			f = 10 Hz to 10 kHz			4			μV
I _n	Equivalent input noise current	R _S = 20 Ω,	f = 1 kHz			0.01			pA/√Hz
THD	Total harmonic distortion	V _{Irms} = 6 V, f = 1 kHz	A _{VD} = 1,	R _S ≤ 1 kΩ,	R _L ≥ 2 kΩ,	0.003			%

*On products compliant to MIL-PRF-38535, this parameter is not production tested.



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TL084, TL084A, TL084B
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operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10\text{ V}$,	$R_L = 2\text{ k}\Omega$,	$C_L = 100\text{ pF}$,	See Figure 1	8	13		$\text{V}/\mu\text{s}$
t_r	Rise time	$V_I = 20\text{ mV}$,	$R_L = 2\text{ k}\Omega$,	$C_L = 100\text{ pF}$,	See Figure 1		0.05		μs
	Overshoot factor						20		%
V_n	Equivalent input noise voltage	$R_S = 20\text{ }\Omega$	$f = 1\text{ kHz}$				18		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 10\text{ Hz to }10\text{ kHz}$				4		μV
I_n	Equivalent input noise current	$R_S = 20\text{ }\Omega$,	$f = 1\text{ kHz}$				0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{I\text{rms}} = 6\text{ V}$, $f = 1\text{ kHz}$	$A_{VD} = 1$,	$R_S \leq 1\text{ k}\Omega$,	$R_L \geq 2\text{ k}\Omega$,		0.003		%

PARAMETER MEASUREMENT INFORMATION

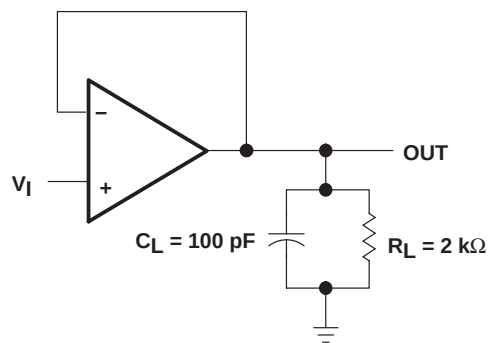


Figure 1

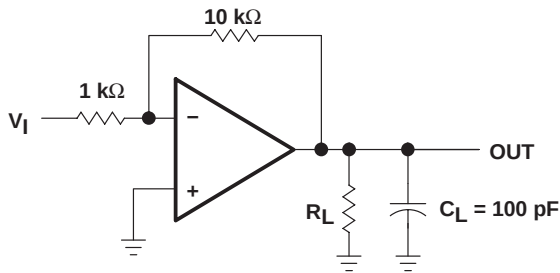


Figure 2

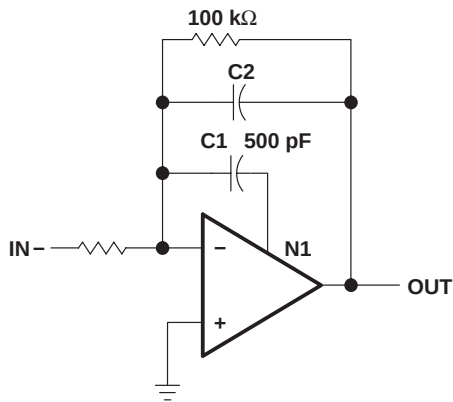


Figure 3

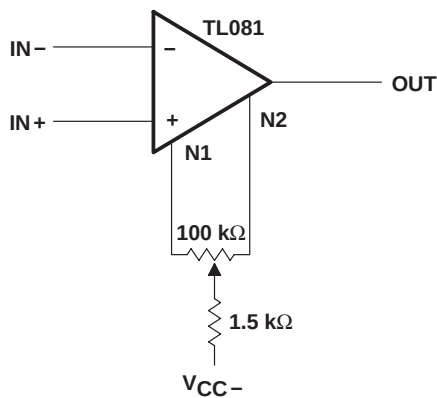


Figure 4

TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

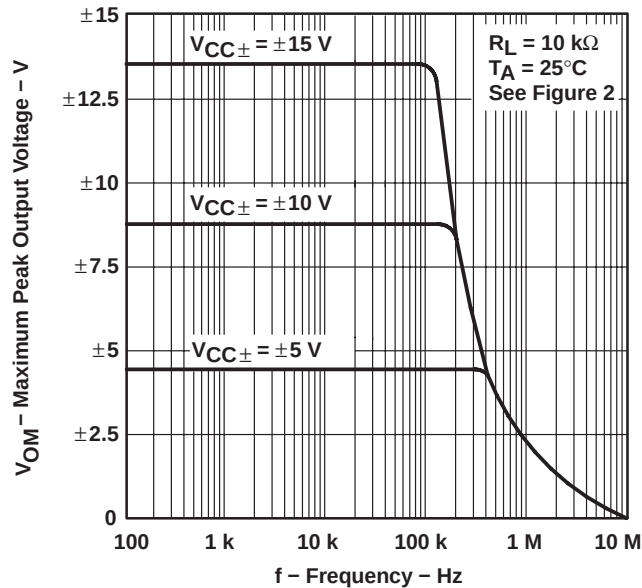
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TYPICAL CHARACTERISTICS

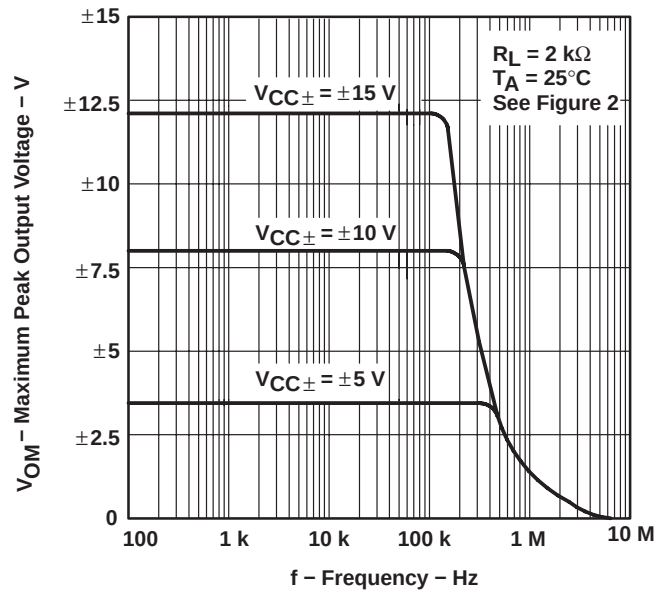
Table of Graphs

		FIGURE
V_{OM}	Maximum peak output voltage	5, 6, 7
		8
		9
		10
A_{VD}	Large-signal differential voltage amplification	11
		12
	Differential voltage amplification	13
P_D	Total power dissipation	14
I_{CC}	Supply current	15
		16
I_{IB}	Input bias current	17
	Large-signal pulse response	18
V_O	Output voltage	19
CMRR	Common-mode rejection ratio	20
V_n	Equivalent input noise voltage	21
THD	Total harmonic distortion	22

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY**



**MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY**



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TYPICAL CHARACTERISTICS†

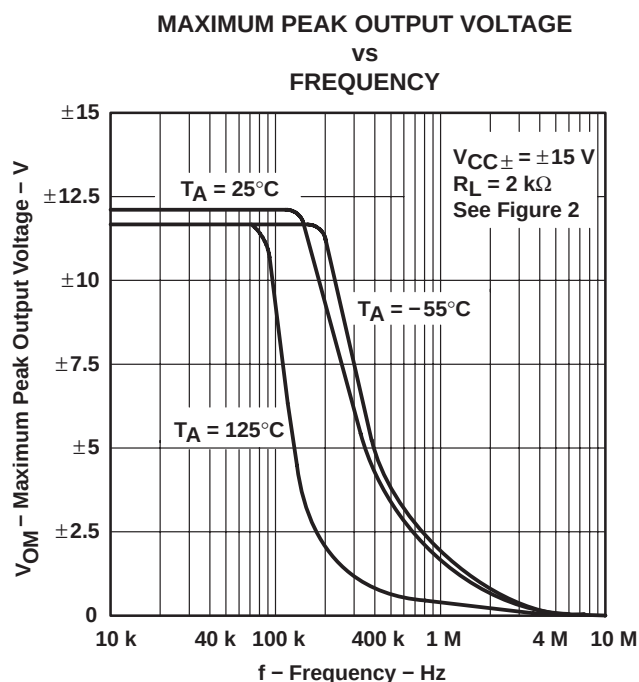


Figure 7

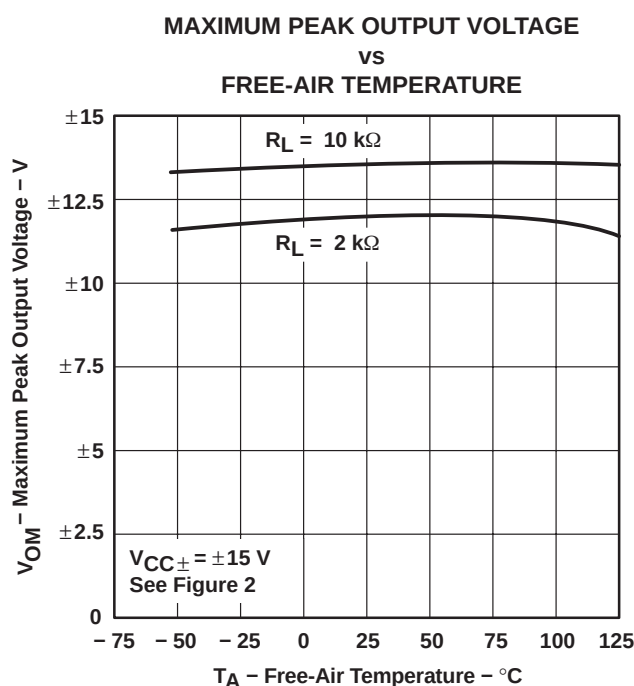


Figure 8

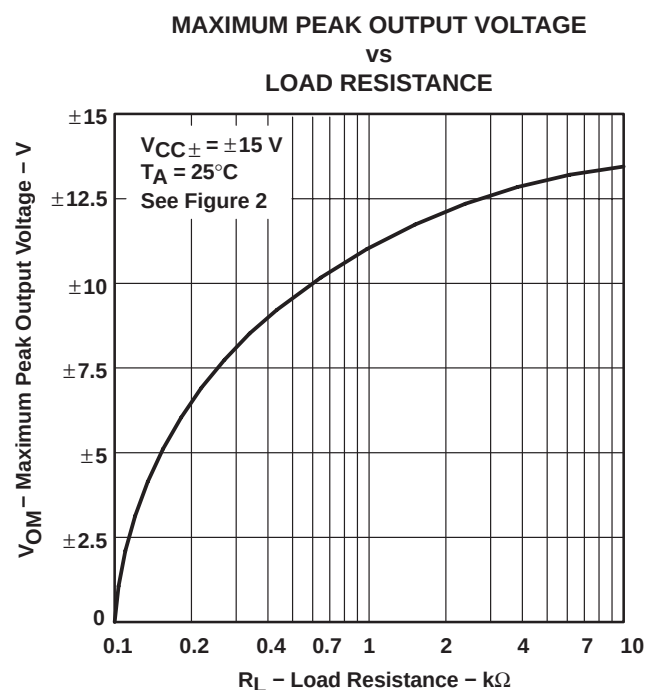


Figure 9

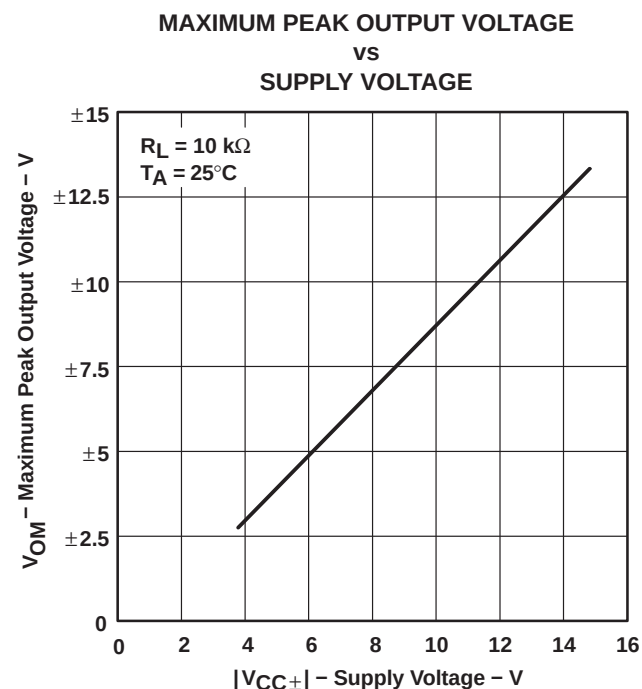


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

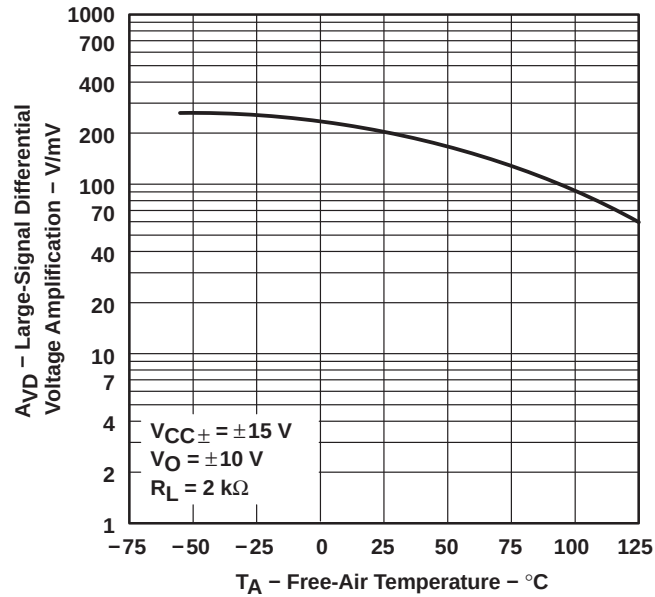


Figure 11

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREQUENCY

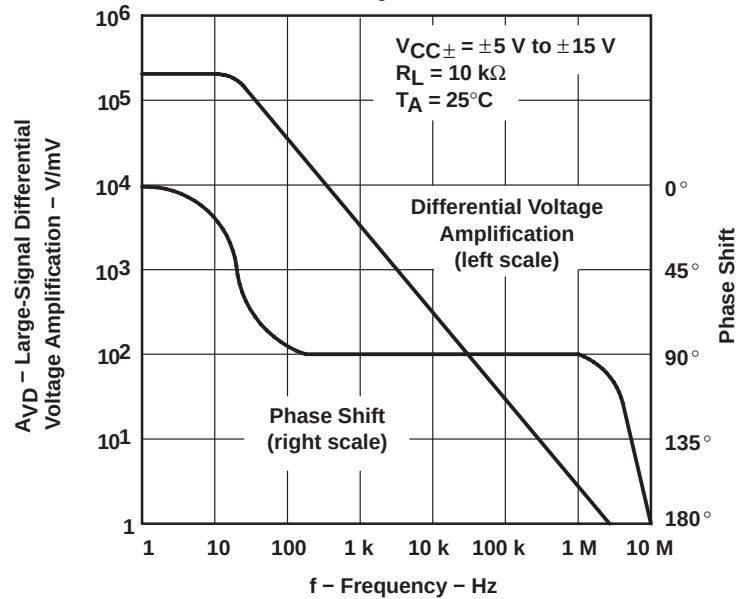


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION

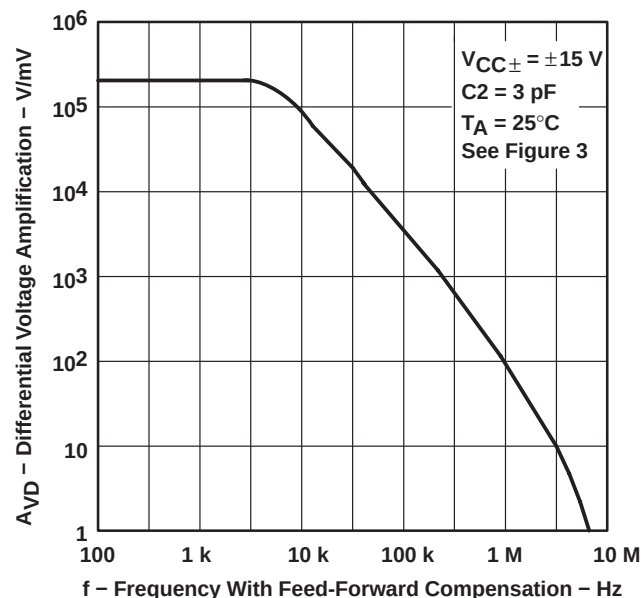


Figure 13

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

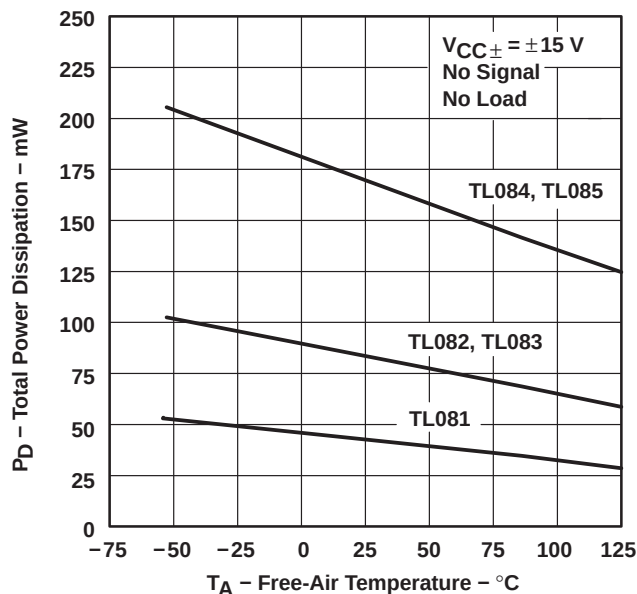


Figure 14

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

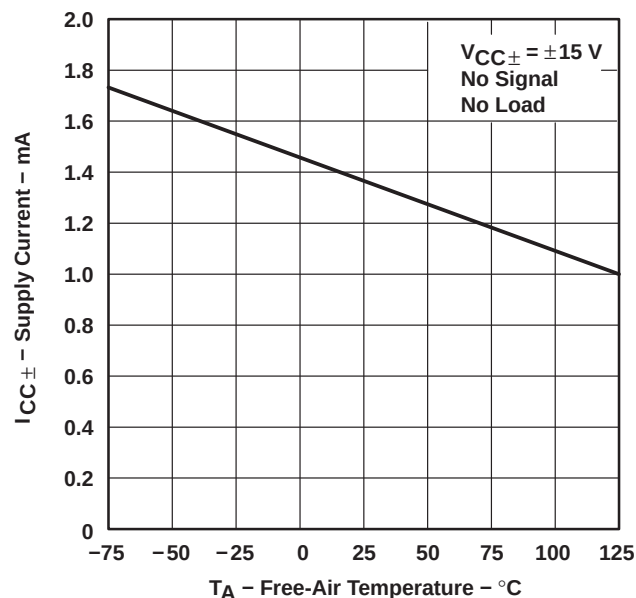


Figure 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

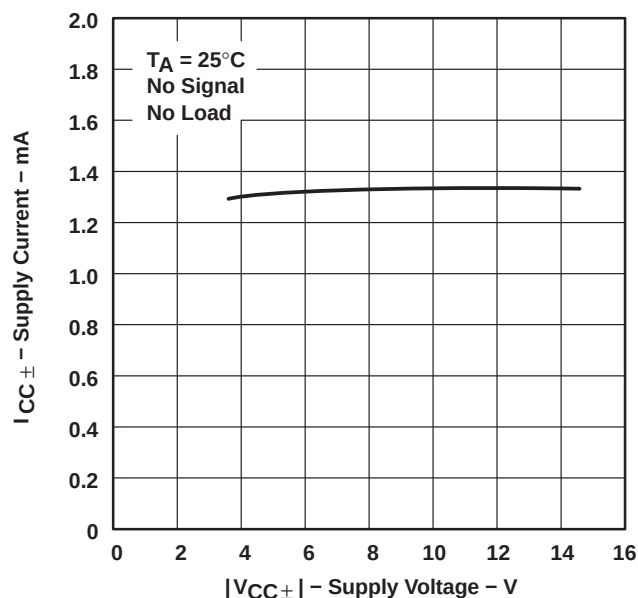


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

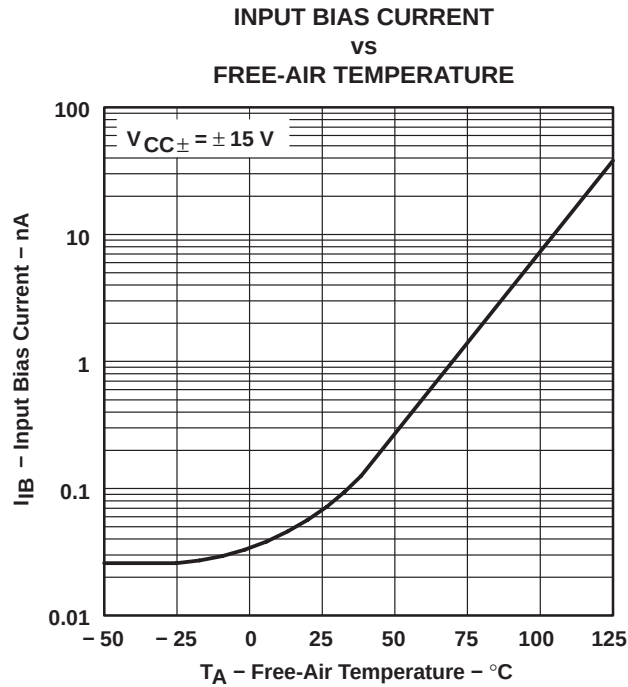


Figure 17

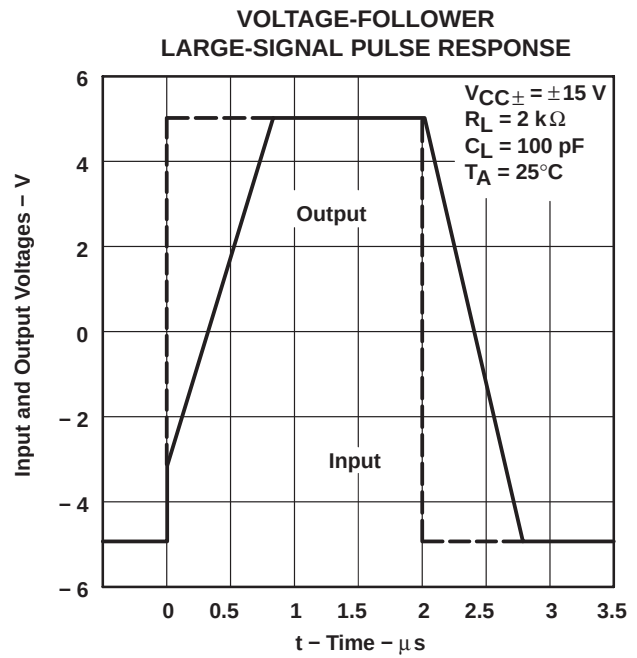


Figure 18

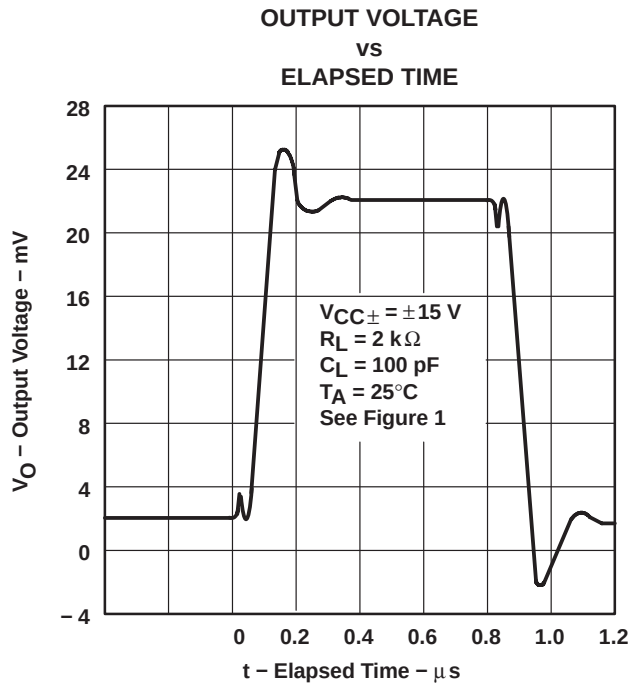


Figure 19

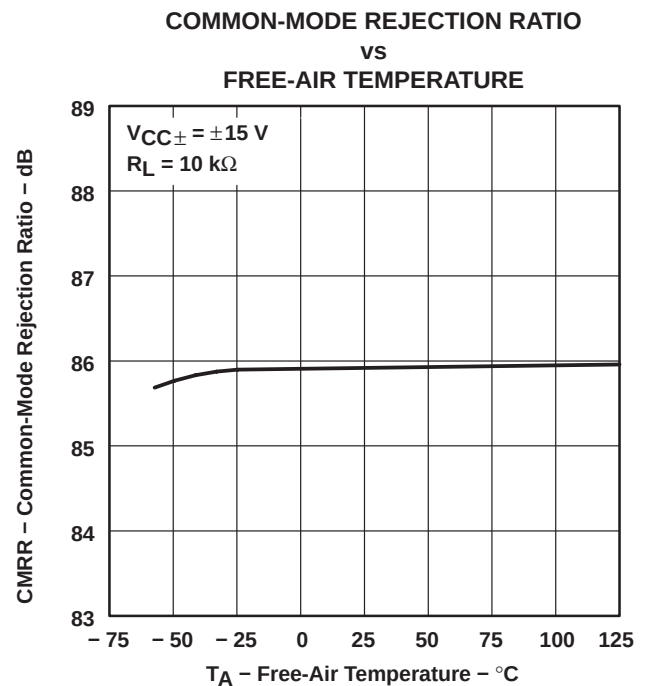


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TL081, TL081A, TL081B, TL082, TL082A, TL082B TL084, TL084A, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

TYPICAL CHARACTERISTICS†

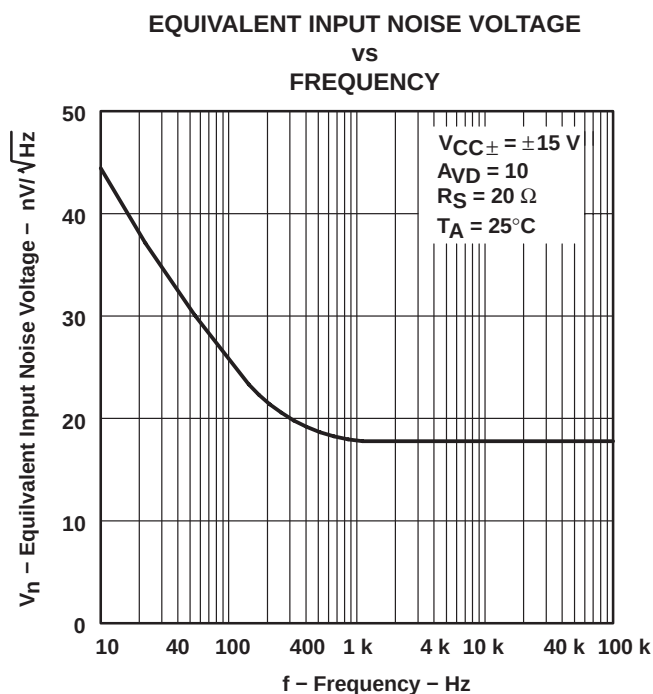


Figure 21

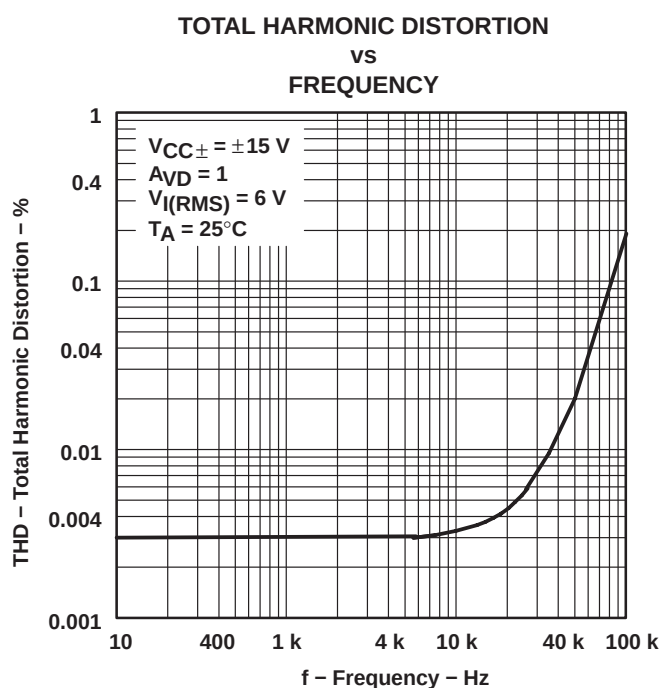


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

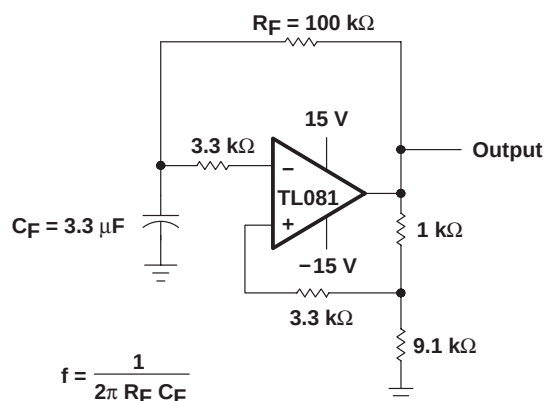


Figure 23

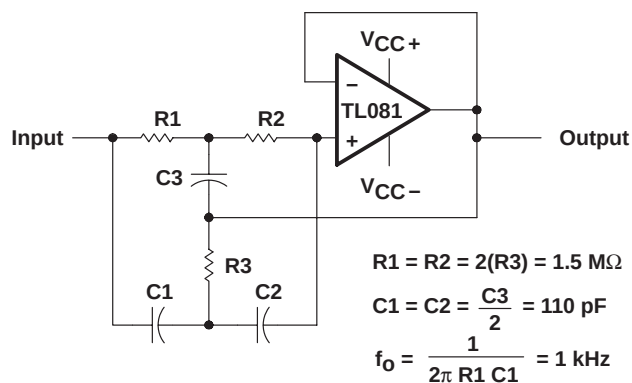


Figure 24

APPLICATION INFORMATION

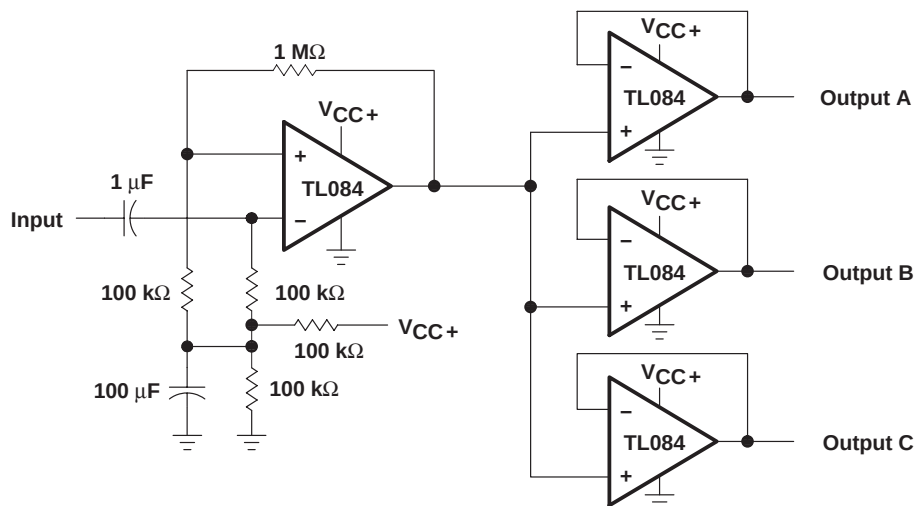
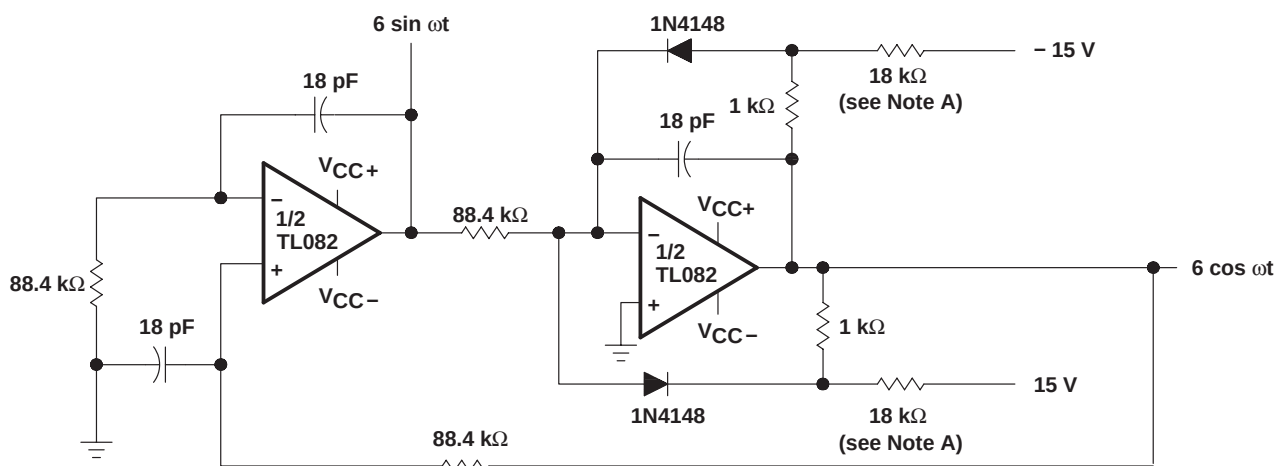


Figure 25. Audio-Distribution Amplifier



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

APPLICATION INFORMATION

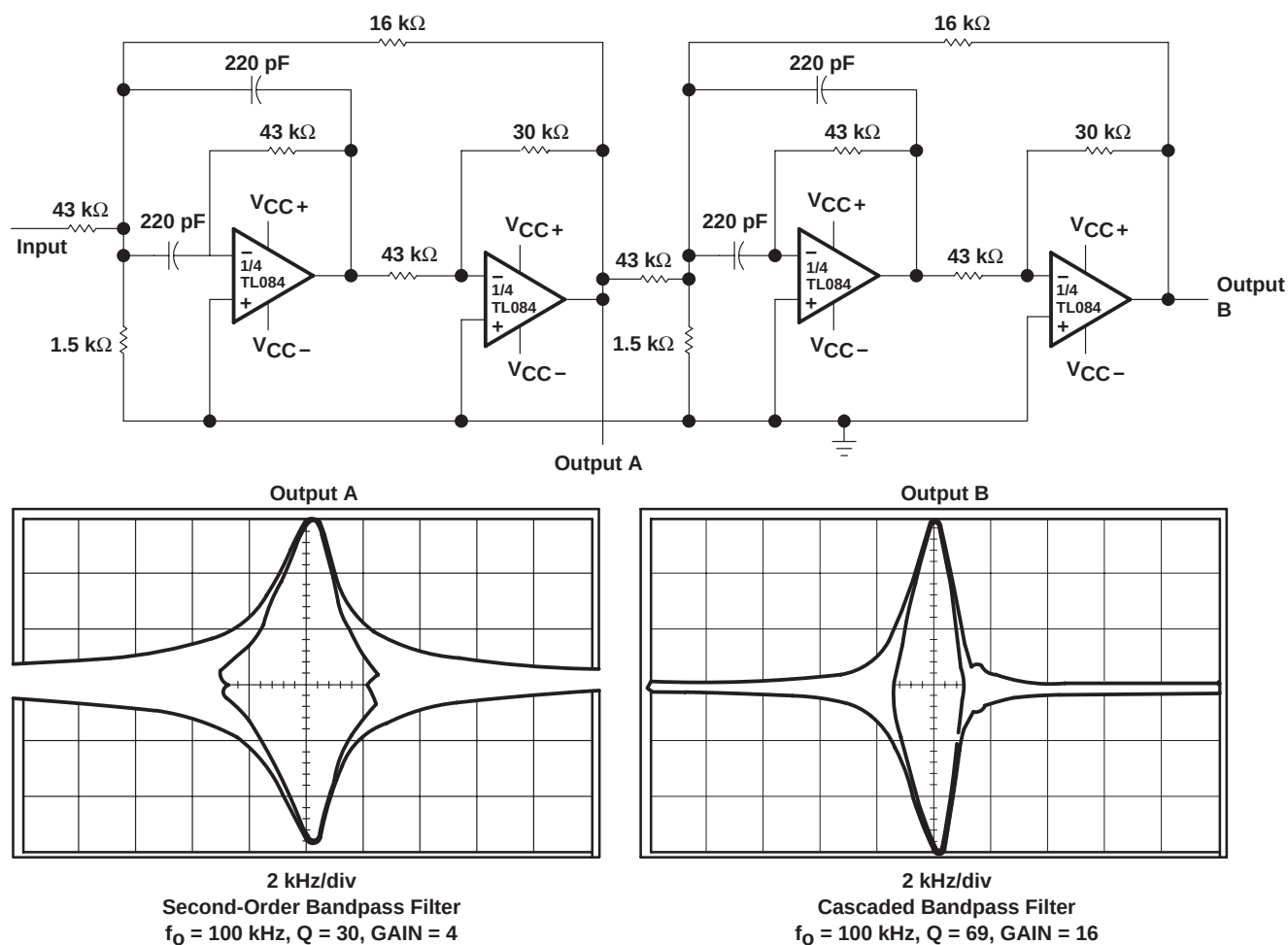


Figure 27. Positive-Feedback Bandpass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9851501Q2A TL082MFKB	Samples
5962-9851501QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
5962-9851503Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9851503Q2A TL084 MFKB	Samples
5962-9851503QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	Samples
TL081ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
TL081ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	Samples
TL081ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	Samples
TL081BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL081BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples
TL081CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples
TL081CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	Samples
TL081CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	Samples
TL081CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	Samples
TL081CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL081ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL081IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL081IP	Samples
TL081IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL081IP	Samples
TL081MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL081MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL081MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL082ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	Samples
TL082ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	Samples
TL082ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082ACPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	Samples
TL082ACPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	Samples
TL082BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
TL082CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	Samples
TL082CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-40 to 85		
TL082IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples
TL082IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082MFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL082MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9851501Q2A TL082MFKB	Samples
TL082MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL082MJG	Samples
TL082MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
TL084ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084ACN	Samples
TL084ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084ACN	Samples
TL084ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples
TL084ACNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples
TL084ACNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
TL084CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI	0 to 70		
TL084CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	Samples
TL084CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70		
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-40 to 85		
TL084IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL084MFK	Samples
TL084MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9851503Q2A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										TL084 MFKB	
TL084MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TL084MJ	Samples
TL084MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	Samples
TL084QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

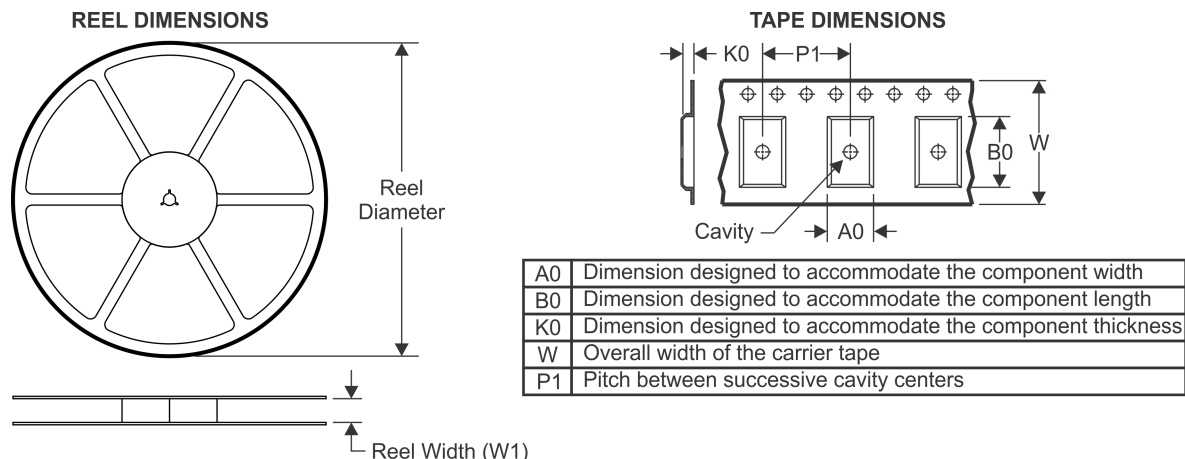
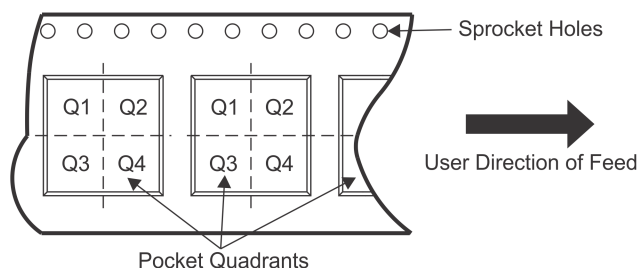
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

- Catalog: [TL082](#), [TL084](#)
- Automotive: [TL082-Q1](#), [TL082-Q1](#)
- Military: [TL082M](#), [TL084M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

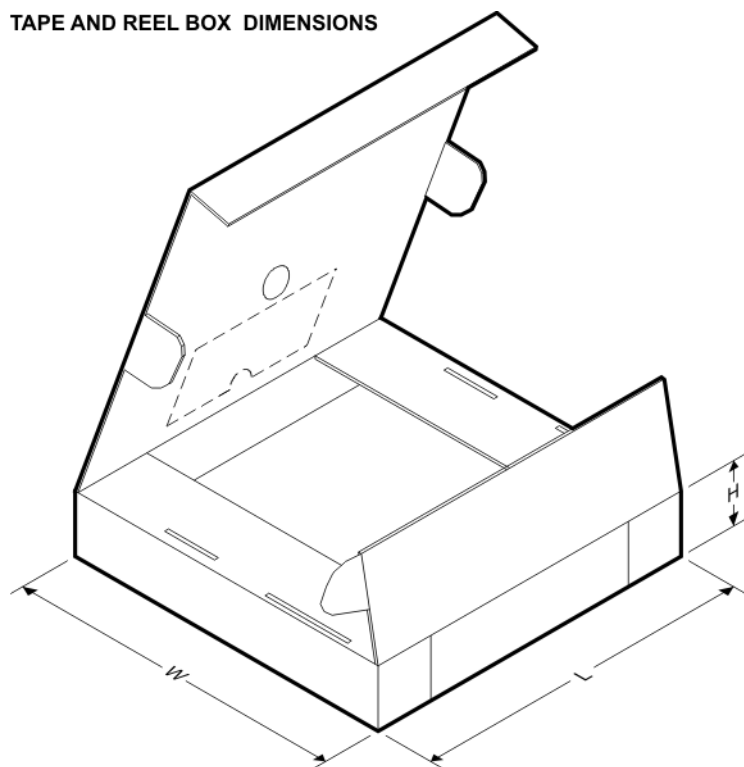
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



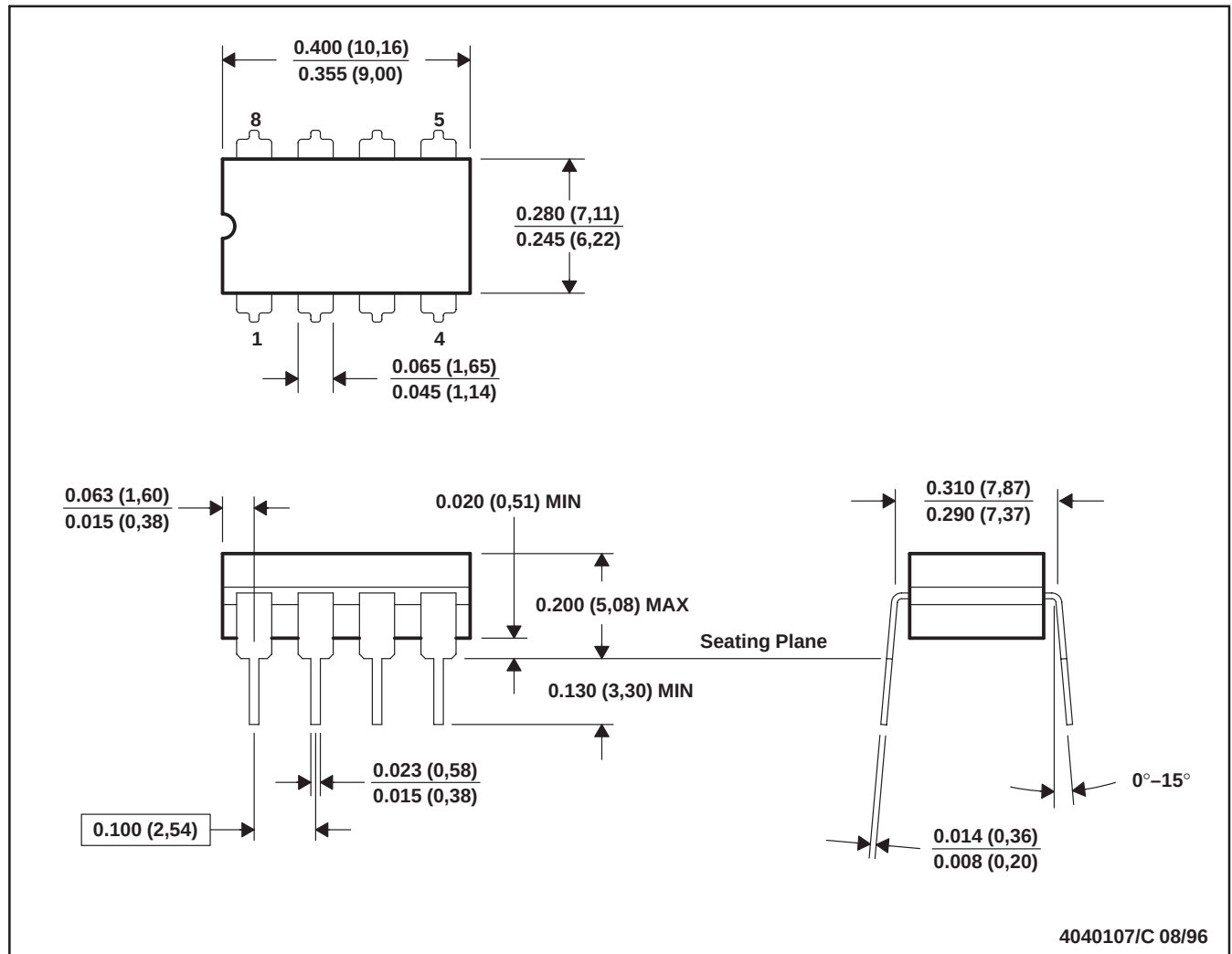
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL081IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL082BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL084ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL084BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL084CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL084IDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084QDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084QDRG4	SOIC	D	14	2500	367.0	367.0	38.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

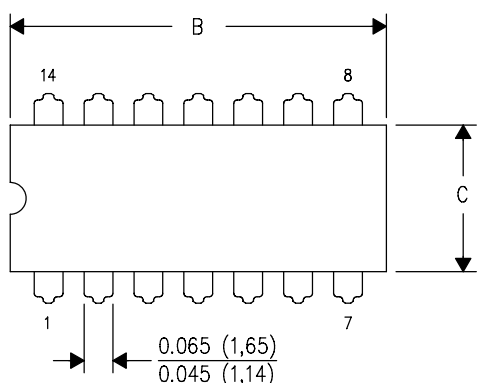


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

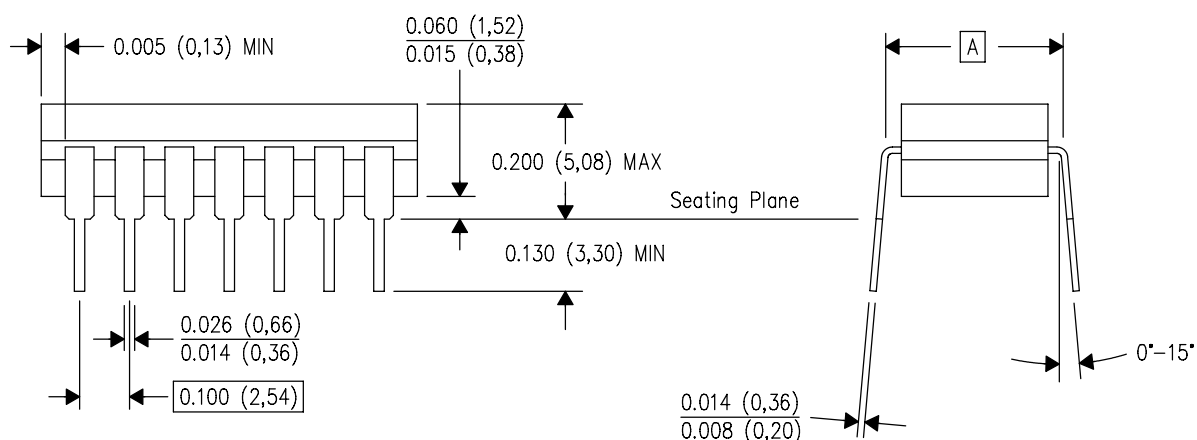
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



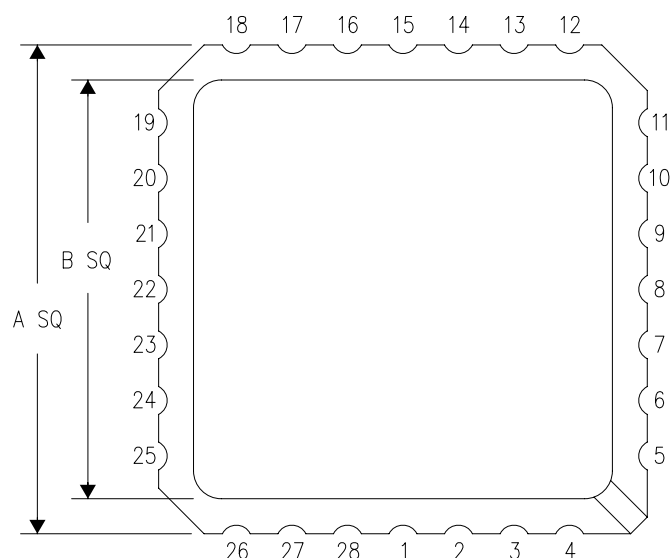
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

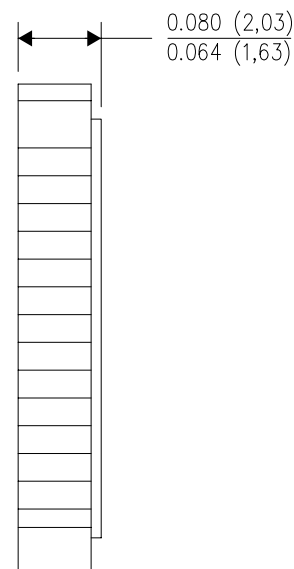
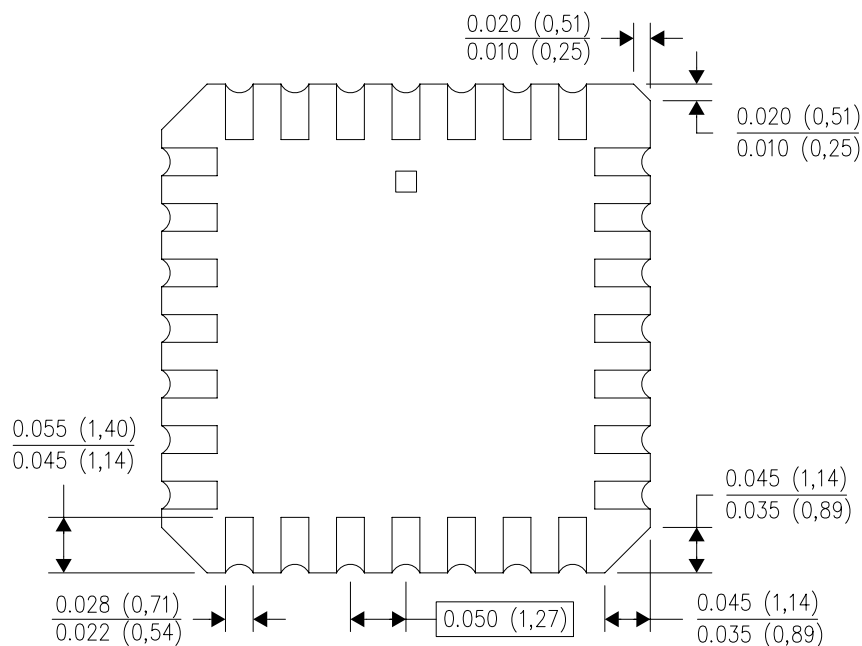
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

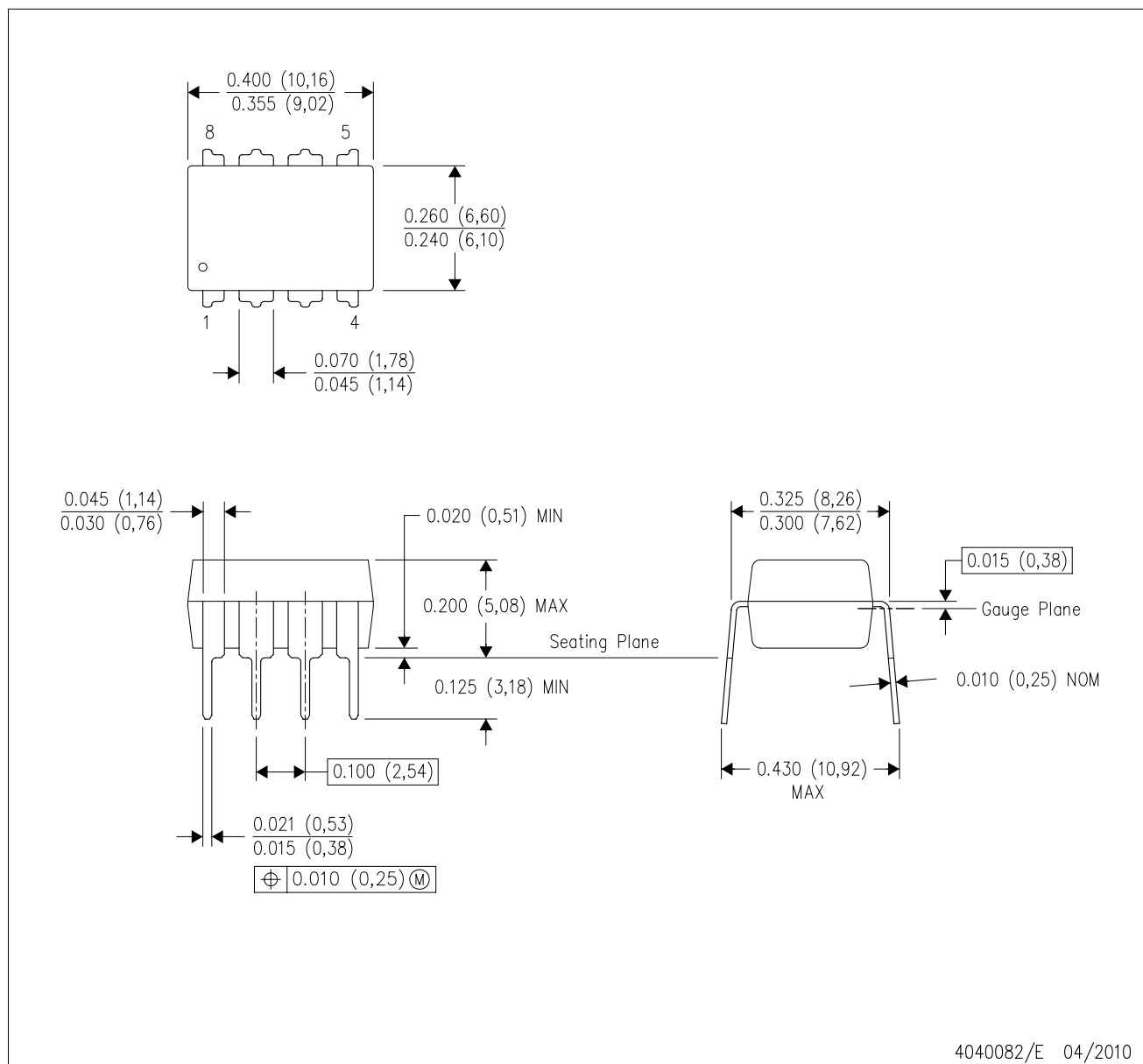


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



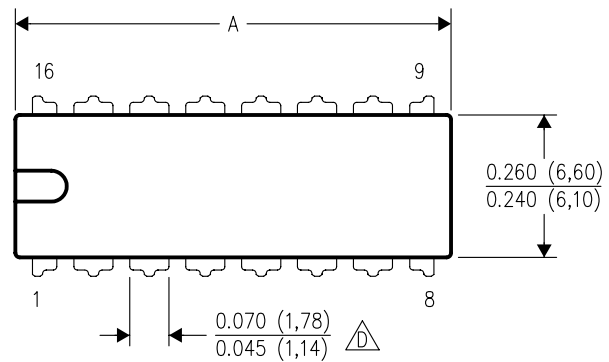
4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

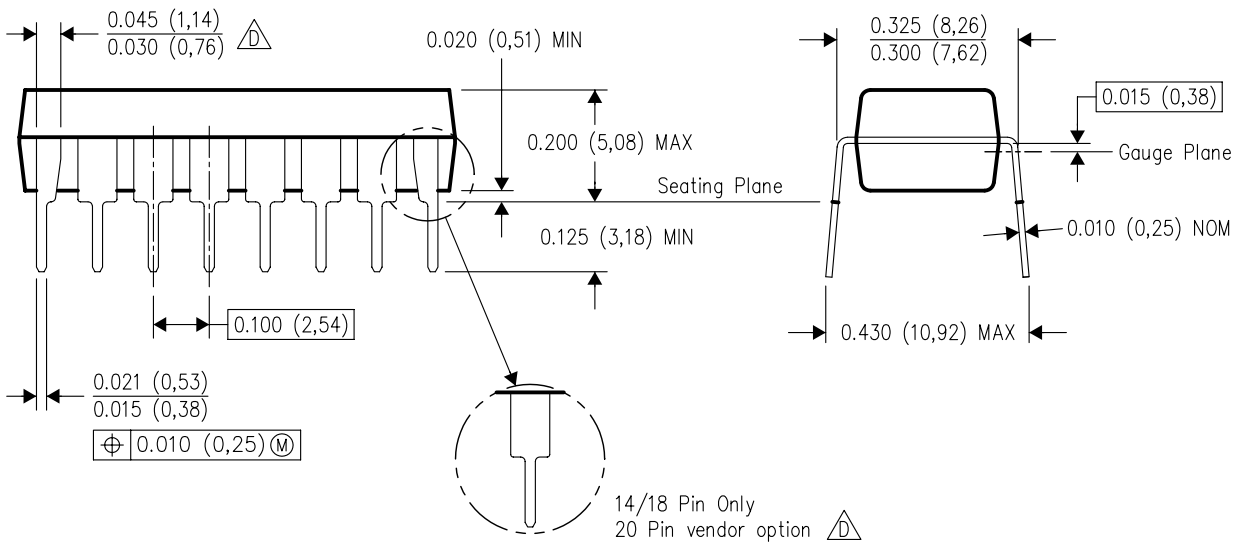
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

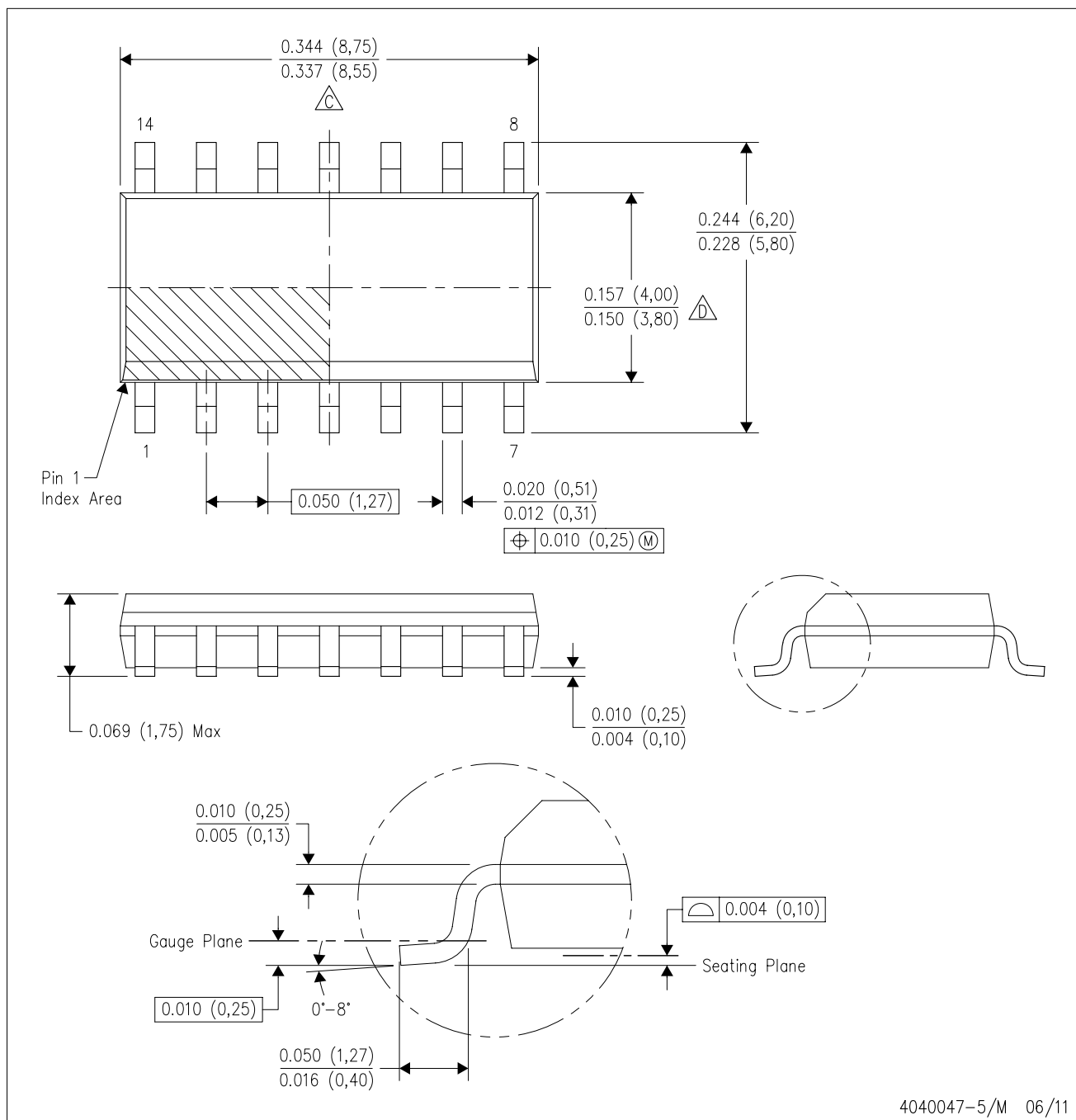


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

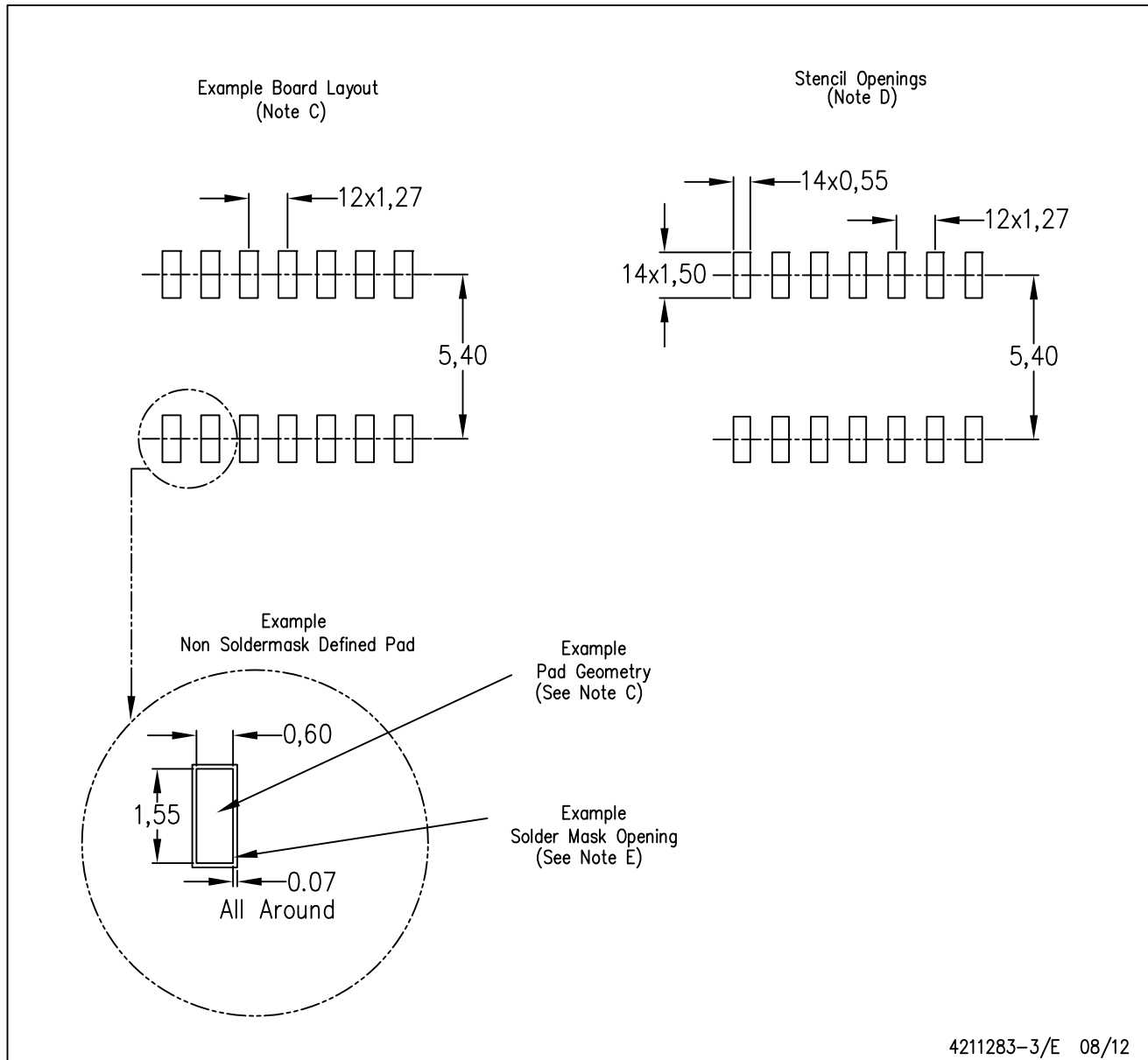


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

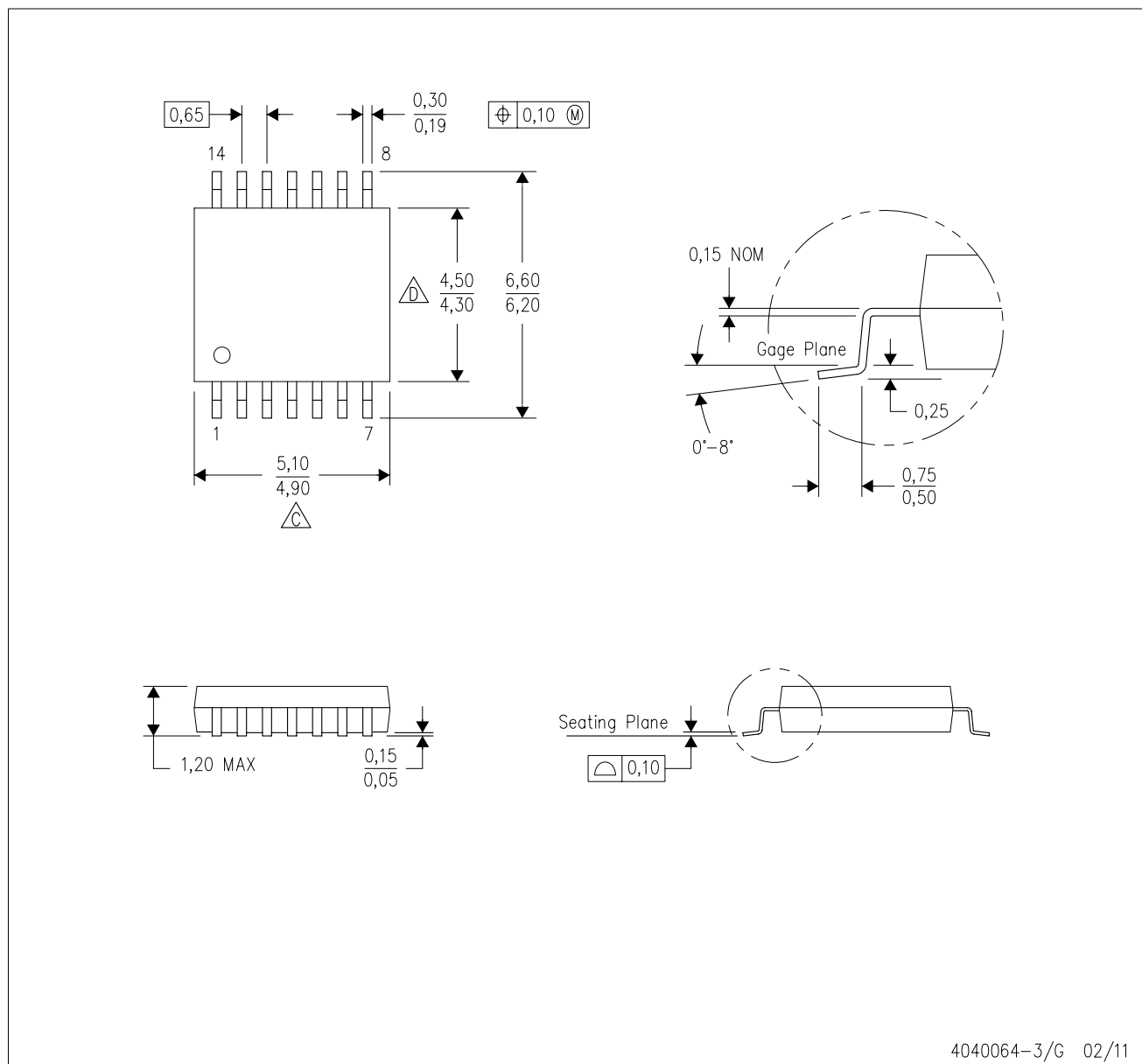
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

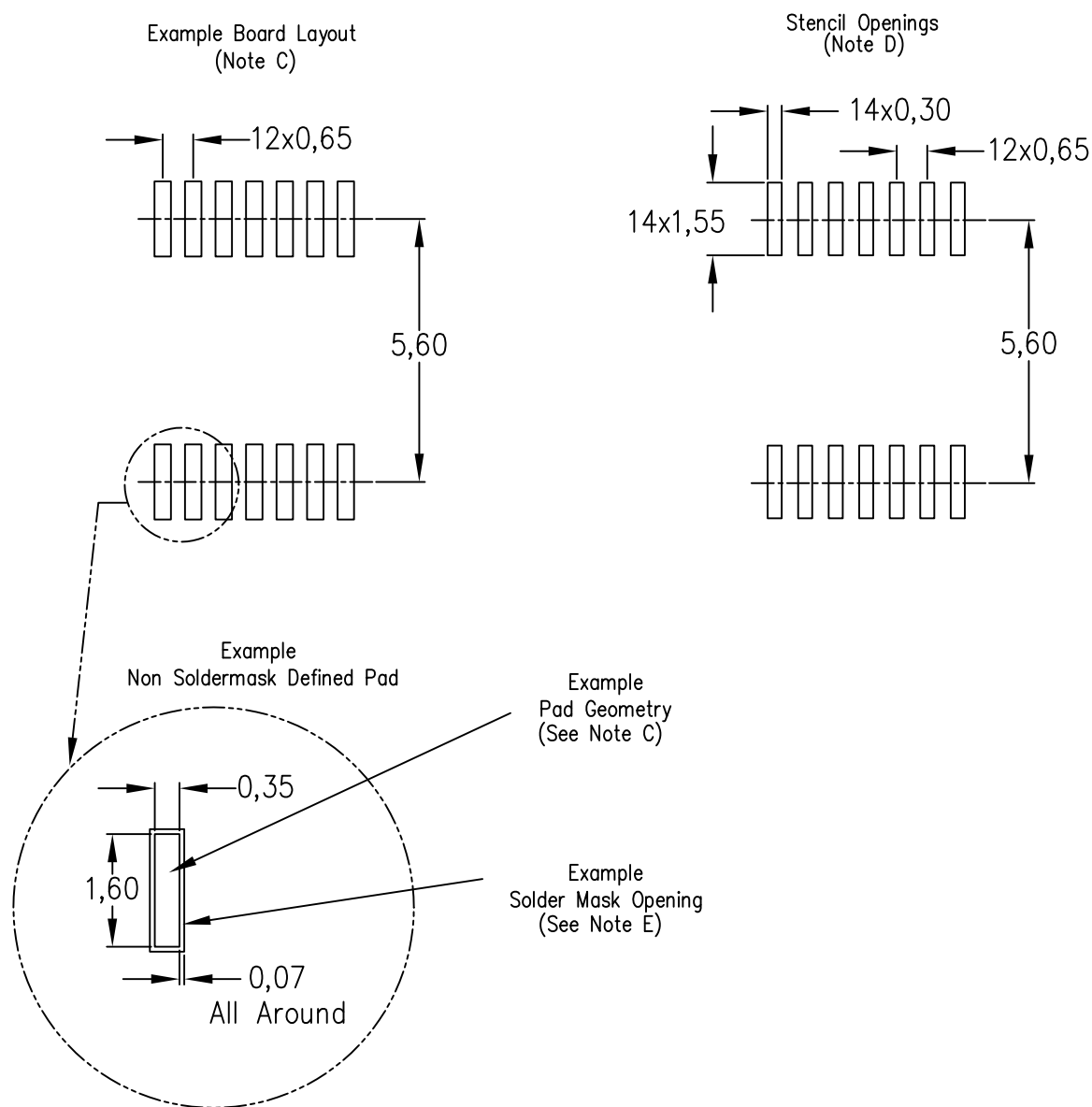


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

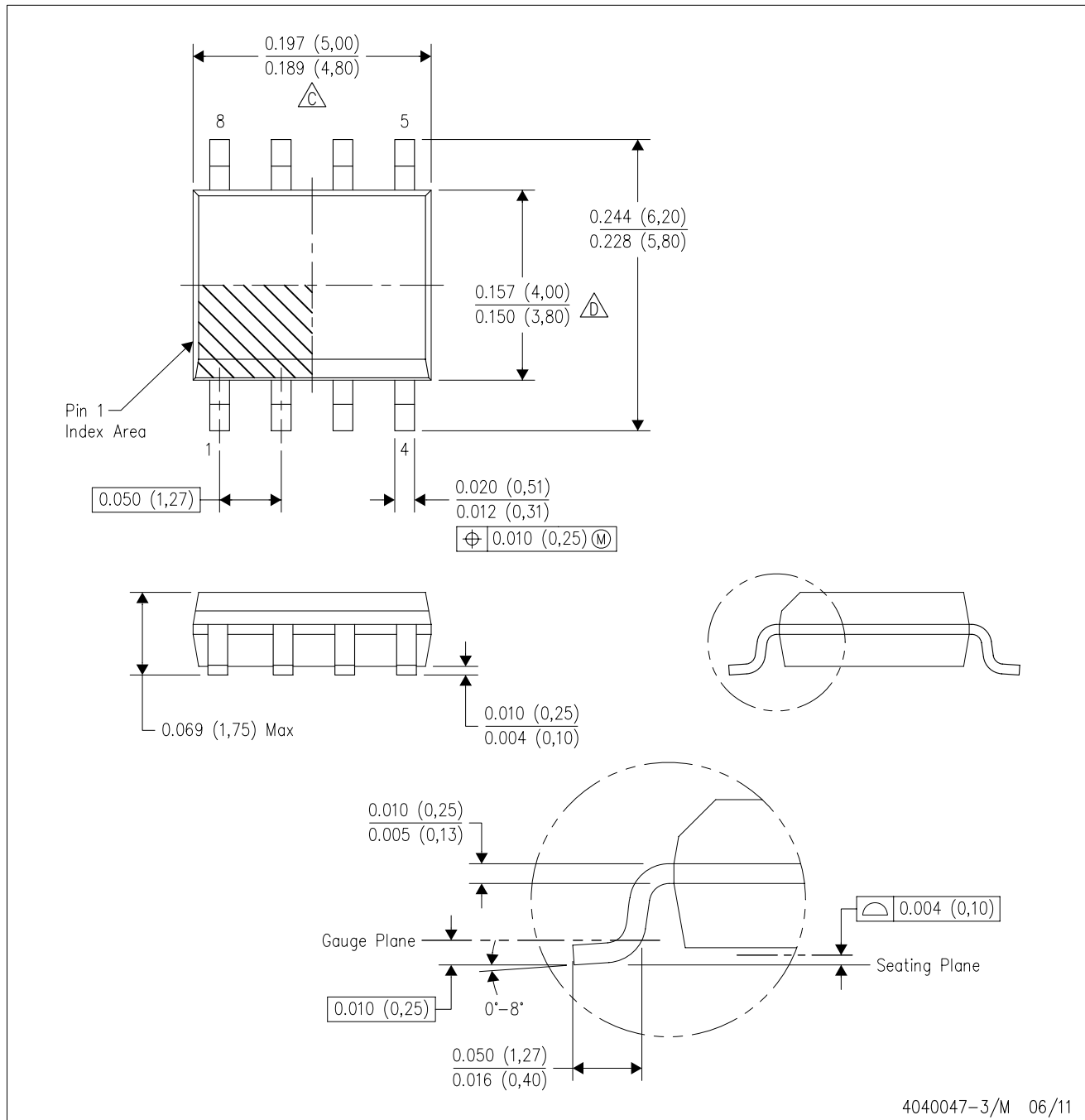


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

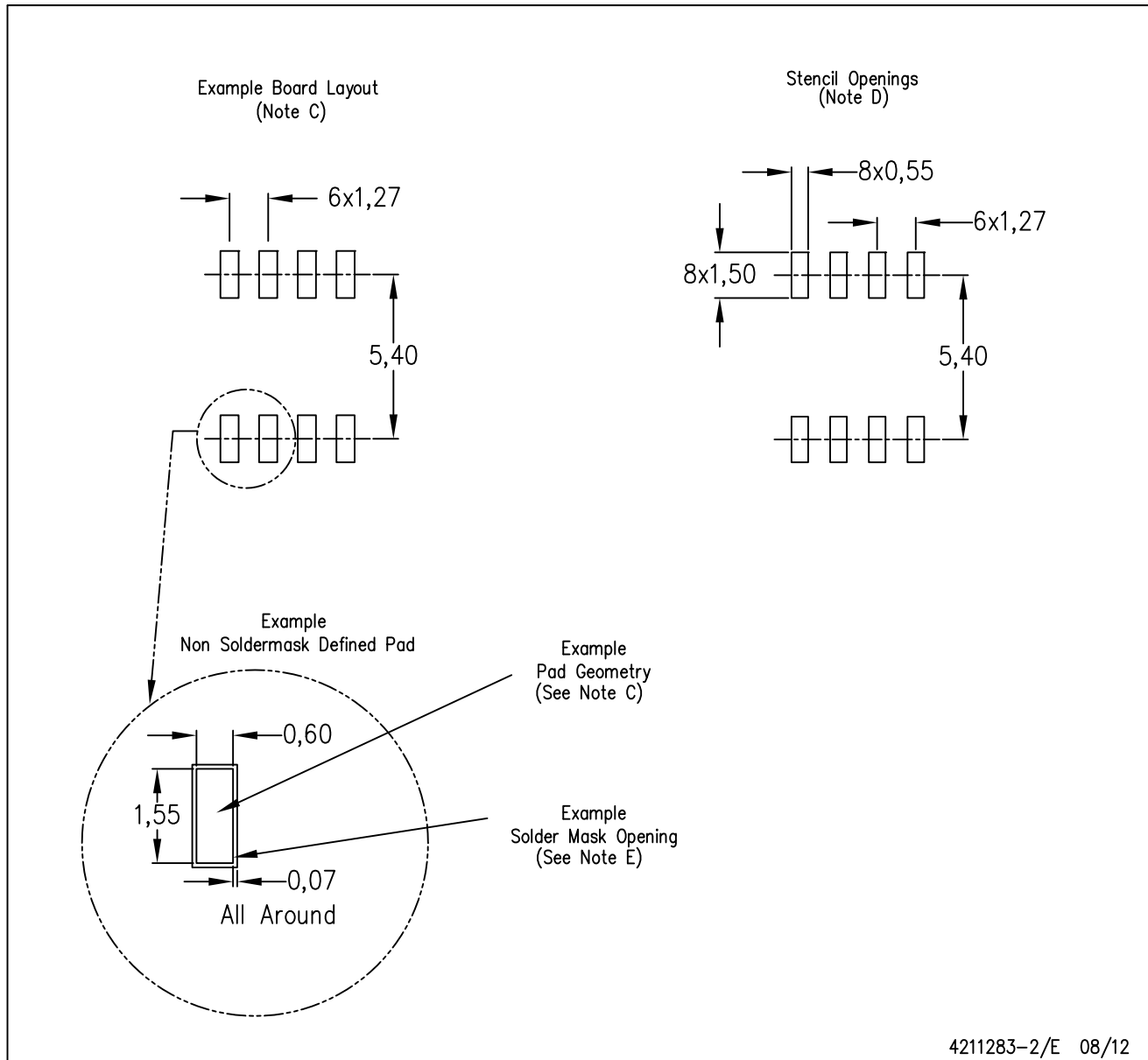
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

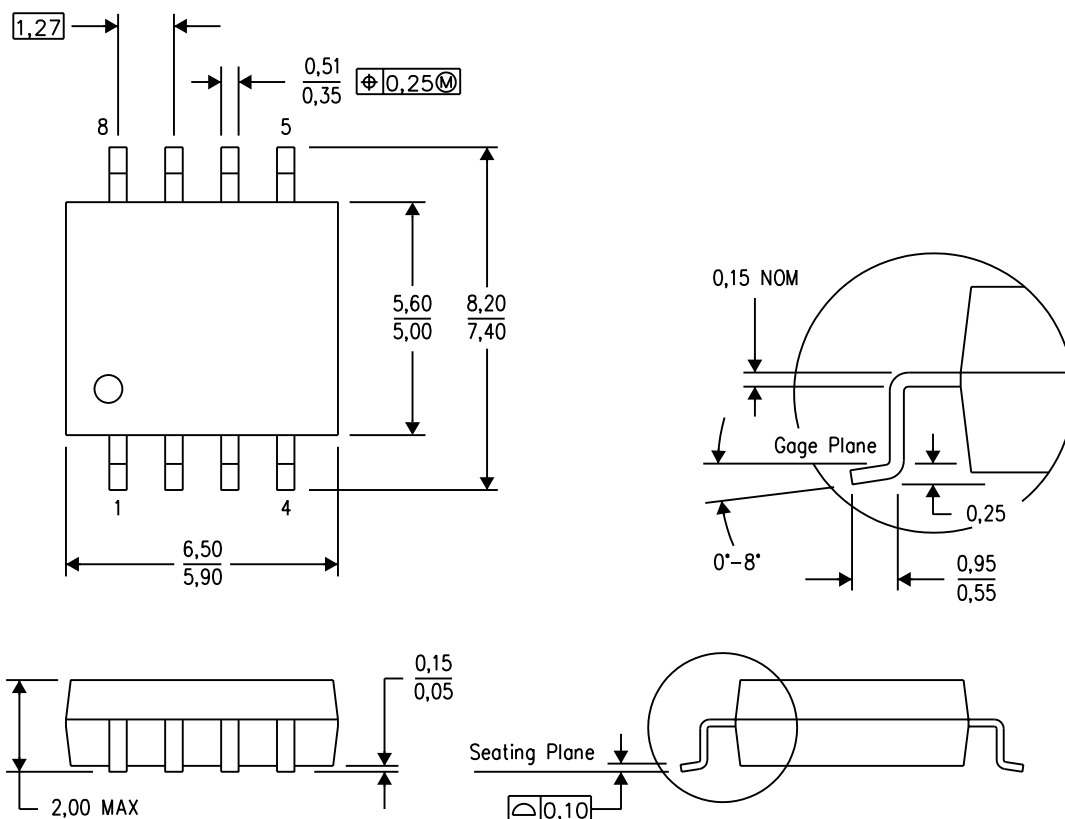


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

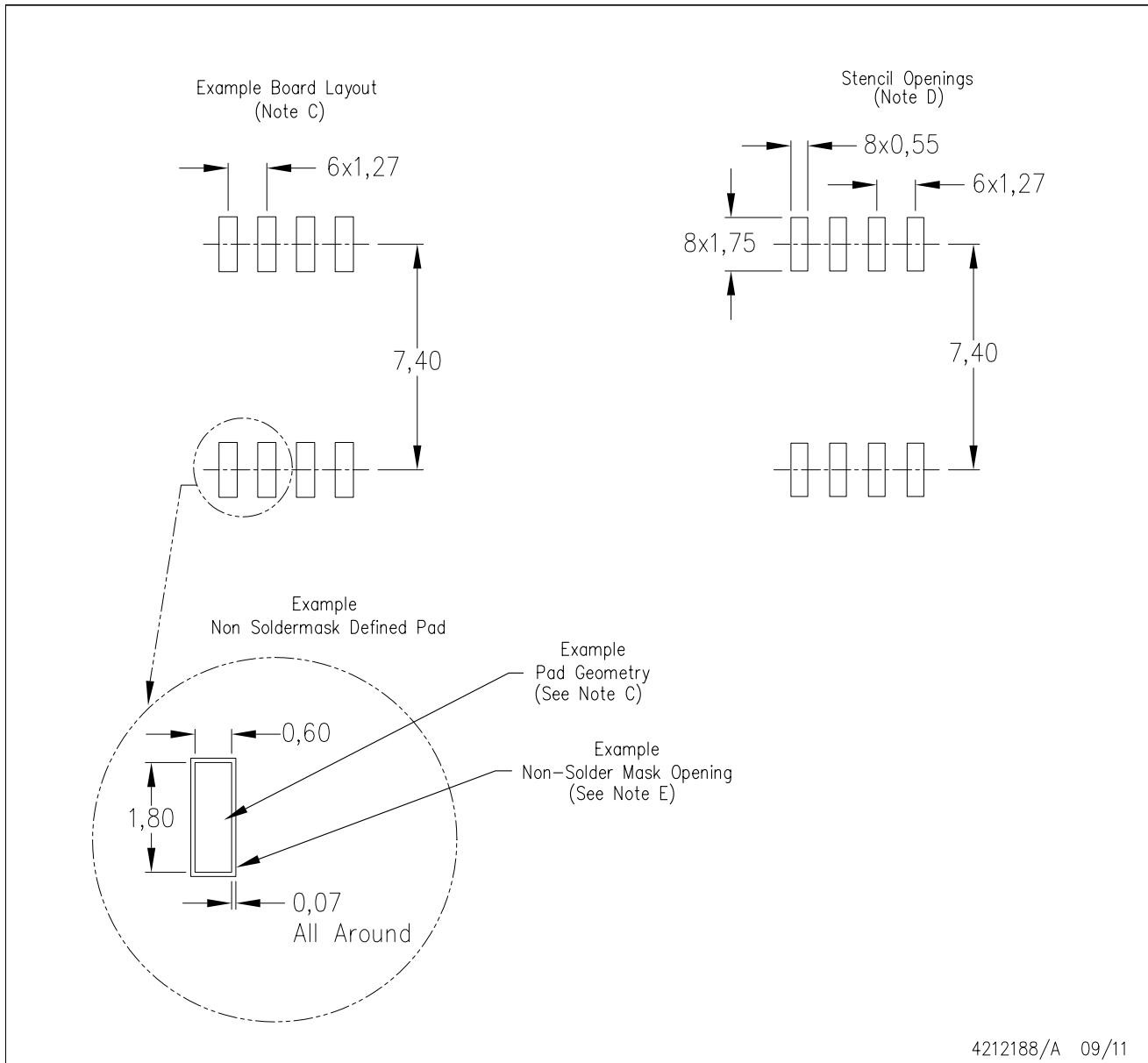


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



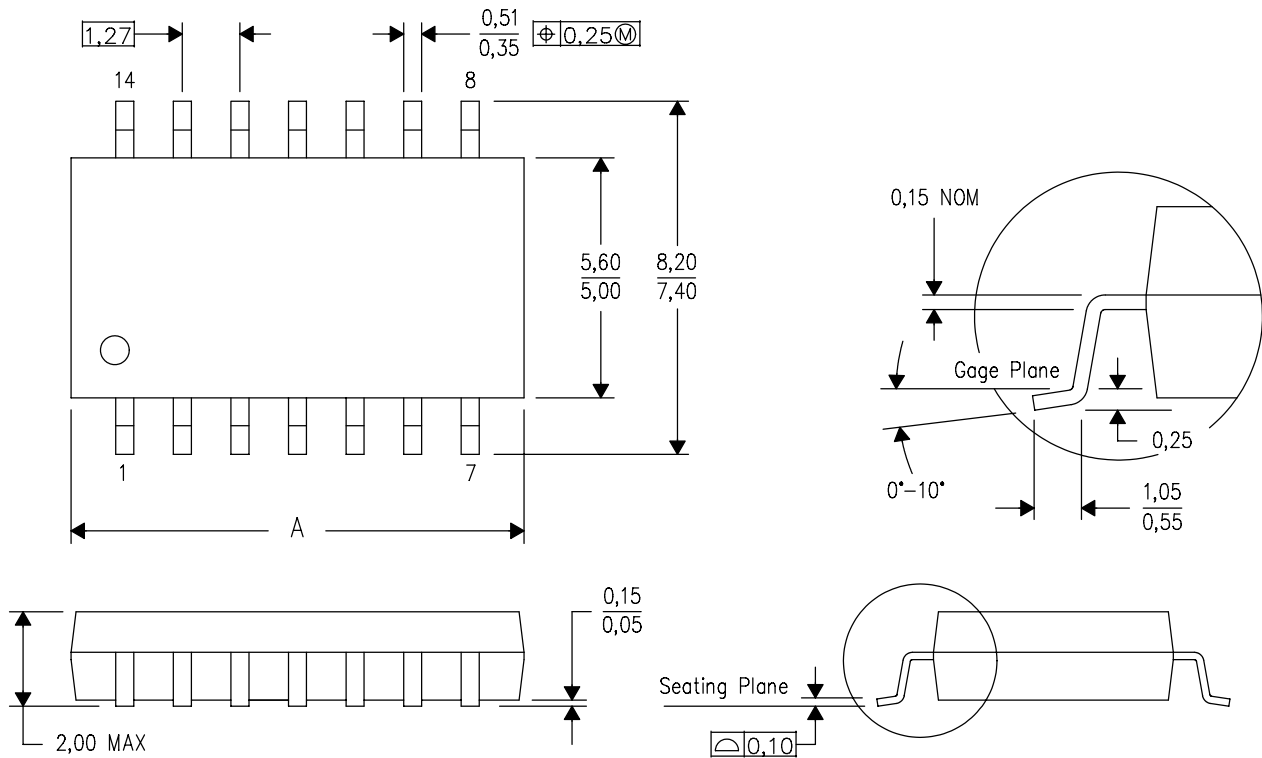
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



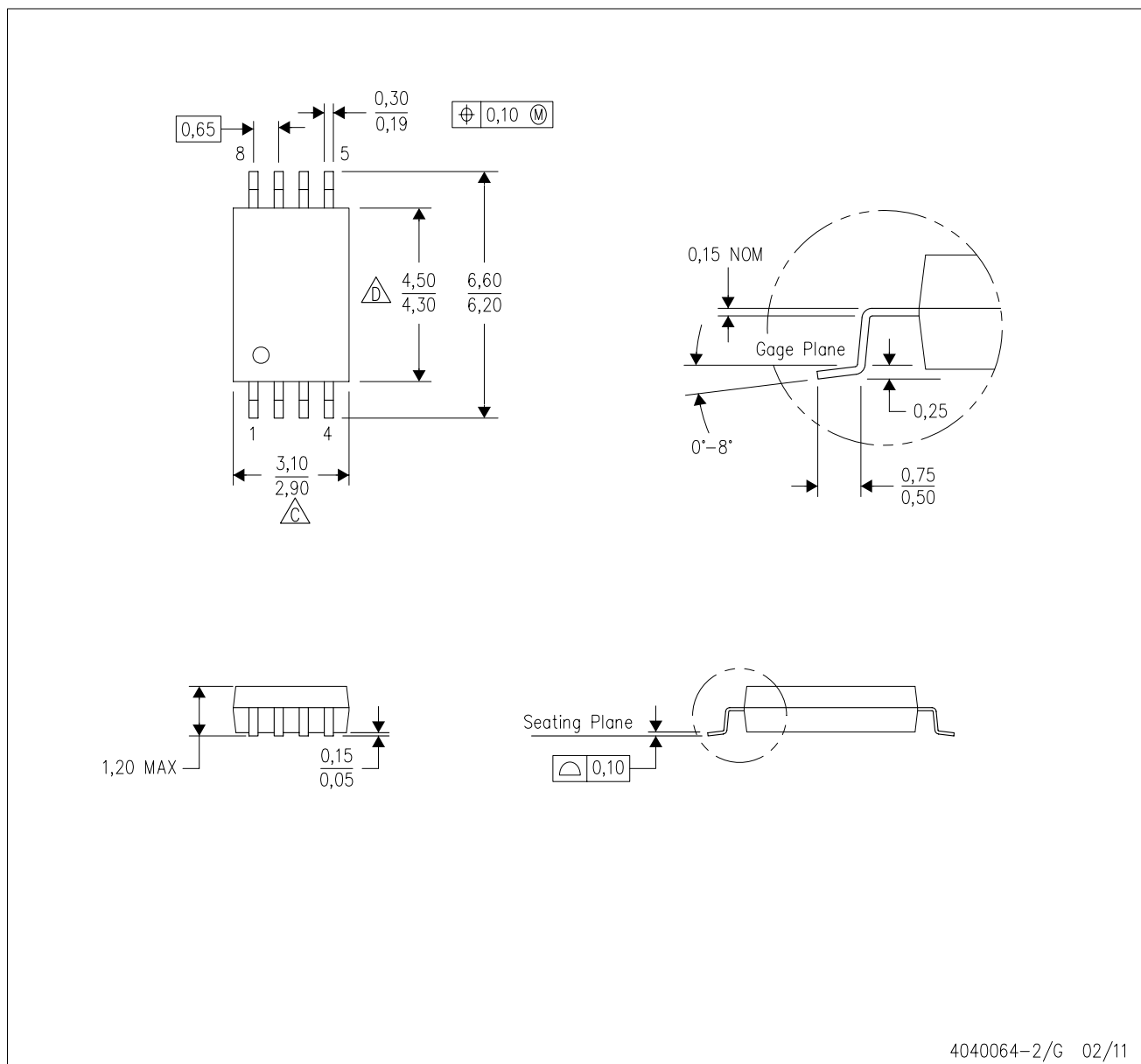
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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