

## TS5A3167 0.9-Ω 1-channel 1:1 SPST Analog Switch

### 1 Features

- Isolation in Powered-Off Mode,  $V_{CC} = 0$
- Low ON-State Resistance ( $0.9\ \Omega$ )
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals
- Microphone Switching – Notebook Docking

### 3 Description

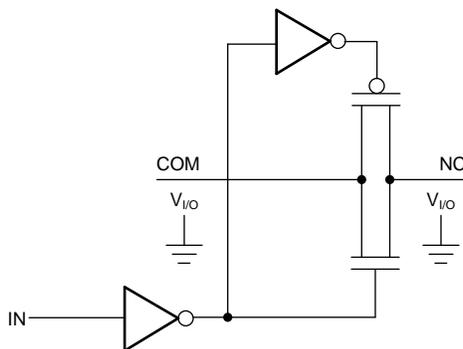
The TS5A3167 is a bidirectional, single-channel, single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The TS5A3167 device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3167	SOT-23	2.90 mm x 1.60 mm
	SC70	2.00 mm x 1.25 mm
	DSBGA	1.50 mm x 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simple Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

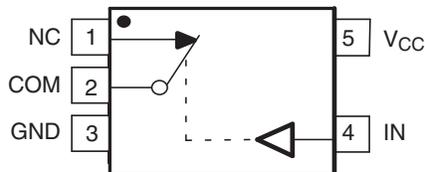
<b>Changes from Original (February 2005) to Revision A</b>	<b>Page</b>
• Updated <i>ORDERING INFORMATION</i> table .....	1

<b>Changes from Revision A (October 2012) to Revision B</b>	<b>Page</b>
• Added the <i>Device Information</i> table, <i>Pin Configuration and Functions</i> , <i>ESD Ratings</i> , <i>Recommended Operating Conditions</i> , <i>Thermal Information</i> , <i>Detailed Description</i> , <i>Feature Description</i> , <i>Device Functional Modes</i> , <i>Application and Implementation</i> , <i>Power Supply Recommendations</i> , <i>Layout</i> , <i>Device and Documentation Support</i> .....	1
• Removed <i>ORDERING INFORMATION</i> table .....	1

## 5 Pin Configuration and Functions

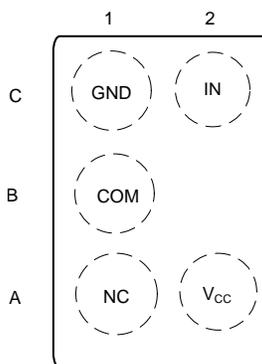
**DBV or DCK Package  
5- Pin (SOT-23 or SC70)  
Top View**



**Pin Functions**

PIN NUMBER	NAME	DESCRIPTION
1	NC	Normally Closed
2	COM	Common
3	GND	Ground
4	IN	Digital control pin, COM connected to NC when logic low
5	V <sub>CC</sub>	Power Supply

**YZP Package  
5-Pin (DSBGA)  
Top View**



**Pin Functions**

PIN NUMBER	NAME	DESCRIPTION
A1	NC	Normally Closed
B1	COM	Common
C1	GND	Ground
A2	V <sub>CC</sub>	Power Supply
C2	IN	Digital control pin, COM connected to NC when logic low

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(3)</sup>	-0.5	6.5	V
$V_{NC}$ $V_{COM}$	Analog voltage range <sup>(3)(4)(5)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_K$	Analog port diode current	$V_{NC}, V_{COM} < 0$		mA
$I_{NC}$ $I_{COM}$	On-state switch current On-state peak switch current <sup>(6)</sup>	$V_{NC}, V_{COM} = 0 \text{ to } V_{CC}$		mA
$V_I$	Digital input voltage range <sup>(3)(4)</sup>	-0.5	6.5	V
$I_{IK}$	Digital clamp current	$V_I < 0$		mA
$I_{CC}$	Continuous current through $V_{CC}$		100	mA
$I_{GND}$	Continuous current through GND	-100		mA
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		V
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	1.65	5.5	V
$V_{NC}$ $V_{COM}$	Analog voltage range	0	$V_{CC}$	V
$V_I$	Digital input voltage range	0	$V_{CC}$	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TS5A3167			UNIT	
	DBV (SOT-23)	DCK (SOT-23)	YZP (DSBGA)		
	5 PINS	5 PINS	5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	230.3	268.0	146.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	111.9	171.8	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.5	64.5	39.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	33.0	40.5	0.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	69.0	62.9	39.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics for 5-V Supply<sup>(1)</sup>

 $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Peak ON resistance	$r_{\text{peak}}$	$0 \leq V_{\text{NC}} \leq V_{\text{CC}}$ , $I_{\text{COM}} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V	0.8	1.1	$\Omega$	
				Full		1.2			
ON-state resistance	$r_{\text{on}}$	$V_{\text{NC}} = 2.5\text{ V}$ , $I_{\text{COM}} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V	0.75	0.9	$\Omega$	
				Full		1			
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq V_{\text{NC}} \leq V_{\text{CC}}$ , $I_{\text{COM}} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V	0.2		$\Omega$	
				25°C		0.15	0.25		
				Full		0.25			
NC OFF leakage current	$I_{\text{NC(OFF)}}$	$V_{\text{NC}} = 1\text{ V}$ , $V_{\text{COM}} = 4.5\text{ V}$ , or $V_{\text{NC}} = 4.5\text{ V}$ , $V_{\text{COM}} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	5.5 V	0	4	20	nA
				Full		-150	150		
	$I_{\text{NC(PWROFF)}}$	$V_{\text{NC}} = 0\text{ to }5.5\text{ V}$ , $V_{\text{COM}} = 5.5\text{ V to }0$ ,		25°C	0 V	-10	0.2	10	$\mu\text{A}$
				Full		-50	50		
COM OFF leakage current	$I_{\text{COM(OFF)}}$	$V_{\text{COM}} = 1\text{ V}$ , $V_{\text{NC}} = 4.5\text{ V}$ , or $V_{\text{COM}} = 4.5\text{ V}$ , $V_{\text{NC}} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	5.5 V	0	4	20	nA
				Full		-150	150		
	$I_{\text{COM(PWROFF)}}$	$V_{\text{COM}} = 5.5\text{ V to }0$ , $V_{\text{NC}} = 0\text{ to }5.5\text{ V}$ ,		25°C	0 V	-10	0.2	10	$\mu\text{A}$
				Full		-50	50		
NC ON leakage current	$I_{\text{NC(ON)}}$	$V_{\text{NC}} = 1\text{ V}$ , $V_{\text{COM}} = \text{Open}$ , or $V_{\text{NC}} = 4.5\text{ V}$ , $V_{\text{COM}} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	5.5 V	-5	0.4	5	nA
				Full		-50	50		
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{COM}} = 1\text{ V}$ , $V_{\text{NC}} = \text{Open}$ , or $V_{\text{COM}} = 4.5\text{ V}$ , $V_{\text{NC}} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	5.5 V	-5	0.4	5	nA
				Full		-20	20		
<b>Digital Control Inputs (IN)</b>									
Input logic high	$V_{\text{IH}}$			Full		2.4	5.5	V	
Input logic low	$V_{\text{IL}}$			Full		0	0.8	V	
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{I}} = 5.5\text{ V or }0$		25°C	5.5 V	-2	0.3	2	nA
				Full		-20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.6 Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	VCC	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_{CC}$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
Turn-off time	$t_{OFF}$	$V_{COM} = V_{CC}$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 20</a>	25°C	5 V		6	pC	
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	5 V		19	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	5 V		18	pF	
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	5 V		35.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	5 V		35.5	pF	
Digital input capacitance	$C_I$	$V_I = V_{CC}$ or GND,	See <a href="#">Figure 16</a>	25°C	5 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ ,	Switch ON, See <a href="#">Figure 18</a>	25°C	5 V		150	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 19</a>	25°C	5 V		-62	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 21</a>	25°C	5 V		0.005%		
<b>Supply</b>									
Positive supply current	$I_{CC}$	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	5.5 V	0.01	0.1	$\mu\text{A}$	
				Full			1		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.7 Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>

 $V_{CC} = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Peak ON resistance	$r_{peak}$	$0 \leq V_{NC} \leq V_{CC}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	3 V	1.3	1.6	$\Omega$	
				Full		1.8			
ON-state resistance	$r_{on}$	$V_{NC} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	3 V	1.1	1.5	$\Omega$	
				Full		1.7			
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NC} \leq V_{CC}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	3 V	0.3		$\Omega$	
				25°C		0.15	0.25		
		Full	0.25						
NC OFF leakage current	$I_{NC(OFF)}$	$V_{NC} = 1\text{ V}$ , $V_{COM} = 3\text{ V}$ , or $V_{NC} = 3\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V	-5	0.5	5	nA
				Full		-50	50		
	$I_{NC(PWROFF)}$	$V_{NC} = 0\text{ to }3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to }0$ ,		25°C	0 V	-5	0.1	5	$\mu\text{A}$
				Full		-25	25		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$ , $V_{NC} = 3\text{ V}$ , or $V_{COM} = 3\text{ V}$ , $V_{NC} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V	-5	0.5	5	nA
				Full		-50	50		
	$I_{COM(PWROFF)}$	$V_{COM} = 3.6\text{ V to }0$ , $V_{NC} = 0\text{ to }3.6\text{ V}$ ,		25°C	0 V	-5	0.1	5	$\mu\text{A}$
				Full		-25	25		
NC ON leakage current	$I_{NC(ON)}$	$V_{NC} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} = 3\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	3.6 V	-2	0.3	2	nA
				Full		-20	20		
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NC} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NC} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	3.6 V	-2	0.3	2	nA
				Full		-20	20		
<b>Digital Control Inputs (IN)</b>									
Input logic high	$V_{IH}$			Full		2	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.8	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$		25°C	3.6 V	-2	0.3	2	nA
				Full		-20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.8 Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (continued)

$V_{CC} = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	VCC	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_{CC}$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1.0		10	
Turn-off time	$t_{OFF}$	$V_{COM} = V_{CC}$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 20</a>	25°C	3.3 V		6	pC	
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	3.3 V		19.5	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	3.3 V		18.5	pF	
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	3.3 V		36	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	3.3 V		36	pF	
Digital input capacitance	$C_I$	$V_I = V_{CC}$ or GND,	See <a href="#">Figure 16</a>	25°C	3.3 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ ,	Switch ON, See <a href="#">Figure 18</a>	25°C	3.3 V		150	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 19</a>	25°C	3.3 V		-62	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 21</a>	25°C	3.3 V		0.01%		
<b>Supply</b>									
Positive supply current	$I_{CC}$	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	3.6 V	0.001	0.05	$\mu\text{A}$	
				Full			0.3		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.9 Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>

 $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Peak ON resistance	$r_{peak}$	$0 \leq V_{NC} \leq V_{CC}$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V	1.8	2.4	$\Omega$	
				Full		2.6			
ON-state resistance	$r_{on}$	$V_{NC} = 2 \text{ V}$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V	1.2	2.1	$\Omega$	
				Full		2.4			
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NC} \leq V_{CC}$ , $I_{COM} = -100 \text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	2.3 V	0.7		$\Omega$	
				25°C		0.4	0.6		
		Full	0.6						
NC OFF leakage current	$I_{NC(OFF)}$	$V_{NC} = 1 \text{ V}$ , $V_{COM} = 3 \text{ V}$ , or $V_{NC} = 3 \text{ V}$ , $V_{COM} = 1 \text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	2.7 V	-5	0.3	5	nA
				Full		-50	50		
	$I_{NC(PWROFF)}$	$V_{NC} = 0 \text{ to } 3.6 \text{ V}$ , $V_{COM} = 3.6 \text{ V to } 0$ ,		25°C	0 V	-2	0.05	2	$\mu\text{A}$
				Full		-15	15		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1 \text{ V}$ , $V_{NC} = 3 \text{ V}$ , or $V_{COM} = 3 \text{ V}$ , $V_{NC} = 1 \text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	2.7 V	-5	0.3	5	nA
				Full		-50	50		
	$I_{COM(PWROFF)}$	$V_{COM} = 3.6 \text{ V to } 0$ , $V_{NC} = 0 \text{ to } 3.6 \text{ V}$ ,		25°C	0 V	-2	0.05	2	$\mu\text{A}$
				Full		-15	15		
NC ON leakage current	$I_{NC(ON)}$	$V_{NC} = 1 \text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} = 3 \text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	2.7 V	-2	0.3	2	nA
				Full		-20	20		
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1 \text{ V}$ , $V_{NC} = \text{Open}$ , or $V_{COM} = 3 \text{ V}$ , $V_{NC} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	2.7 V	-2	0.3	2	nA
				Full		-20	20		
<b>Digital Control Inputs (IN)</b>									
Input logic high	$V_{IH}$			Full		1.8	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.6	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$		25°C	2.7 V	-2	0.3	2	nA
				Full		-20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.10 Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (continued)

$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	VCC	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_{CC}$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
Turn-off time	$t_{OFF}$	$V_{COM} = V_{CC}$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1 \text{ nF}$ , See <a href="#">Figure 20</a>	25°C	2.5 V		4	pC	
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	2.5 V		19.5	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	2.5 V		18.5	pF	
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.5 V		36.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	2.5 V		36.5	pF	
Digital input capacitance	$C_I$	$V_I = V_{CC}$ or GND,	See <a href="#">Figure 16</a>	25°C	2.5 V		2	pF	
Bandwidth	BW	$R_L = 50 \Omega$ ,	Switch ON, See <a href="#">Figure 18</a>	25°C	2.5 V		150	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 19</a>	25°C	2.5 V		-62	dB	
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , See <a href="#">Figure 21</a>	25°C	2.5 V		0.02%		
<b>Supply</b>									
Positive supply current	$I_{CC}$	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	2.7 V	0.001	0.02	$\mu\text{A}$	
				Full			0.25		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.11 Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>

 $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Peak ON resistance	$r_{peak}$	$0 \leq V_{NC} \leq V_{CC}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V	4.2	25	$\Omega$	
				Full		30			
ON-state resistance	$r_{on}$	$V_{NC} = 2\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V	1.6	3.9	$\Omega$	
				Full		4.0			
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NC} \leq V_{CC}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V	2.8		$\Omega$	
				25°C		4.1	22		
		Full	27						
NC OFF leakage current	$I_{NC(OFF)}$	$V_{NC} = 1\text{ V}$ , $V_{COM} = 3\text{ V}$ , or $V_{NC} = 3\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	1.95 V	-5	5	nA	
				Full		-50	50		
	$I_{NC(PWROFF)}$	$V_{NC} = 0\text{ to }3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to }0$ ,		25°C	0 V	-2	2	$\mu\text{A}$	
				Full		-10	10		
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1\text{ V}$ , $V_{NC} = 3\text{ V}$ , or $V_{COM} = 3\text{ V}$ , $V_{NC} = 1\text{ V}$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	1.95 V	-5	5	nA	
				Full		-50	50		
	$I_{COM(PWROFF)}$	$V_{COM} = 0\text{ to }3.6\text{ V}$ , $V_{NC} = 3.6\text{ V to }0$ ,		25°C	0 V	-2	2	$\mu\text{A}$	
				Full		-10	10		
NC ON leakage current	$I_{NC(ON)}$	$V_{NC} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} = 3\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	1.95 V	-2	2	nA	
				Full		-20	20		
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1\text{ V}$ , $V_{NC} = \text{Open}$ , or $V_{COM} = 3\text{ V}$ , $V_{NC} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	1.95 V	-2	2	nA	
				Full		-20	20		
<b>Digital Control Inputs (IN)</b>									
Input logic high	$V_{IH}$			Full		1.5	5.5	V	
Input logic low	$V_{IL}$			Full		0	0.6	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$		25°C	1.95 V	-2	0.3	2	nA
				Full		-20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 6.12 Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (continued)

$V_{CC} = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_{CC}$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
Turn-off time	$t_{OFF}$	$V_{COM} = V_{CC}$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 20</a>	25°C	1.8 V		2	pC	
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	1.8 V		19.5	pF	
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See <a href="#">Figure 16</a>	25°C	1.8 V		18.5	pF	
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	1.8 V		36.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND,	Switch ON, See <a href="#">Figure 16</a>	25°C	1.8 V		36.5	pF	
Digital input capacitance	$C_I$	$V_I = V_{CC}$ or GND,	See <a href="#">Figure 16</a>	25°C	1.8 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ ,	Switch ON, See <a href="#">Figure 18</a>	25°C	1.8 V		150	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 19</a>	25°C	1.8 V		-62	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ See <a href="#">Figure 21</a>	25°C	1.8 V		0.055%		
<b>Supply</b>									
Positive supply current	$I_{CC}$	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	1.95 V	0.001	0.01	$\mu\text{A}$	
				Full			0.15		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

### 6.13 Typical Performance

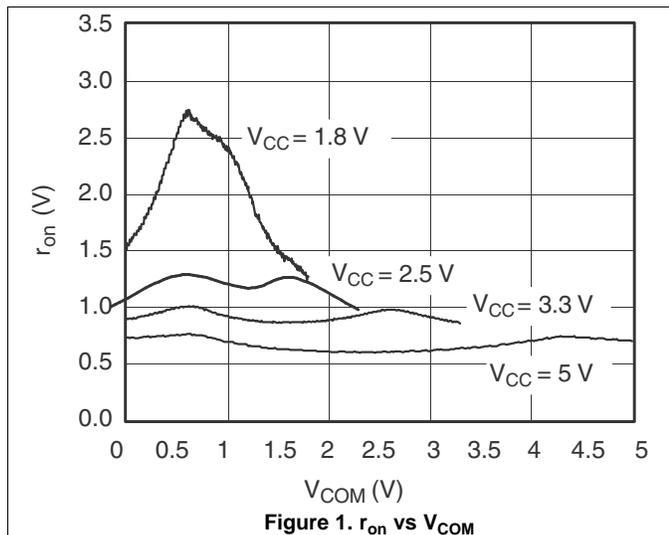


Figure 1.  $r_{on}$  vs  $V_{COM}$

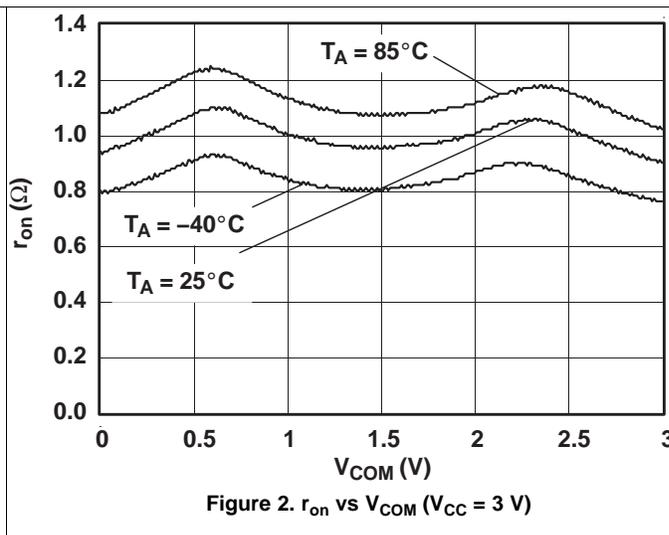


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_{CC} = 3$  V)

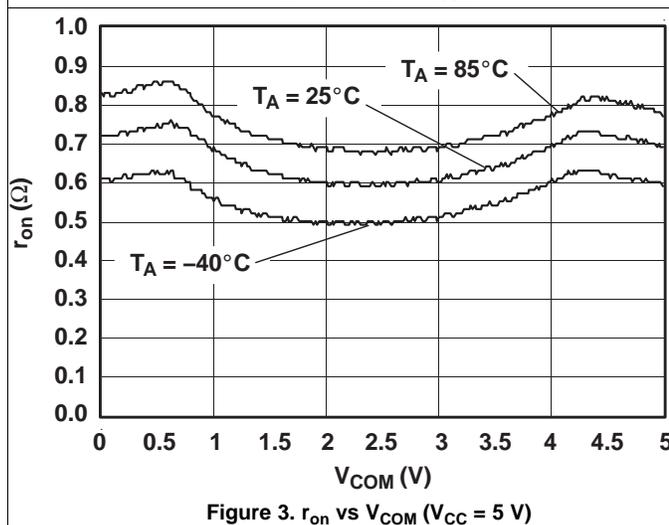


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_{CC} = 5$  V)

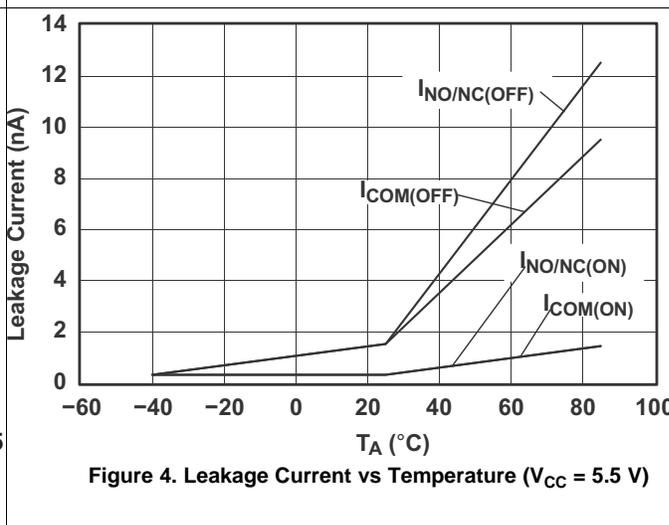


Figure 4. Leakage Current vs Temperature ( $V_{CC} = 5.5$  V)

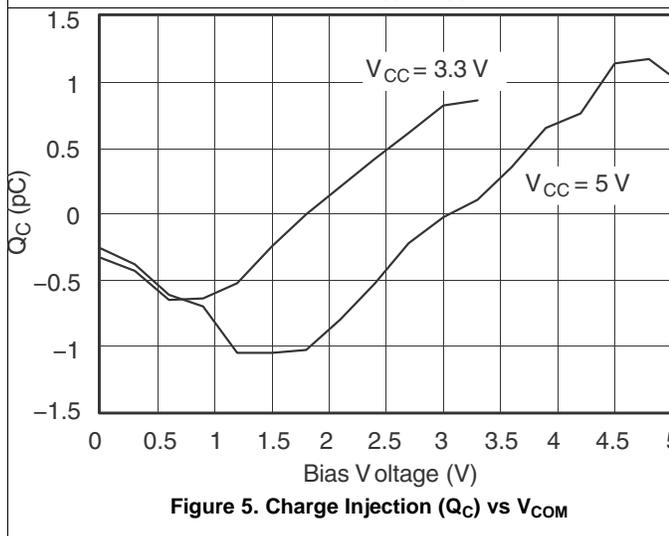


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

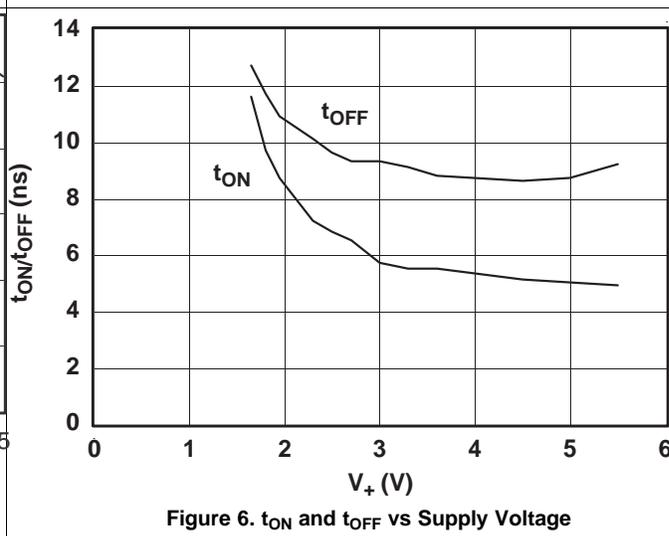


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

Typical Performance (continued)

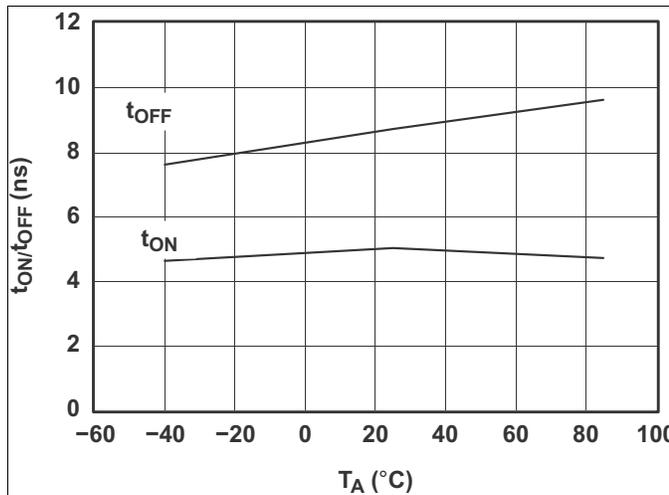


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_{CC} = 5\text{ V}$ )

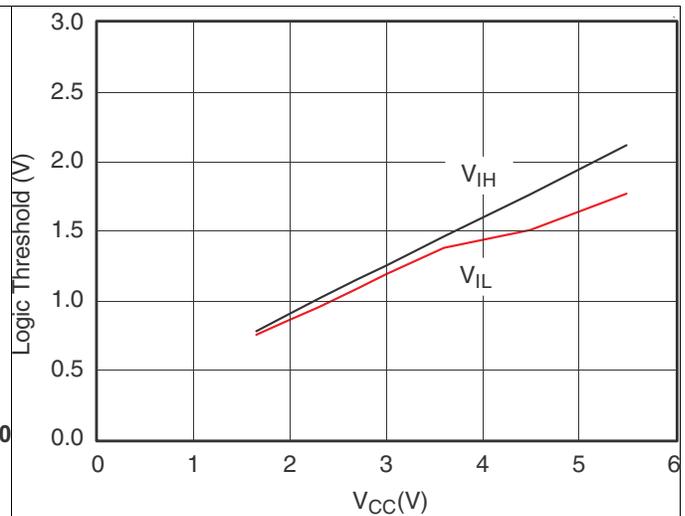


Figure 8. Logic Threshold vs  $V_{CC}$

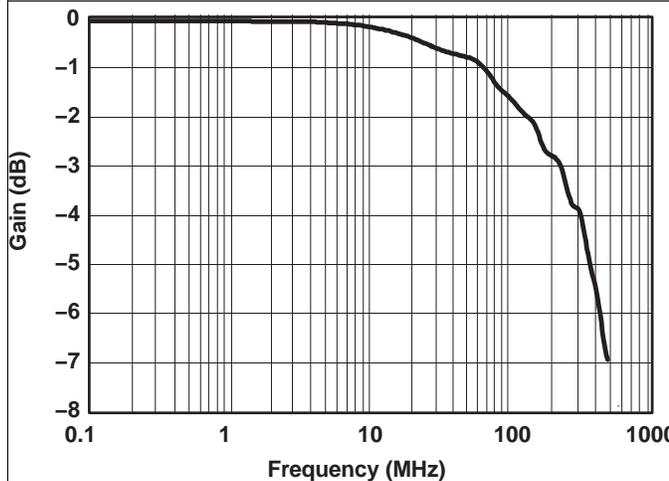


Figure 9. Gain vs Frequency ( $V_{CC} = 5\text{ V}$ )

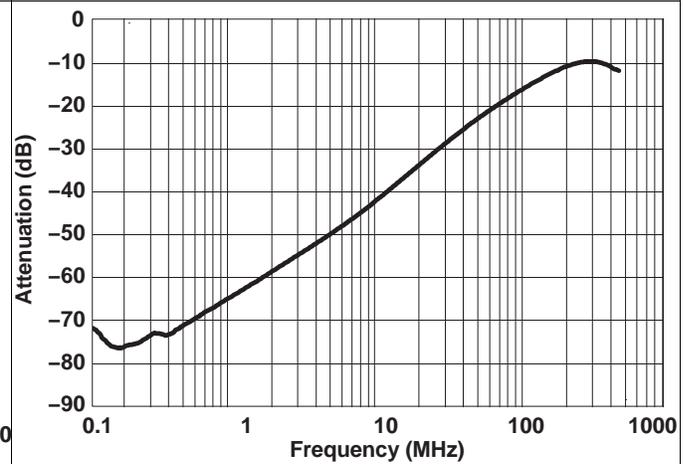


Figure 10. OFF Isolation vs Frequency ( $V_{CC} = 5\text{ V}$ )

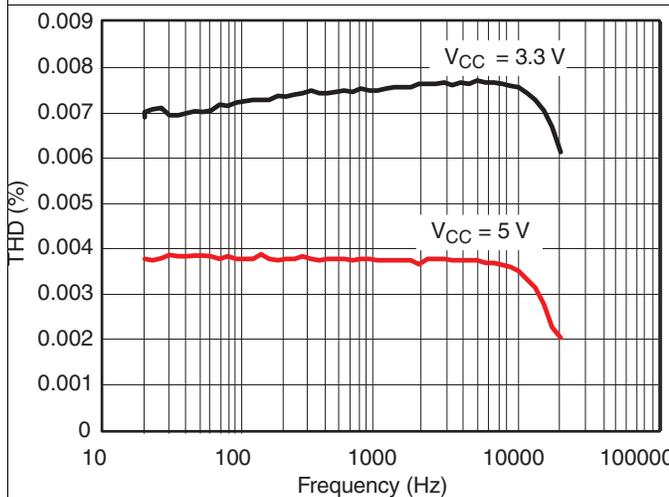


Figure 11. Total Harmonic Distortion vs Frequency ( $V_{CC} = 5\text{ V}$ )

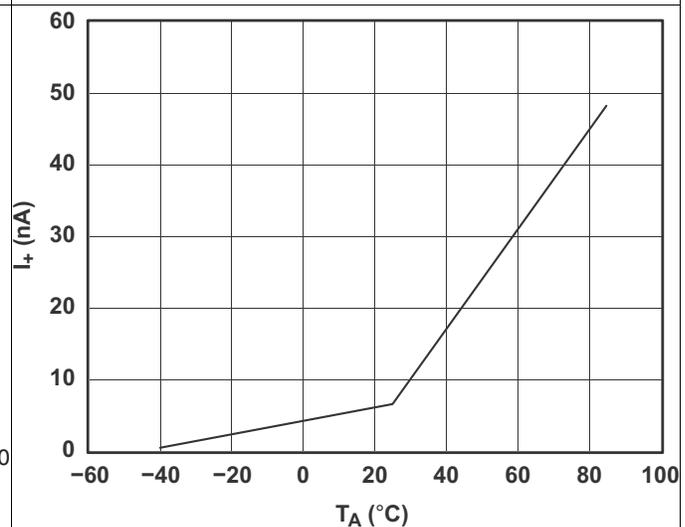


Figure 12. Power-Supply Current vs Temperature ( $V_{CC} = 5\text{ V}$ )

## 7 Parameter Measurement Information

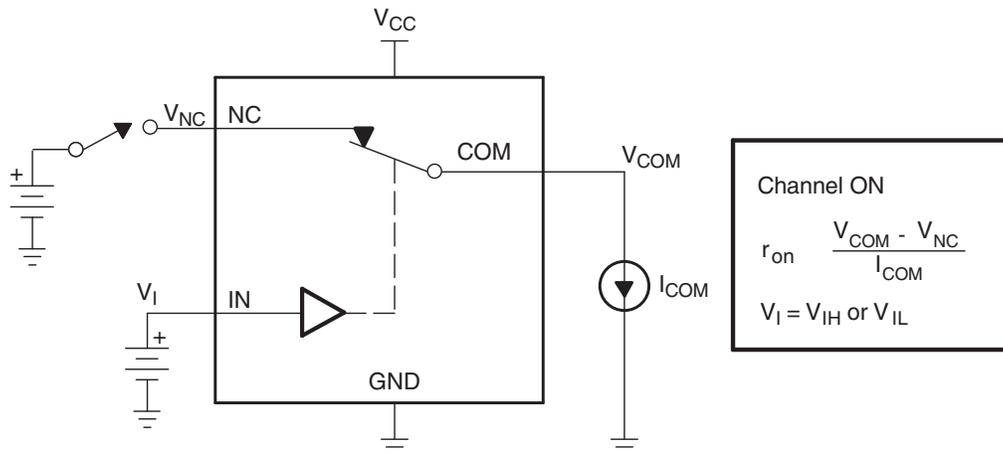


Figure 13. ON-State Resistance ( $r_{on}$ )

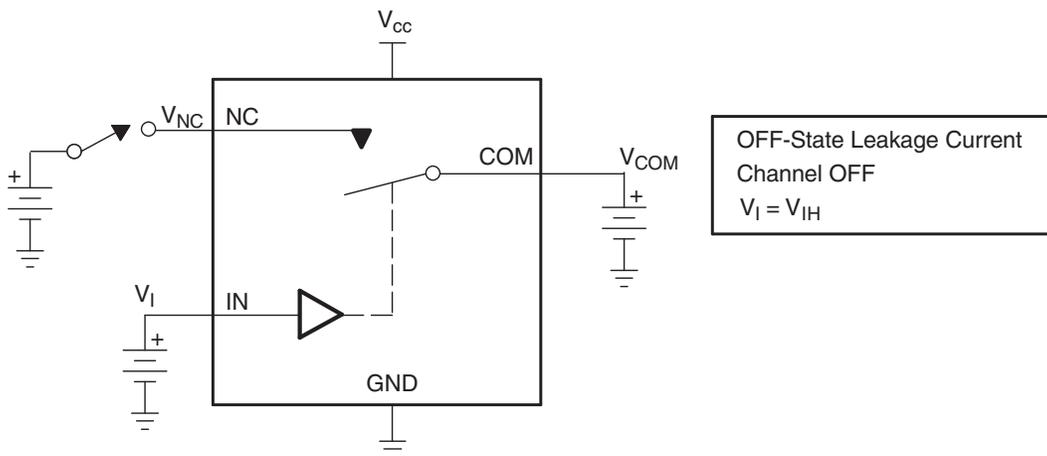


Figure 14. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NC(OFF)}$ ,  $I_{COM(PWROFF)}$ ,  $I_{NC(PWROFF)}$ )

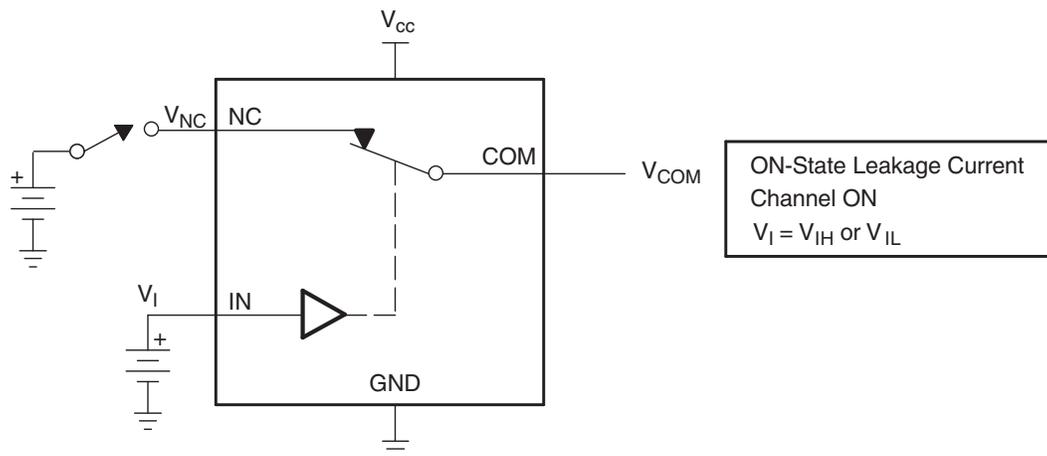
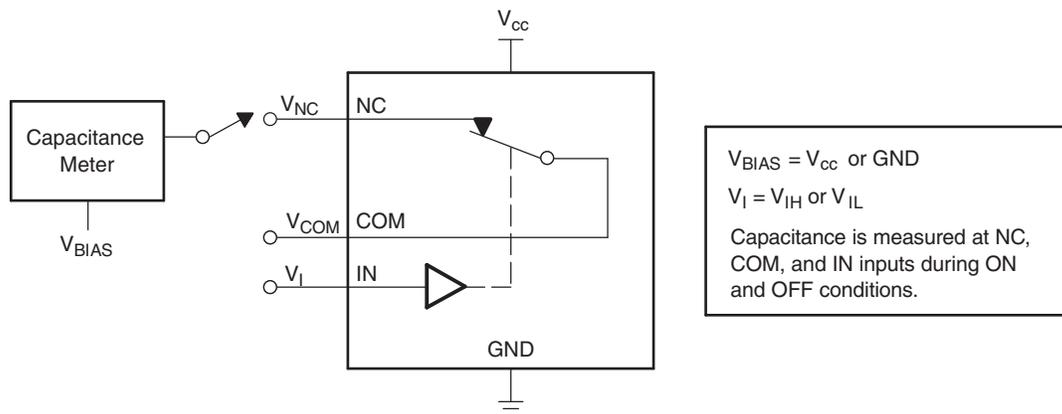
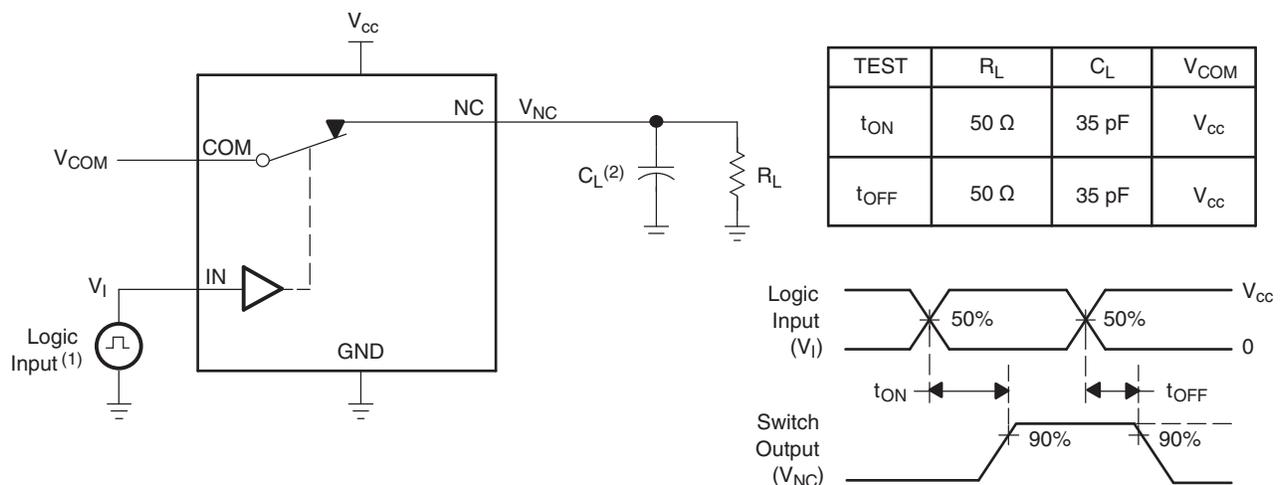


Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ )

**Parameter Measurement Information (continued)**

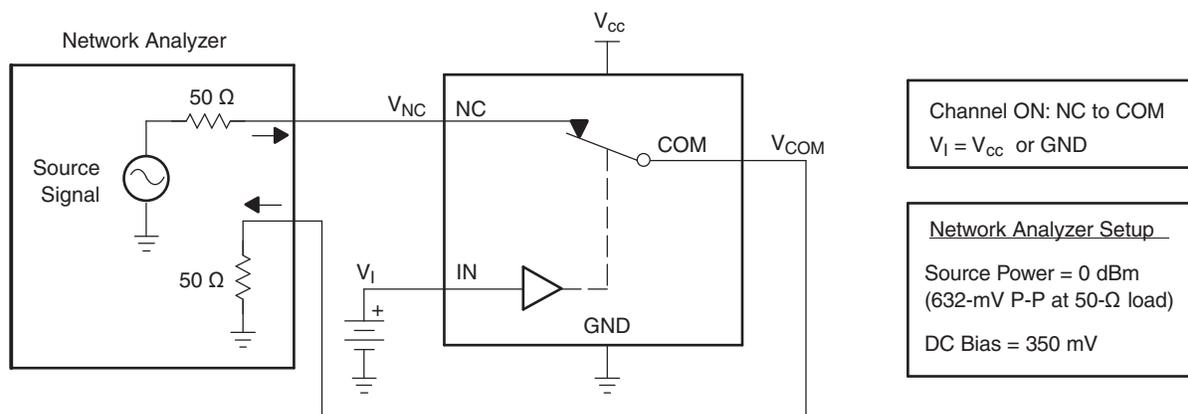


**Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NC(ON)}$ )**



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- (2)  $C_L$  includes probe and jig capacitance.

**Figure 17. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )**



**Figure 18. Bandwidth (BW)**

Parameter Measurement Information (continued)

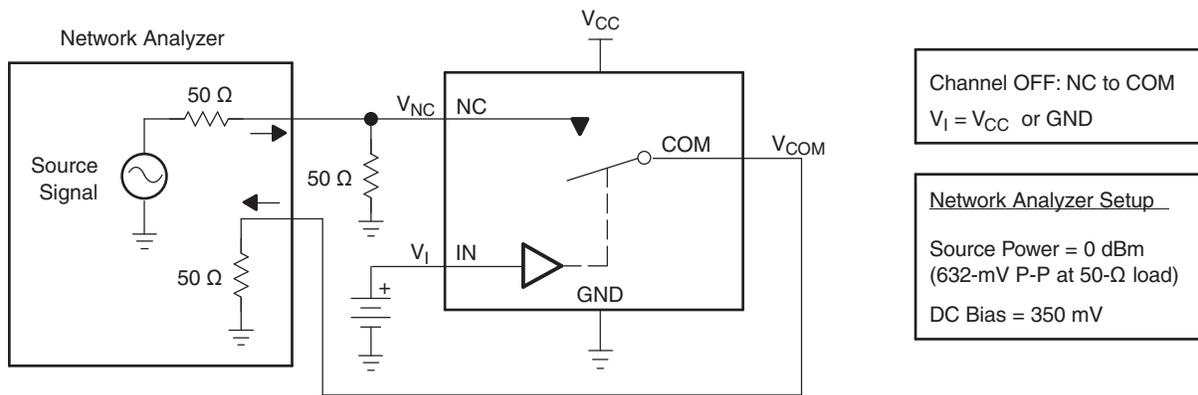
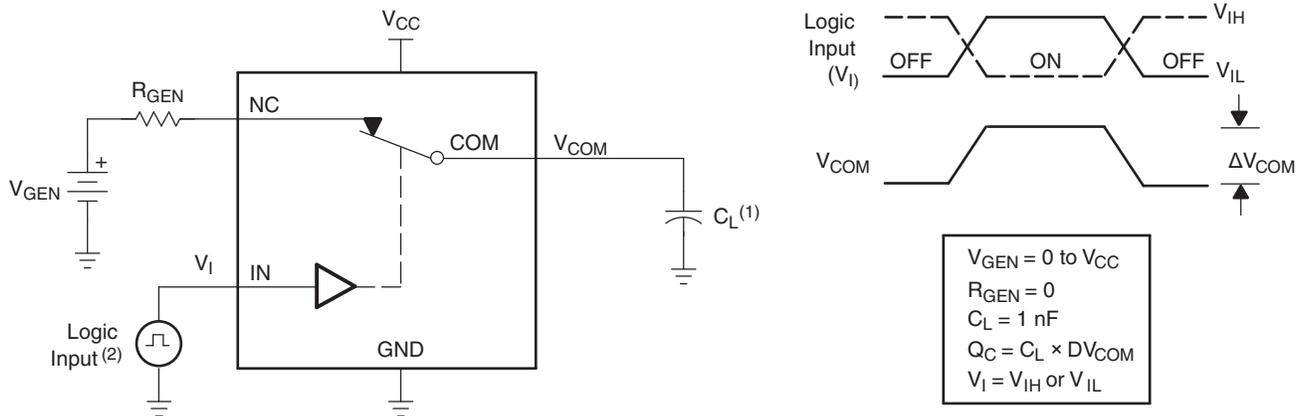
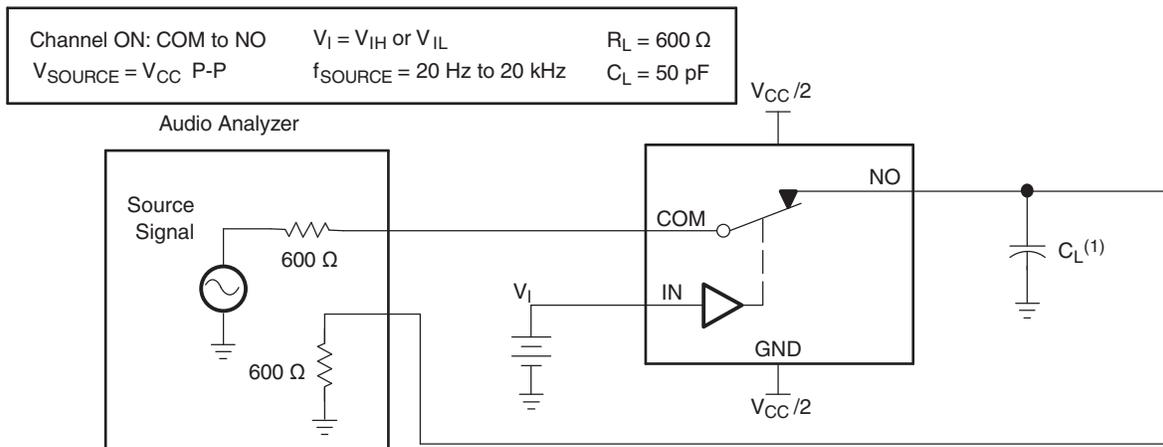


Figure 19. OFF Isolation ( $O_{Iso}$ )



- (1)  $C_L$  includes probe and jig capacitance.
- (2) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.

Figure 20. Charge Injection ( $Q_C$ )



- (1)  $C_L$  includes probe and jig capacitance.

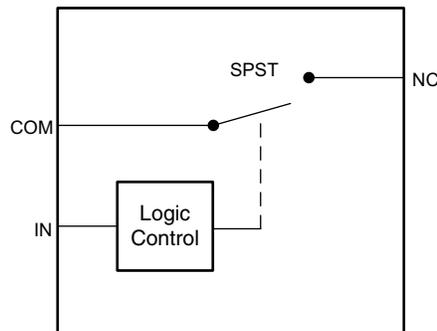
Figure 21. Total Harmonic Distortion (THD)

## 8 Detailed Description

### 8.1 Overview

The TS5A3167 is a bidirectional, single-channel, single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3167 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. The device consumes very low power and provides isolation when  $V_{CC} = 0$ .

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Isolation in Powered-Off Mode, $V_{CC} = 0$

When power is not supplied to the  $V_{CC}$  pin,  $V_{CC} = 0$ , the signal paths NC and COM are high impedance. This is specified in the electrical characteristics table under the COM and NC OFF leakage current when  $V_{CC} = 0$ . Because the device is high impedance when it is not powered, you may connect other signals to the signal chain without interference of the TS5A3167.

### 8.4 Device Functional Modes

Placing a logic low signal on the IN pin of the device will turn on the switch and provide a low impedance path from NC to COM.

**Table 1. Function Table**

IN	NC TO COM, COM TO NC
L	ON
H	OFF

## 9 Application and Implementation

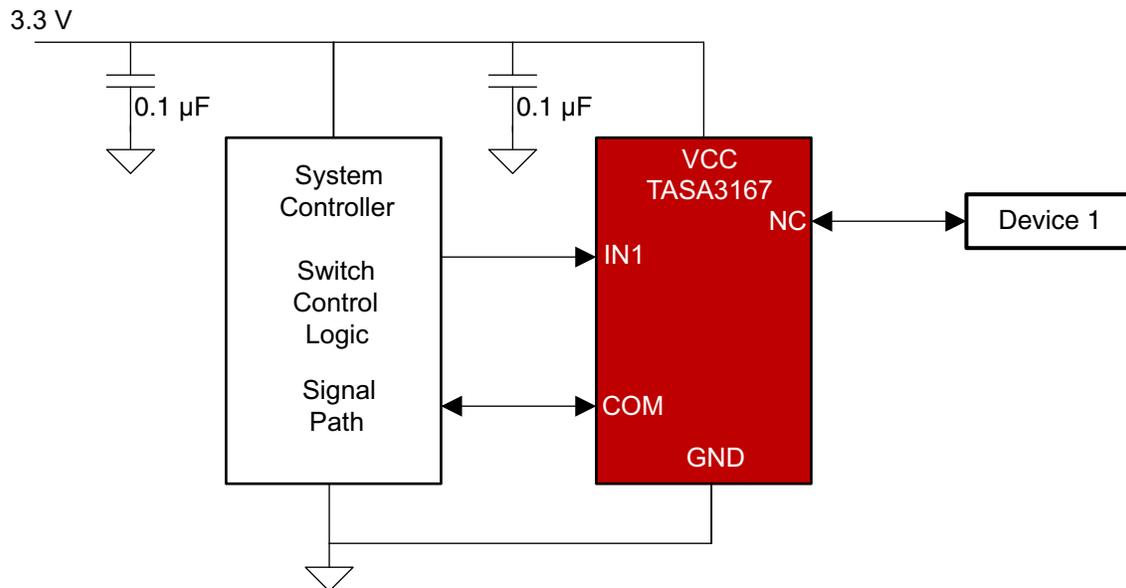
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TS5A3167 switch is bidirectional, so the NC and COM pins can be used as either inputs or outputs. This switch is typically used when there is one signal path that needs to be isolated at certain times.

### 9.2 Typical Application



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Figure 22. Typical Application

#### 9.2.1 Design Requirements

The TS5A3167 device can be properly operated without any external components.

Unused pin may be left floating or connected to ground.

TI recommends pulling up the digital control pin (IN) to  $V_{CC}$  or pulling down to GND to avoid undesired switch positions that could result from the floating pin. A floating digital pin could cause excess current consumption refer to [Implications of Slow or Floating CMOS Inputs](#).

#### 9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3167 input and output signal swing through NC and COM are dependent on the supply voltage  $V_{CC}$ . For example, if the desired signal level to pass through the switch is 5 V,  $V_{CC}$  must be greater than or equal to 5 V.  $V_{CC} = 3.3$  V would not be valid for passing a 5-V signal since the analog signal voltage cannot exceed the supply.

## Typical Application (continued)

### 9.2.3 Application Curves

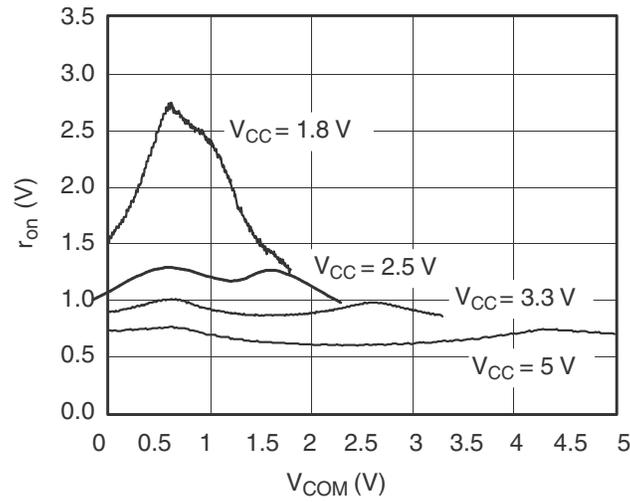


Figure 23.  $r_{on}$  vs  $V_{COM}$

## 10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. It is recommended that  $V_{CC}$  is powered on first, followed by NC or COM but not required because of the Isolation in Powered-Off Mode,  $V_{CC} = 0$  feature.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the  $V_{CC}$  supply to other components. A 0.1- $\mu$ F capacitor, connected from  $V_{CC}$  to GND, is adequate for most applications.

## 11 Layout

### 11.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

### 11.2 Layout Example

 = VIA to GND Plane

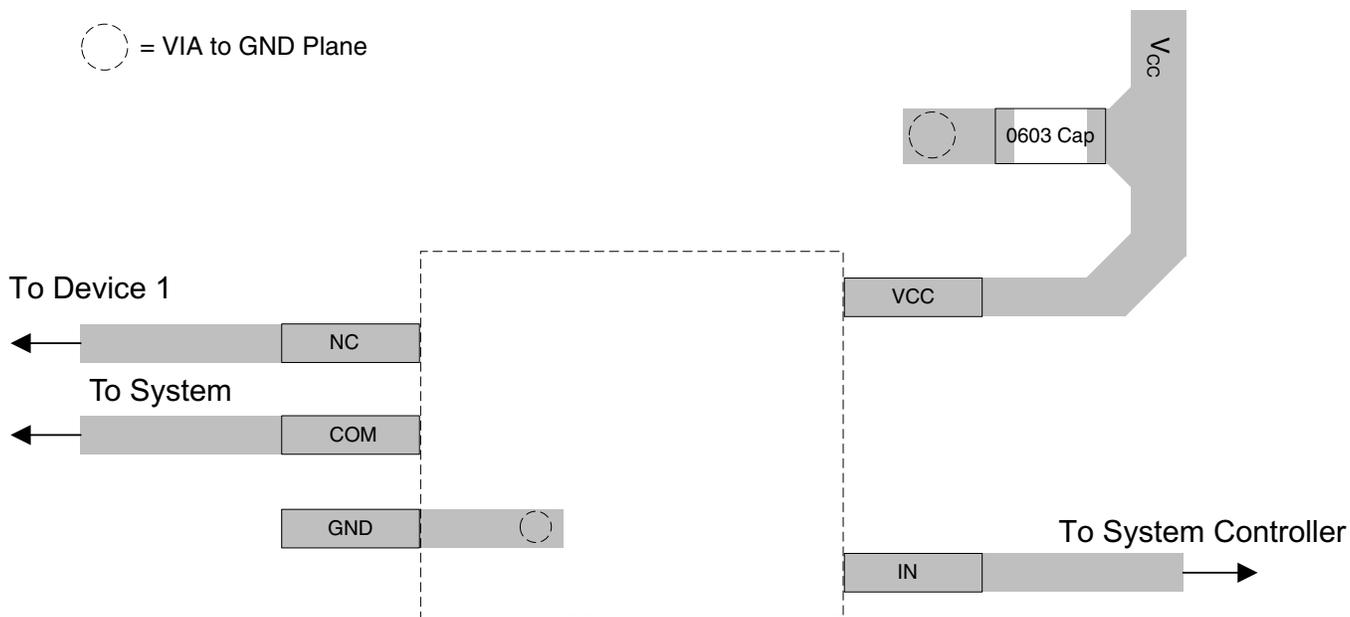


Figure 24. Example Layout

## 12 Device and Documentation Support

### 12.1 Documentation Support

**Table 2. Parameter Description**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM.
$V_{NC}$	Voltage at NC.
$r_{on}$	Resistance between COM and NC ports when the channel is ON.
$r_{peak}$	Peak on-state resistance over a specified voltage range.
$r_{on(Flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions.
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions.
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_{CC} = 0$ .
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the OFF state under worst-case input and output conditions.
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_{CC} = 0$ .
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open.
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the ON state and the output (NC) open.
$V_{IH}$	Minimum input voltage for logic high for the control input (IN).
$V_{IL}$	Maximum input voltage for logic low for the control input (IN).
$V_I$	Voltage at the control input (IN).
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN).
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning OFF.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or COM) output. This is measured in coulombs (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ , $C_L$ is the load capacitance, and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF.
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF.
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON.
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON.
$C_I$	Capacitance of control input (IN).
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
$I_{CC}$	Static power-supply current with the control (IN) pin at $V_{CC}$ or GND.

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## Community Resources (continued)

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.

## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3167DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU   CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JATF ~ JATR) (JATH ~ JATP)	<a href="#">Samples</a>
TS5A3167DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JATF	<a href="#">Samples</a>
TS5A3167DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JATF	<a href="#">Samples</a>
TS5A3167DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5 ~ JGF ~ JGR) (JGH ~ JGP ~ JGS)	<a href="#">Samples</a>
TS5A3167DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5 ~ JGF ~ JGR) (JGH ~ JGP ~ JGS)	<a href="#">Samples</a>
TS5A3167YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(JG7 ~ JGN)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

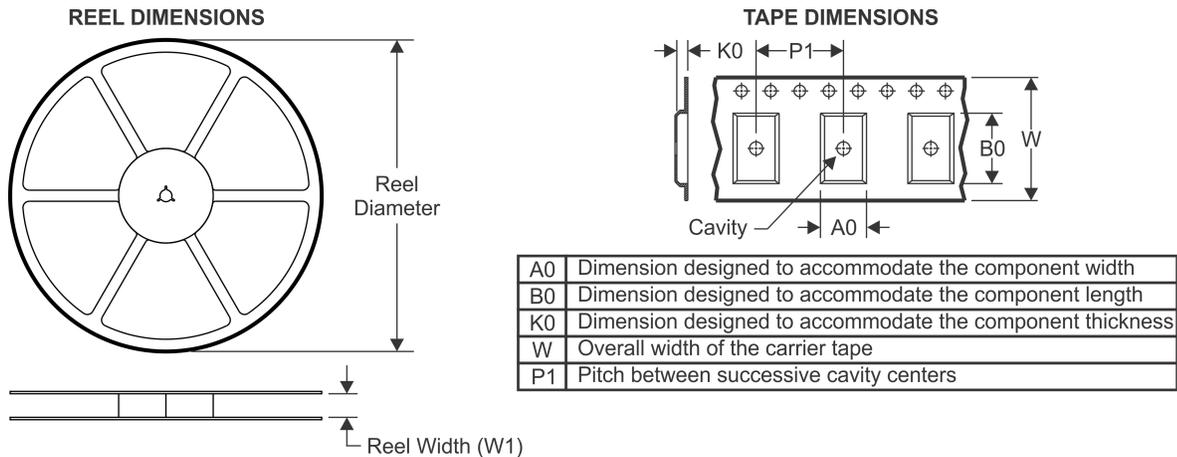
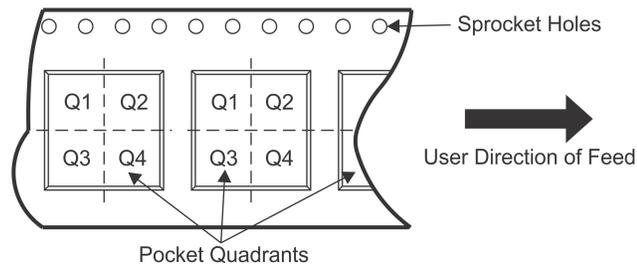
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

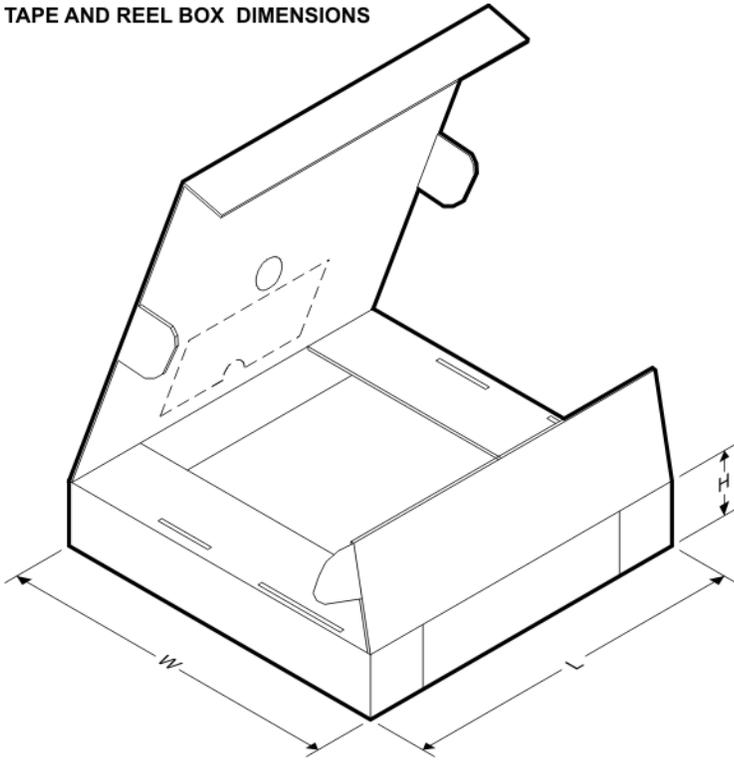
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3167DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3167DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3167DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3167DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
TS5A3167YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

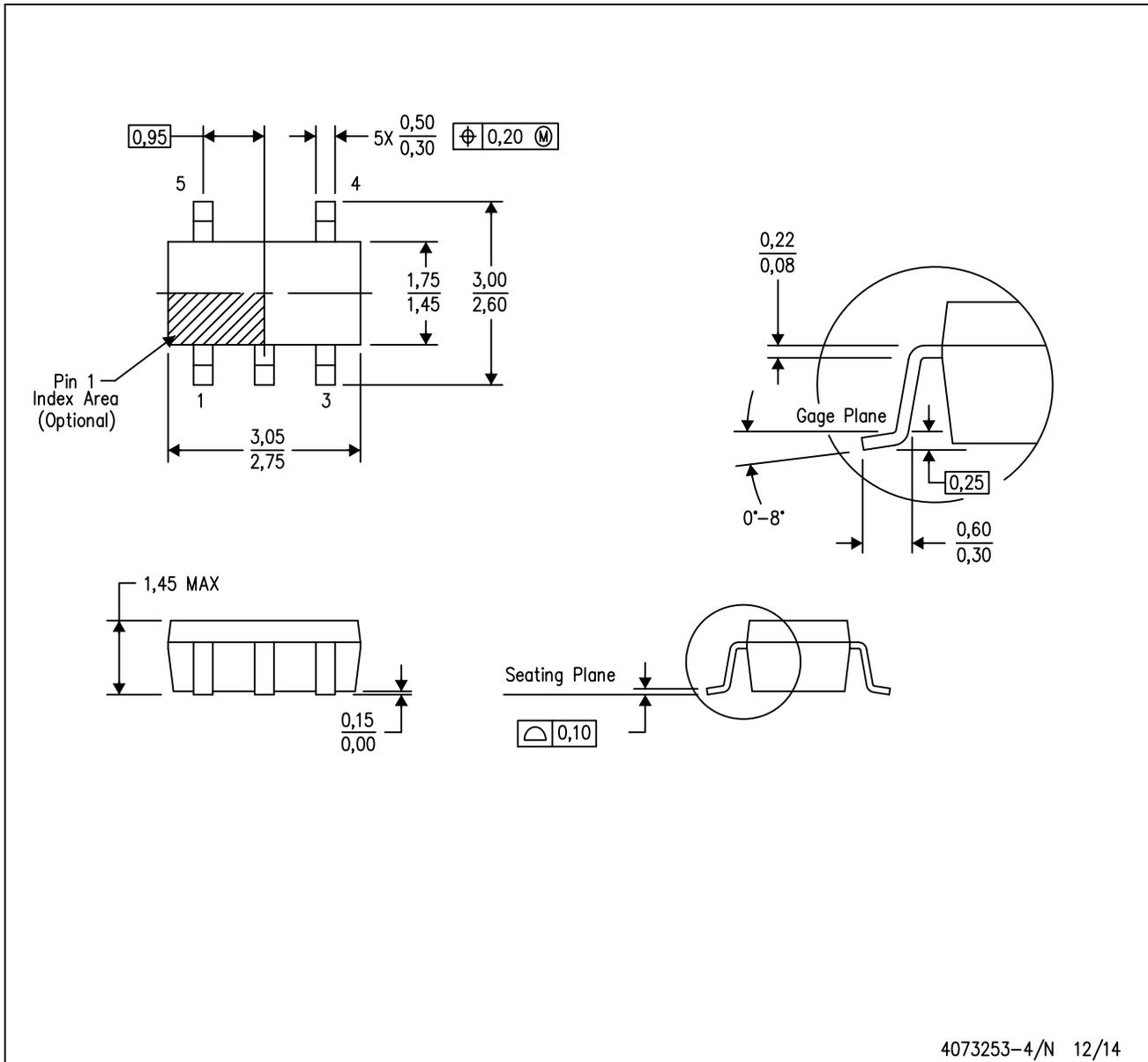
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3167DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A3167DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3167DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3167DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A3167YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DBV (R-PDSO-G5)

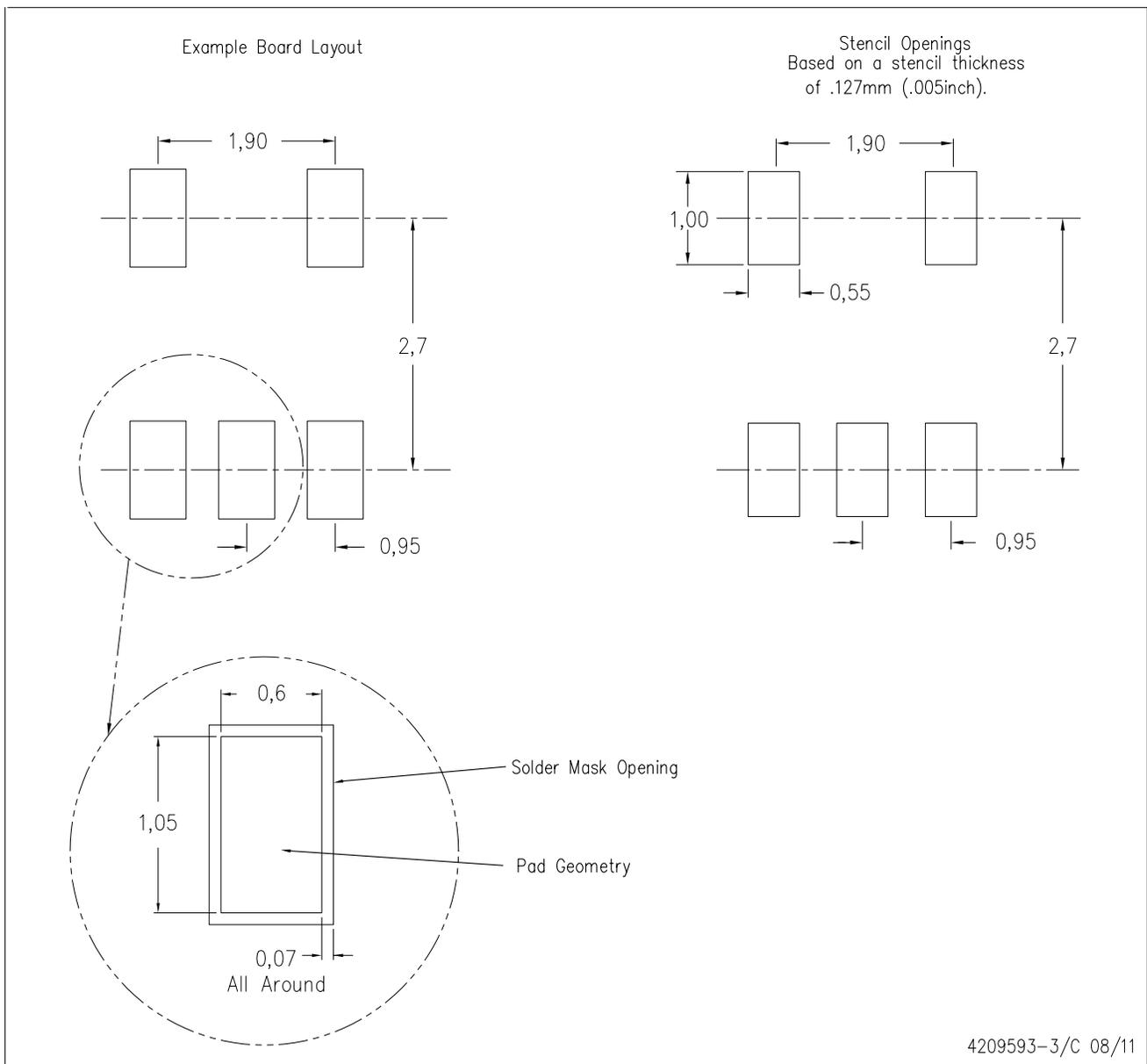
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

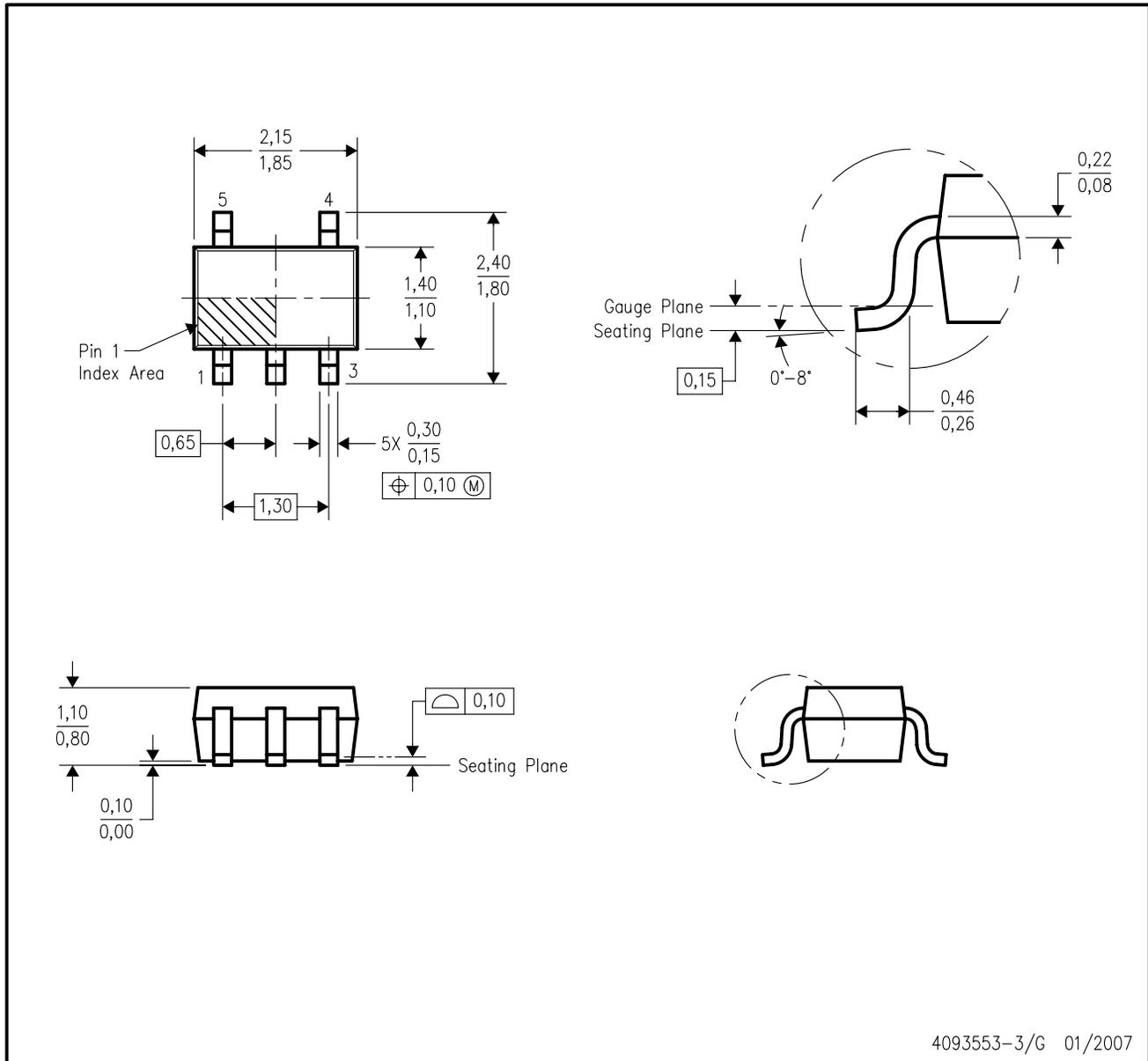
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

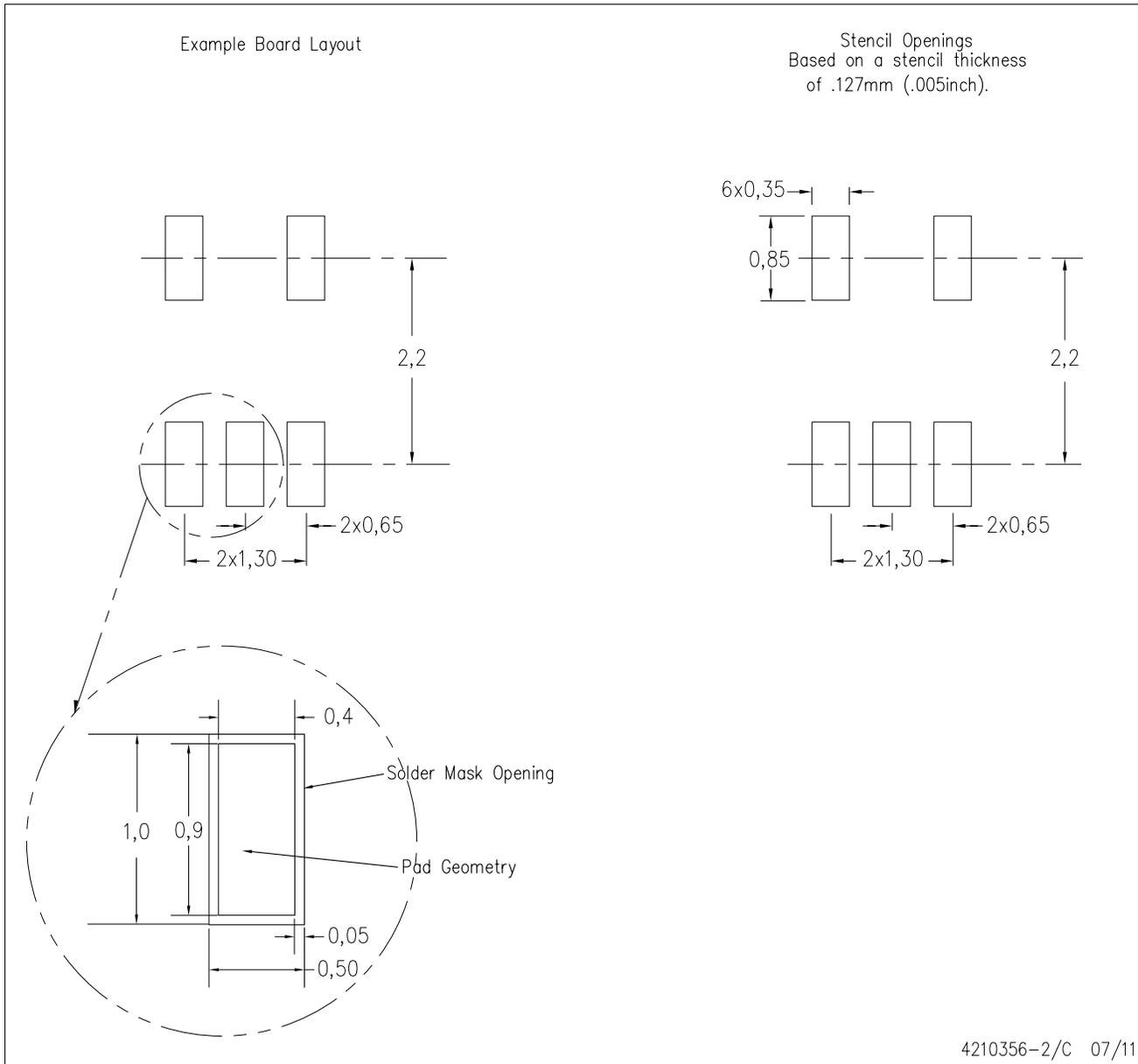
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

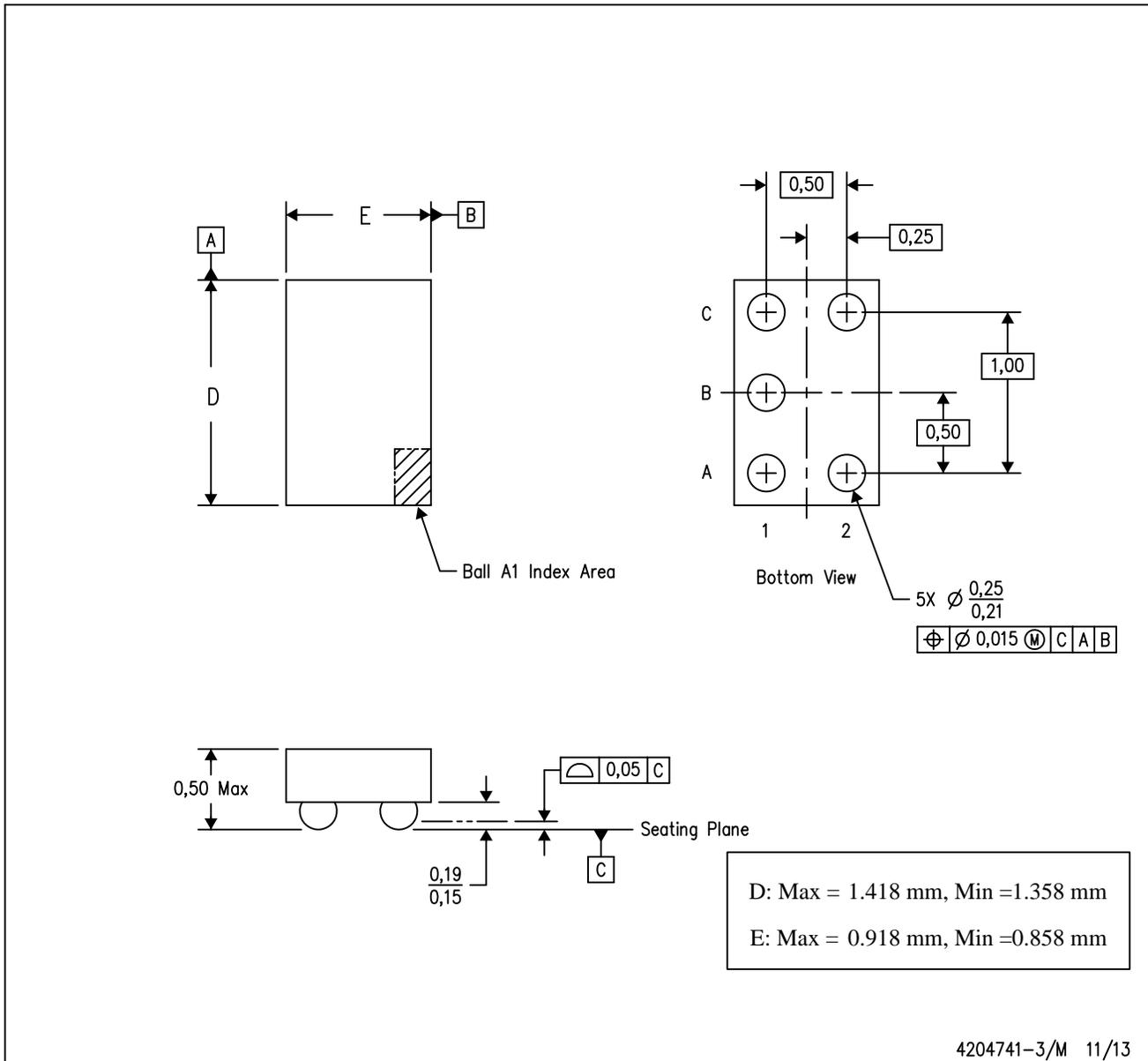
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

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