



CD4067

16-channel Analog Multiplexer/Demultiplexer

Product Specification

Specification Revision History:

Version	Date	Description
2019-09-A1	2019-09	New
2023-04-B1	2023-04	Update the template
2023-07-B2	2023-07	Additional package
2024-04-B3	2024-04	Modify the parameters
2024-09-B4	2024-09	Add the SSOP24 (0.635mm) package form



Contents

1、 General Description.....	3
2、 Block Diagram And Pin Description	5
2.1、 Block Diagram	5
2.2、 Pin Configurations.....	6
2.3、 Pin Description	6
2.4、 Function Table.....	7
3、 Electrical Parameter	8
3.1、 Absolute Maximum Ratings.....	8
3.2、 Recommended Operating Conditions.....	8
3.3、 Electrical Characteristics	8
3.3.1、 DC Characteristics 1	8
3.3.2、 DC Characteristics 2	9
3.3.3、 AC Characteristics 1	9
3.3.4、 AC Characteristics 2	10
4、 Testing Circuit	10
4.1、 AC Testing Circuit 1	10
4.2、 AC Testing Waveforms.....	11
4.3、 AC Testing Circuit 2	12
4.4、 Measurement Points	13
4.5、 Test Data	13
5、 Package Information	14
5.1、 SOP24	14
5.2、 TSSOP24.....	15
5.3、 SSOP24 (0.65mm)	16
5.4、 SSOP24 (0.635mm)	17
6、 Statements And Notes	18
6.1、 The name and content of Hazardous substances or Elements in the product	18
6.2、 Notes	18



1、General Description

The CD4067 is a 16-channel analog multiplexer/demultiplexer with four address inputs (A0 to A3), an active LOW enable input (\bar{E}), sixteen independent inputs/outputs (Y0 to Y15) and a common input/output (Z). The device contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y15) and the other side connected to the common input/output (Z). With \bar{E} LOW, one of the sixteen switches is selected (low-impedance ON-state) by A0 to A3. All unselected switches are in the high-impedance OFF-state. With \bar{E} HIGH all switches are in the high-impedance OFF-state, independent of A0 to A3. The analog inputs/outputs (Y0 to Y15 and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 9V.

Features:

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information:SOP24/TSSOP24/SSOP24(0.65mm)/SSOP24(0.635mm)



Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4067SA24.TB	SOP24	CD4067	30 PCS/tube	80 tube/box	2400 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing: 1.27mm
CD4067TA24.TB	TSSOP24	CD4067	62 PCS/tube	200 tube/box	12400 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm
CD4067VA24.TB	SSOP24	CD4067	60 PCS/tube	100 tube/box	6000 PCS/box	Dimensions of plastic enclosure: 8.2mm×5.3mm Pin spacing: 0.65mm
CD4067VB24.TB	SSOP24	CD4067	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 0.635mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4067SA24.TR	SOP24	CD4067	1250 PCS/reel	1250 PCS/box	Dimensions of plastic enclosure: 15.4mm×7.5mm Pin spacing:1.27mm
CD4067TA24.TR	TSSOP24	CD4067	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm
CD4067VA24.TR	SSOP24	CD4067	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 8.2mm×5.3mm Pin spacing: 0.65mm
CD4067VB24.TR	SSOP24	CD4067	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 0.635mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

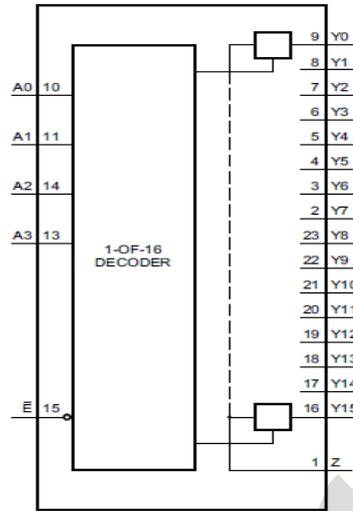


Figure 1. Functional diagram

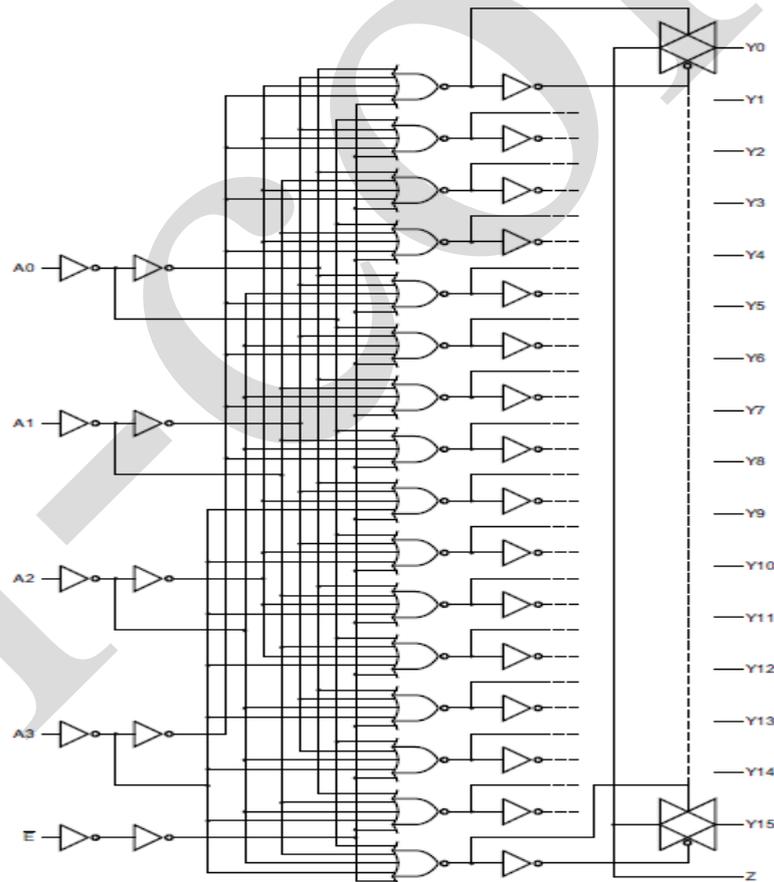


Figure 2. Logic diagram

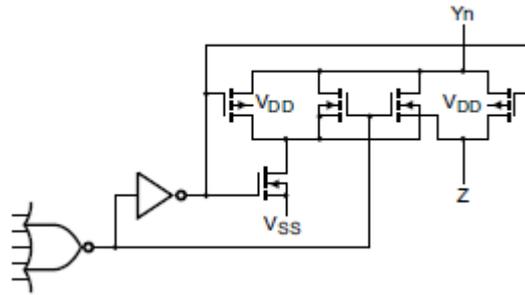
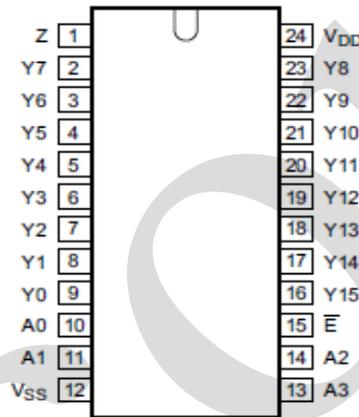


Figure 3. Schematic diagram (one switch)

2.2、 Pin Configurations



2.3、 Pin Description

Pin No.	Pin Name	Description
1	Z	common input/output
2	Y7	independent input/output
3	Y6	independent input/output
4	Y5	independent input/output
5	Y4	independent input/output
6	Y3	independent input/output
7	Y2	independent input/output
8	Y1	independent input/output
9	Y0	independent input/output
10	A0	address input
11	A1	address input
12	V _{SS}	ground (0V)
13	A3	address input
14	A2	address input
15	\bar{E}	enable input (active LOW)
16	Y15	independent input/output



17	Y14	independent input/output
18	Y13	independent input/output
19	Y12	independent input/output
20	Y11	independent input/output
21	Y10	independent input/output
22	Y9	independent input/output
23	Y8	independent input/output
24	V _{DD}	supply voltage

2.4、Function Table

\bar{E}	Input				Channel ON
	A3	A2	A1	A0	
L	L	L	L	L	Y0=Z
L	L	L	L	H	Y1=Z
L	L	L	H	L	Y2=Z
L	L	L	H	H	Y3=Z
L	L	H	L	L	Y4=Z
L	L	H	L	H	Y5=Z
L	L	H	H	L	Y6=Z
L	L	H	H	H	Y7=Z
L	H	L	L	L	Y8=Z
L	H	L	L	H	Y9=Z
L	H	L	H	L	Y10=Z
L	H	L	H	H	Y11=Z
L	H	H	L	L	Y12=Z
L	H	H	L	H	Y13=Z
L	H	H	H	L	Y14=Z
L	H	H	H	H	Y15=Z
H	X	X	X	X	none

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.



3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{DD}	-	-0.5	+12	V
input clamping current	I_{IK}	$V_I < 0.5V$ or $V_I > V_{DD} + 0.5V$	-	± 20	mA
switch current	I	-	-	± 25	mA
input voltage	V_I	all inputs	-0.5	$V_{DD} + 0.5$	V
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
soldering temperature	T_L	10s	260		°C

3.2、Recommended Operating Conditions

($T_{amb} = 25^\circ C$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	5	9	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C
input voltage	V_I	-	0	-	V_{DD}	V
multiplexer switch input current capability	-	-	-	-	25	mA
output load resistance	-	-	100	-	-	Ω

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb} = 25^\circ C$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)	$T_{amb} = 25^\circ C$			Unit	
			Min.	Typ.	Max.		
LOW-level input voltage	V_{IL}	$ I_O < 1\mu A$	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	-	-	1.5	V
			$V_{DD} = 9V$, $V_O = 1.0V$ or $9V$	-	-	3	V
HIGH-level input voltage	V_{IH}	$ I_O < 1\mu A$	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5	-	-	V
			$V_{DD} = 9V$, $V_O = 1.0V$ or $9V$	7	-	-	V
input leakage current	I_I	$V_I = 0V$ or $9V$, $V_{DD} = 9V$	-	-	± 1	μA	
OFF-state leakage current	$I_{S(OFF)}$	$V_{SS} = 0V$; $V_{DD} = 9V$	-	-	± 100	nA	
supply current	I_{DD}	all valid input combinations; $I_O = 0A$	$V_{DD} = 5V$	-	-	5	μA
			$V_{DD} = 9V$	-	-	10	μA
input capacitance	C_I	any address or inhibit input	-	5	7.5	pF	



ON resistance	R _{ON}	V _{SS} ≤ V _{is} ≤ V _{DD}	V _{DD} =5V	-	470	1050	Ω
			V _{DD} =9V	-	180	400	Ω
change in on-state resistance between channels	ΔR _{ON}	-	V _{DD} =5V	-	15	-	Ω
			V _{DD} =9V	-	10	-	Ω

3.3.2、DC Characteristics 2

(T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)	T _{amb} =-40°C		T _{amb} =+85°C		T _{amb} =+125°C		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
LOW-level input voltage	V _{IL}	I _O < 1μA	V _{DD} =5V, V _O =0.5V or 4.5V	-	1.5	-	1.5	-	1.5	V
			V _{DD} =9V, V _O =1.0V or 9V	-	3	-	3	-	3	V
HIGH-level input voltage	V _{IH}	I _O < 1μA	V _{DD} =5V, V _O =0.5V or 4.5V	3.5	-	3.5	-	3.5	-	V
			V _{DD} =9V, V _O =1.0V or 9V	7	-	7	-	7	-	V
input leakage current	I _I	V _I =0V or 9V, V _{DD} =9V	-	±1	-	±1	-	±1	μA	
OFF-state leakage current	I _{S(OFF)}	V _{SS} =0V; V _{DD} =9V	-	±100	-	±1000	-	±1000	nA	
supply current	I _{DD}	all valid input combinations; I _O =0A	V _{DD} =5V	-	5	-	150	-	150	μA
			V _{DD} =9V	-	10	-	300	-	300	μA
ON resistance	R _{ON}	V _{SS} ≤ V _{is} ≤ V _{DD}	V _{DD} =5V	-	850	-	1200	-	1300	Ω
			V _{DD} =9V	-	330	-	520	-	550	Ω

3.3.3、AC Characteristics 1

(T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH to LOW propagation delay time	t _{PHL}	Y _n , Z to Z, Y _n ; see Figure 5	V _{DD} =5V	-	30	60	ns
			V _{DD} =9V	-	15	30	ns
LOW to HIGH propagation delay	t _{PLH}	Y _n , Z to Z, Y _n ; see Figure 5	V _{DD} =5V	-	30	60	ns
			V _{DD} =9V	-	15	30	ns
HIGH to LOW propagation delay time	t _{PHL}	A _n to Z, Y _n ; see Figure 6	V _{DD} =5V	-	190	380	ns
			V _{DD} =9V	-	70	140	ns
LOW to HIGH propagation delay	t _{PLH}	A _n to Z, Y _n ; see Figure 6	V _{DD} =5V	-	175	350	ns
			V _{DD} =9V	-	70	140	ns
HIGH to OFF-state propagation delay	t _{PHZ}	E̅ to Y _n , Z; see Figure 7	V _{DD} =5V	-	325	650	ns
			V _{DD} =9V	-	135	270	ns
LOW to OFF-state propagation delay	t _{PLZ}	E̅ to Y _n , Z; see Figure 7	V _{DD} =5V	-	325	650	ns
			V _{DD} =9V	-	135	270	ns
OFF-state to HIGH propagation delay	t _{PZH}	E̅ to Y _n , Z; see Figure 7	V _{DD} =5V	-	220	440	ns
			V _{DD} =9V	-	90	180	ns
OFF-state to LOW propagation delay	t _{PZL}	E̅ to Y _n , Z; see Figure 7	V _{DD} =5V	-	220	440	ns
			V _{DD} =9V	-	90	180	ns



3.3.4、AC Characteristics 2

($T_{amb}=25^{\circ}C$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
-3dB frequency response	$f_{(-3dB)}$	$V_{is}=5V; V_{DD}=9V;$ $R_L=1k\Omega;$ see Figure 9	V_{os} at Z	-	14	-	MHz
			V_{os} at any channel	-	60	-	MHz
total harmonic distortion	THD	$f_{is}=1kHz$ sine wave; see Figure 8	$V_{is}=2V; V_{DD}=5V;$ $R_L=10k\Omega$	-	0.3	-	%
			$V_{is}=3V; V_{DD}=9V;$ $R_L=10k\Omega$	-	0.2	-	%
-40dB feed through frequency	$f_{(-40dB)}$	$V_{is}=5V; V_{DD}=9V;$ $R_L=1k\Omega;$ all channel off	V_{os} at Z	-	20	-	MHz
			V_{os} at any channel	-	8	-	MHz
crosstalk	X_{talk}	$V_{is}=5V; V_{DD}=9V; R_L=1k\Omega;$ frequency at -40dB; between any 2 channels; see Figure 11	-	1	-	MHz	
crosstalk voltage	V_{ct}	$V_{DD}=9V; R_L=10k\Omega; V_C=V_{DD}-V_{SS}$ (square wave); see Figure 10	-	75	-	mV	

Note:

[1] $20\log(V_{os}/V_{is}) = -3dB$.

[2] $20\log(V_{os}/V_{is}) = -40dB$.

[3] Peak-to-peak voltage symmetrical about $(V_{DD}-V_{SS})/2$.

4、Testing Circuit

4.1、AC Testing Circuit 1

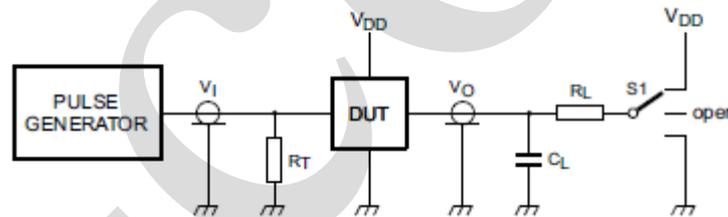


Figure 4. Test circuit for switching times

Definitions for test circuit:

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

$S1$ =Test selection switch.



4.2、AC Testing Waveforms

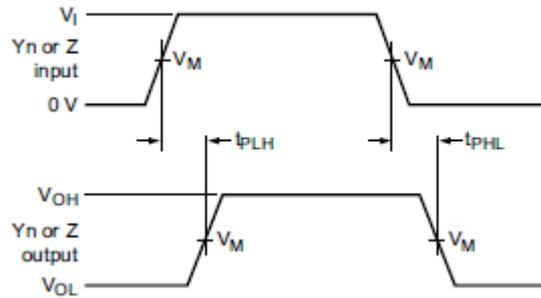


Figure 5. Yn, Z to Z, Yn propagation delays

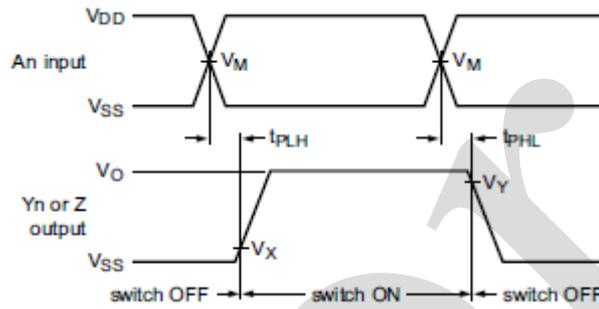


Figure 6. An to Yn, Z propagation delays

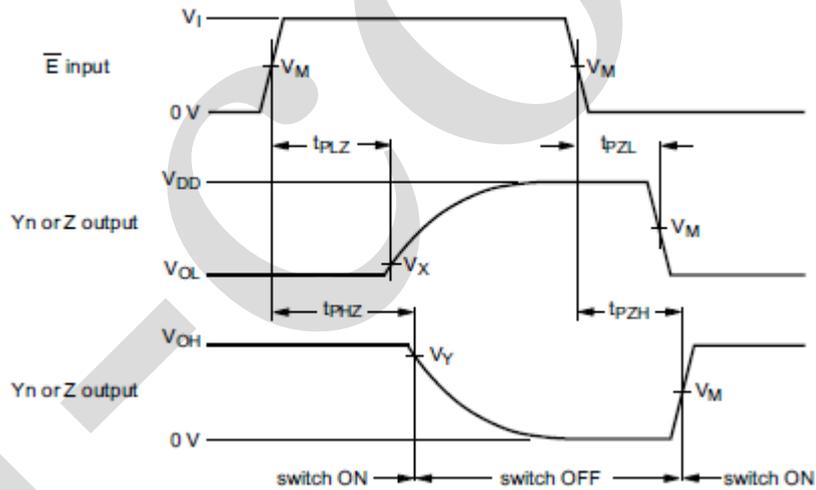


Figure 7. Enable and disable times



4.3、AC Testing Circuit 2

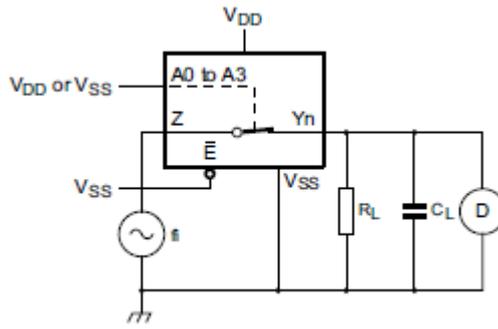


Figure 8. Test circuit for measuring total harmonic distortion

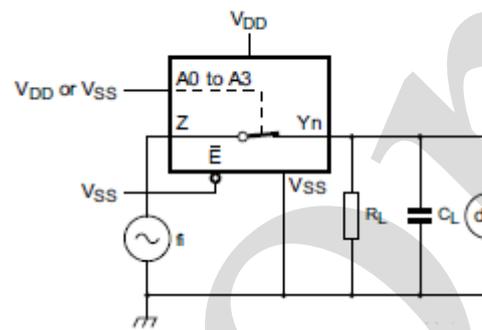
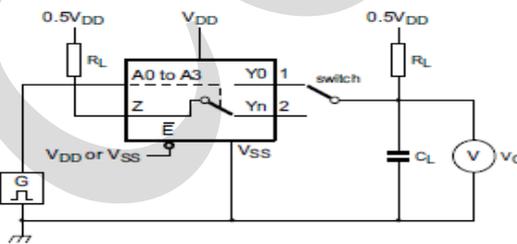
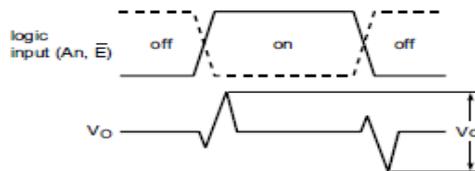


Figure 9. Test circuit for measuring frequency response



a. Test circuit



b. Input and output pulse definitions

Figure 10. Test circuit for measuring crosstalk voltage between digital inputs and switch

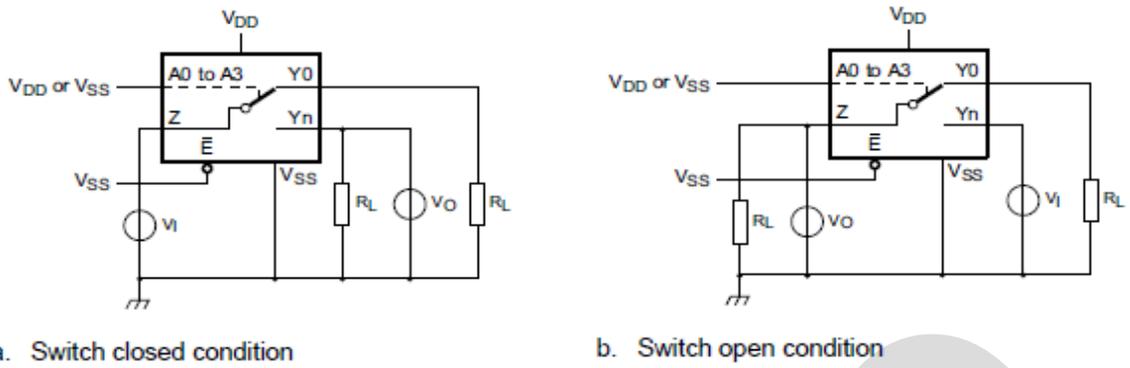


Figure 11. Test circuit for measuring crosstalk between switches

4.4、 Measurement Points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 9V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

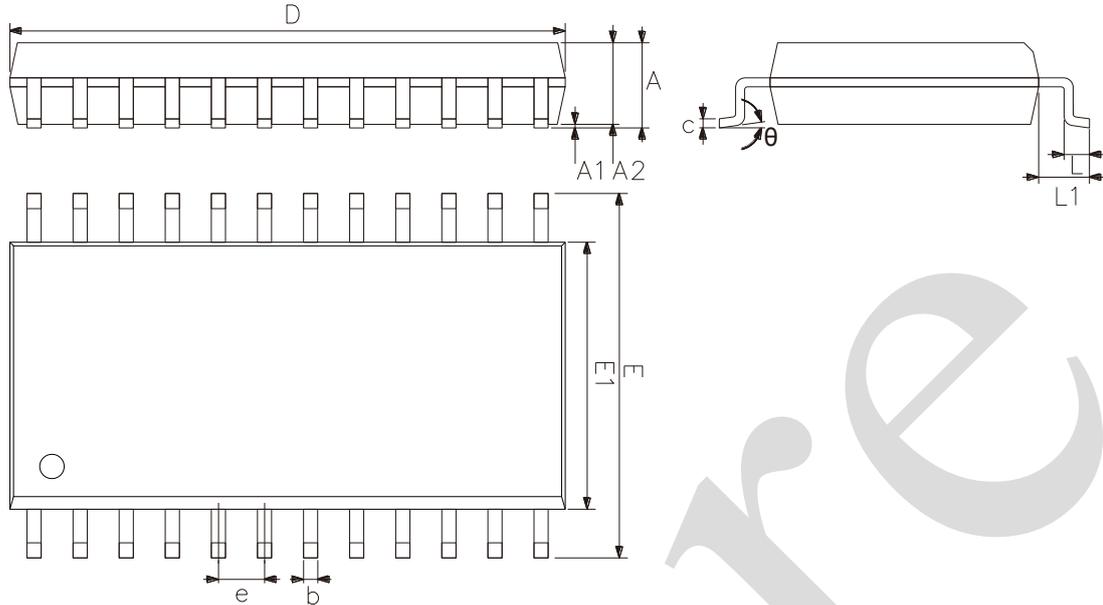
4.5、 Test Data

Test	Input		Load		S1 position
	V_M	t_r, t_f	C_L	R_L	
t_{PHL}	$0.5 \times V_{DD}$	$\leq 20\text{ns}$	50pF	10k Ω	V_{DD} or V_{SS}
t_{PLH}	$0.5 \times V_{DD}$	$\leq 20\text{ns}$	50pF	10k Ω	V_{SS}
t_{PZH}, t_{PHZ}	$0.5 \times V_{DD}$	$\leq 20\text{ns}$	50pF	10k Ω	V_{SS}
t_{PZL}, t_{PLZ}	$0.5 \times V_{DD}$	$\leq 20\text{ns}$	50pF	10k Ω	V_{DD}
other	$0.5 \times V_{DD}$	$\leq 20\text{ns}$	50pF	10k Ω	V_{SS}



5、Package Information

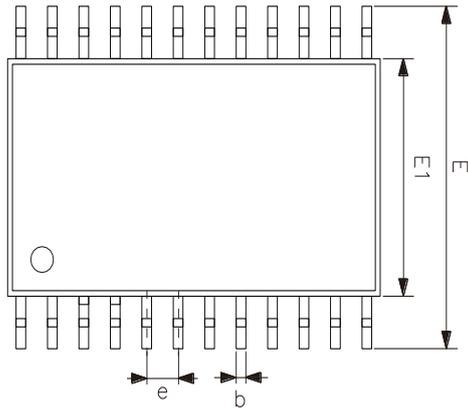
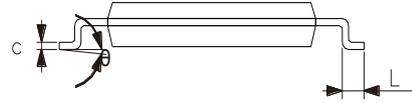
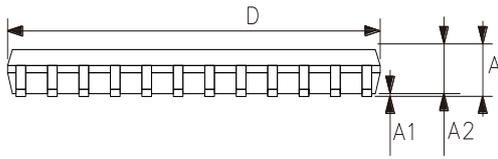
5.1、SOP24



2023/12/A	Dimensions In Millimeters	
Symbol	Min.	Max.
A	2.35	2.65
A1	0.10	0.30
A2	2.13	2.44
b	0.39	0.47
c	0.25	0.30
D	15.19	15.55
E	10.10	10.57
E1	7.40	7.62
e	1.27	
L	0.41	1.00
L1	1.30	1.50
θ	0°	8°



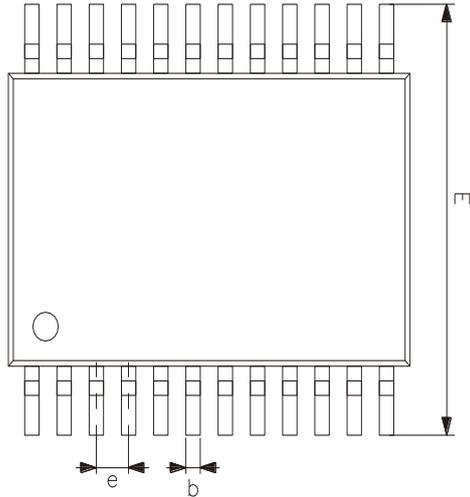
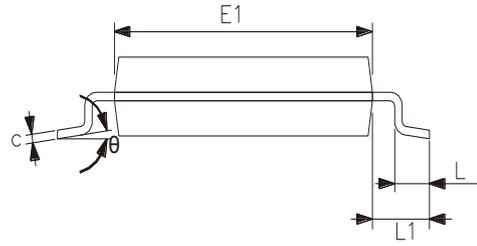
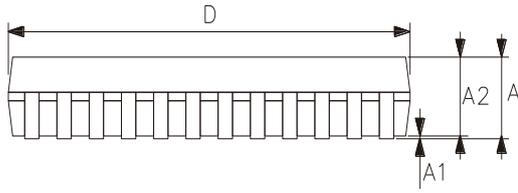
5.2、TSSOP24



2023/12/A Symbol	Dimensions In Millimeters	
	Min	Max
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.20	6.60
E1	4.30	4.50
e	0.65	
L	0.45	0.75
θ	0°	8°



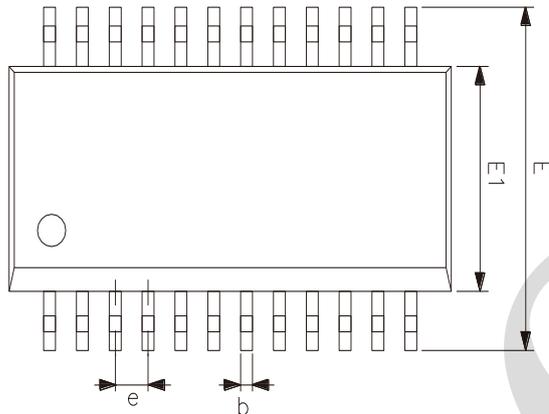
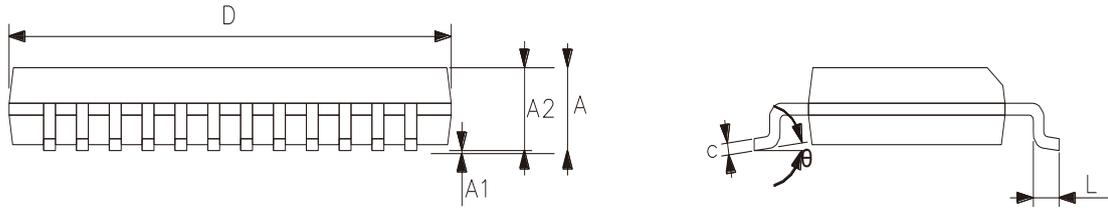
5.3、SSOP24 (0.65mm)



2023/12/A	Dimensions In Millimeters		
	Symbol	Min	Max
	A	1.60	2.00
	A1	0.05	0.25
	A2	1.40	1.85
	b	0.28	0.37
	c	0.15	0.20
	D	8.00	8.40
	E	7.60	8.00
	E1	5.10	5.50
	e	0.65	
	L	0.55	1.10
	L1	1.15	1.35
	θ	0°	8°



5.4、SSOP24 (0.635mm)



2023/12/A	Dimensions In Millimeters		
	Symbol	Min	Max
	A	1.35	1.75
	A1	0.10	0.25
	A2	1.30	1.55
	b	0.23	0.47
	c	0.19	0.26
	D	8.45	8.85
	E	5.80	6.20
	E1	3.70	4.10
	e	0.635	
	L	0.40	0.80
	θ	0°	8°



6、 Statements And Notes

6.1、 The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、 Notes

We recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer's third party users. I-Core does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials form i-Core's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.