CD4099
8-Bit Addressable Latch

Product Specification

Specification Revision History：

Version	Date	Description
2024-08-A0	2024-08	New
2025-03-A1	2025-03	Modify the parameters

Contents

1、General Description

The CD4099 8-bit addressable latch is a serial input, parallel output storage register that can perform a variety of functions.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Features:

- Supply voltage range:3V to 15V
- Temperature range:-40℃ to +125℃
- Packaging information: DIP16/SOP16/SSOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4099DA16.TB	DIP16	CD4099	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4099SA16.TR	SOP16	CD4099	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4099VB16.TR	SSOP16	CD4099	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 0.635mm
CD4099TA16.TR	TSSOP16	CD4099	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

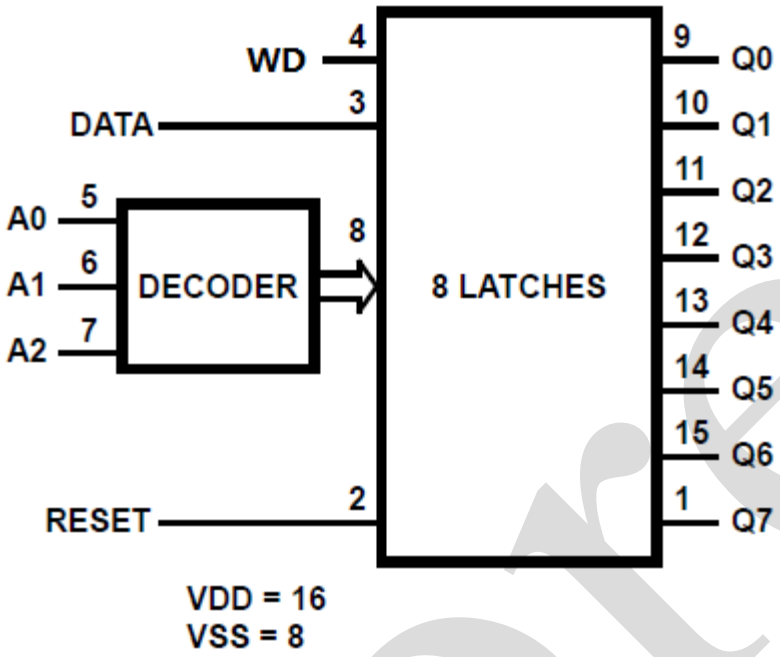
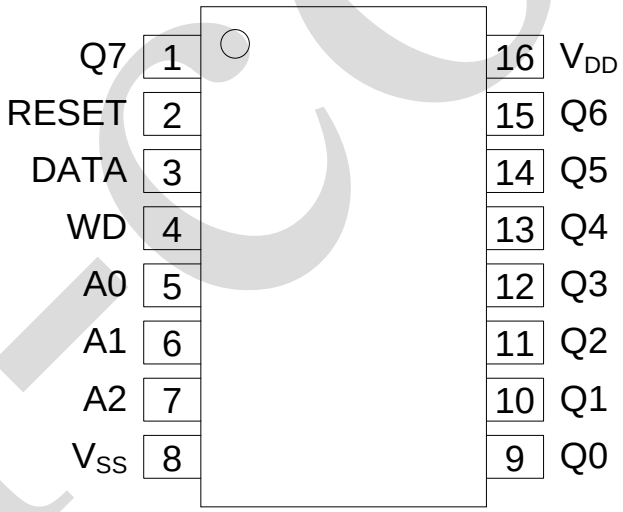


Figure 1. Functional diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	Q7	data output
2	RESET	reset
3	DATA	data input
4	WD	write disable
5	A0	address input
6	A1	address input
7	A2	address input
8	V_{SS}	ground (0V)
9	Q0	data output
10	Q1	data output
11	Q2	data output
12	Q3	data output
13	Q4	data output
14	Q5	data output
15	Q6	data output
16	V_{DD}	supply voltage

2.4、Function Table

Mode Selection			
WD	**RESET**	**Addressed Latch**	**Unaddressed Latch**
L	L	Follows Data	Holds Previous State
L	H	Follows Data	Reset to ‘0’
		(Active High 8-Channel Demultiplexer)	
H	L	Holds Previous State	
H	H	Reset to ‘0’	

Note: H=HIGH voltage level; L=LOW voltage level.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+18	V
input voltage	V_I	all inputs		-0.5	V_{DD}+0.5	V
DC input current	I_{IK}	any one input		-	±10	mA
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/SSOP/TSSOP	260		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	5V	-	3.5	-	-	V
		10V	-	7	-	-	V
		15V	-	11	-	-	V
LOW-level input voltage	V_{IL}	5V	-	-	-	1.5	V
		10V	-	-	-	3	V
		15V	-	-	-	4	V
HIGH-level output voltage	V_{OH}	5V	$\|I_O\|$<1uA	4.95	-	-	V
		10V	$\|I_O\|$<1uA	9.95	-	-	V
		15V	$\|I_O\|$<1uA	14.95	-	-	V
LOW-level output voltage	V_{OL}	5V	$\|I_O\|$<1uA	-	-	0.05	V
		10V	$\|I_O\|$<1uA	-	-	0.05	V
		15V	$\|I_O\|$<1uA	-	-	0.05	V
HIGH-level output current	I_{OH}	5V	V_O=4.6V	-	-	-0.34	mA
		5V	V_O=2.5V	-	-	-1.3	mA
		10V	V_O=9.5V	-	-	-0.55	mA
		15V	V_O=13.5V	-	-	-1.65	mA
LOW-level output current	I_{OL}	5V	V_O=0.4V	0.34	-	-	mA
		10V	V_O=0.5V	0.46	-	-	mA
		15V	V_O=1.5V	1.4	-	-	mA
input leakage current	I_I	15V	V_I=15V or GND	-	-	±1	uA
supply current	I_{DD}	5V	V_I=5V or GND;I_O=0A	-	-	150	uA
		10V	V_I=10V or GND;I_O=0A	-	-	300	uA
		15V	V_I=15V or GND;I_O=0A	-	-	600	uA

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	5V	-	3.5	-	-	V
		10V	-	7	-	-	V
		15V	-	11	-	-	V
LOW-level input voltage	V_{IL}	5V	-	-	-	1.5	V
		10V	-	-	-	3	V
		15V	-	-	-	4	V
HIGH-level output voltage	V_{OH}	5V	$\|I_O\|$<1uA	4.95	-	-	V
		10V	$\|I_O\|$<1uA	9.95	-	-	V
		15V	$\|I_O\|$<1uA	14.95	-	-	V
LOW-level output voltage	V_{OL}	5V	$\|I_O\|$<1uA	-	-	0.05	V
		10V	$\|I_O\|$<1uA	-	-	0.05	V
		15V	$\|I_O\|$<1uA	-	-	0.05	V
HIGH-level output current	I_{OH}	5V	V_O=4.6V	-	-	-0.3	mA
		5V	V_O=2.5V	-	-	-1.15	mA
		10V	V_O=9.5V	-	-	-0.45	mA
		15V	V_O=13.5V	-	-	-1.4	mA
LOW-level output current	I_{OL}	5V	V_O=0.4V	0.29	-	-	mA
		10V	V_O=0.5V	0.38	-	-	mA
		15V	V_O=1.5V	1.2	-	-	mA
input leakage current	I_I	15V	V_I=15V or GND	-	-	±1	uA
supply current	I_{DD}	5V	V_I=5V or GND;I_O=0A	-	-	150	uA
		10V	V_I=10V or GND;I_O=0A	-	-	300	uA
		15V	V_I=15V or GND;I_O=0A	-	-	600	uA

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, V_{SS}=0V, unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
propagation delay time data to output	t_{PHL}, t_{PLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	200	400	ns
		10V		-	75	150	ns
		15V		-	50	100	ns
propagation delay time WD to output	t_{PHL}, t_{PLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	200	400	ns
		10V		-	80	160	ns
		15V		-	60	120	ns
propagation delay time reset to output	t_{PHL}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	175	350	ns
		10V		-	80	160	ns
		15V		-	65	130	ns
propagation delay time address to output	t_{PHL}, t_{PLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	225	450	ns
		10V		-	100	200	ns
		15V		-	75	150	ns
transition time	t_{THL}, t_{TLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	100	200	ns
		10V		-	50	100	ns

		15V		-	40	80	ns
Minimum pulse width, data	t_W	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	100	200	ns
		10V		-	50	100	ns
		15V		-	40	80	ns
Minimum pulse width, address	t_W	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	200	400	ns
		10V		-	100	200	ns
		15V		-	65	125	ns
Minimum pulse width, reset	t_W	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	75	150	ns
		10V		-	40	75	ns
		15V		-	25	50	ns
Minimum setup time, data to WD	t_S	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	50	100	ns
		10V		-	25	50	ns
		15V		-	20	35	ns
Minimum hold time, data to WD	t_H	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	75	150	ns
		10V		-	40	75	ns
		15V		-	25	50	ns

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, V_{SS}=0V, unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
propagation delay time data to output	t_{PHL}, t_{PLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	480	ns
		10V		-	-	180	ns
		15V		-	-	120	ns
propagation delay time WD to output	t_{PHL}, t_{PLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	480	ns
		10V		-	-	192	ns
		15V		-	-	144	ns
propagation delay time reset to output	t_{PHL}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	420	ns
		10V		-	-	192	ns
		15V		-	-	156	ns
propagation delay time address to output	t_{PHL}, t_{PLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	540	ns
		10V		-	-	240	ns
		15V		-	-	180	ns
transition time	t_{THL}, t_{TLH}	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	240	ns
		10V		-	-	120	ns
		15V		-	-	96	ns
Minimum pulse width, data	t_W	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	240	ns
		10V		-	-	120	ns
		15V		-	-	96	ns
Minimum pulse width, address	t_W	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	480	ns
		10V		-	-	240	ns
		15V		-	-	150	ns
Minimum pulse width, reset	t_W	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	180	ns
		10V		-	-	90	ns
		15V		-	-	60	ns

Minimum setup time, data to WD	t_S	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	120	ns
		10V		-	-	60	ns
		15V		-	-	42	ns
Minimum hold time, data to WD	t_H	5V	C_L=50pF, R_L=200kΩ see Figure 4	-	-	180	ns
		10V		-	-	90	ns
		15V		-	-	60	ns

4、Testing Circuit

4.1、AC Testing Circuit

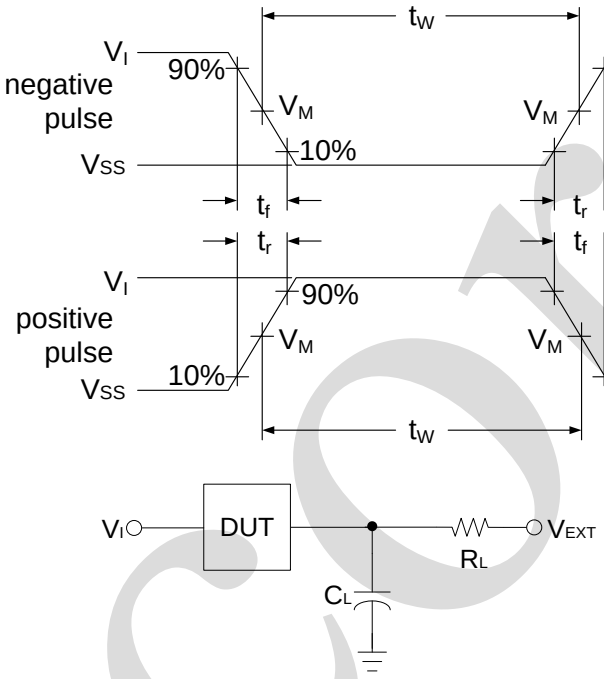


Figure 3. Load circuit

C_L includes probe and jig capacitance.

4.2、Test Data

Supply voltage	Input		Load		V_{EXT}
V_{DD}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}
5V to 15V	V_{CC}	≤ 3ns	50pF	200kΩ	Open

4.3、AC Testing Waveforms

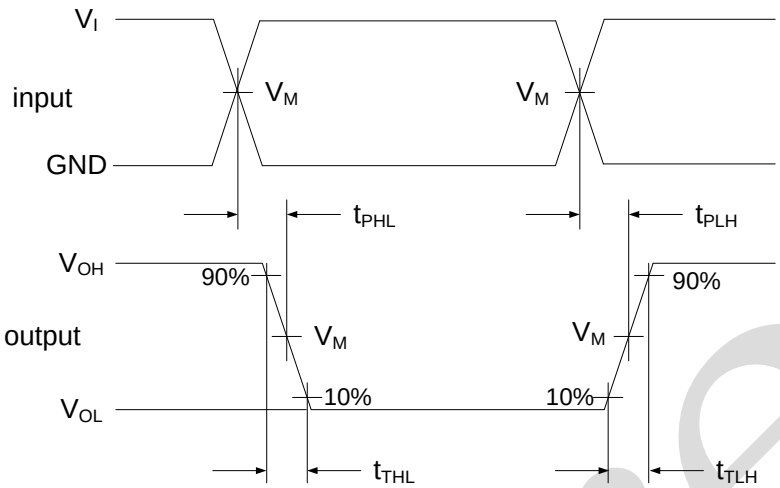


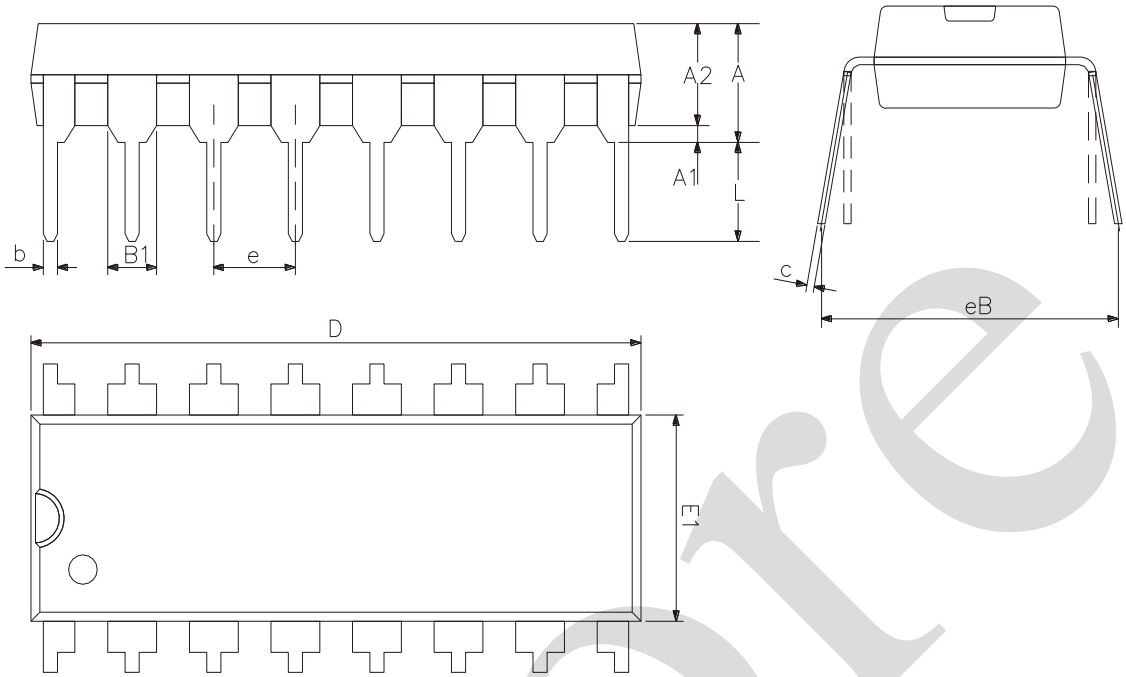
Figure 4. Propagation delay, output transition time

4.4、Measurement Points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 15V	$0.5\times V_{DD}$	$0.5\times V_{DD}$

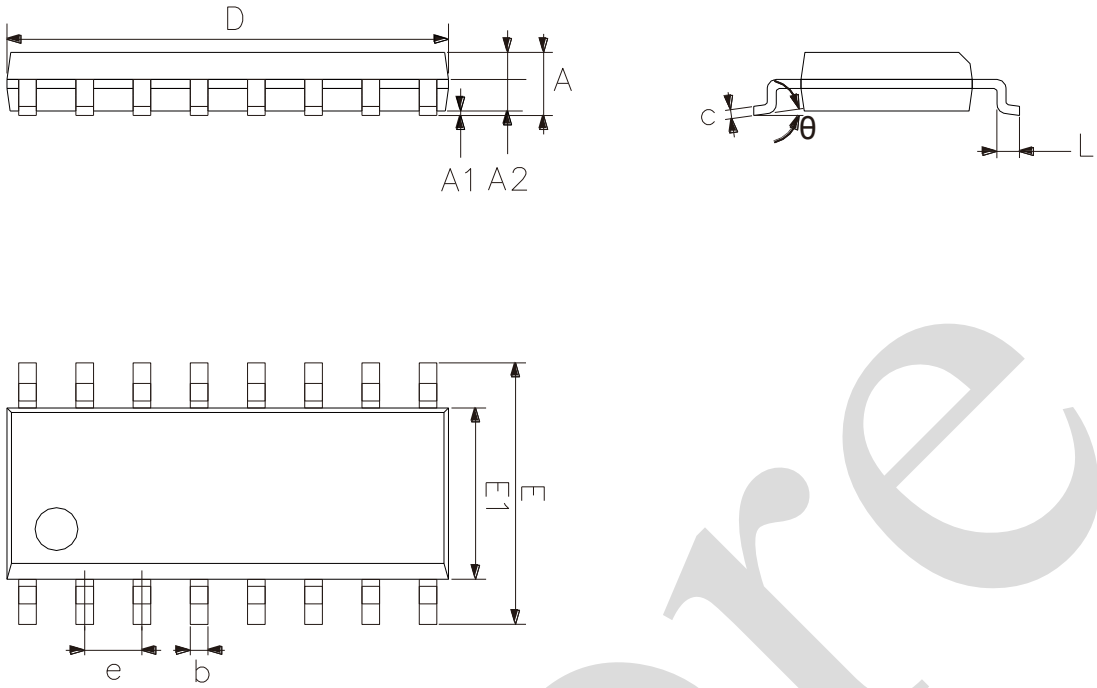
5、Package Information

5.1、DIP16



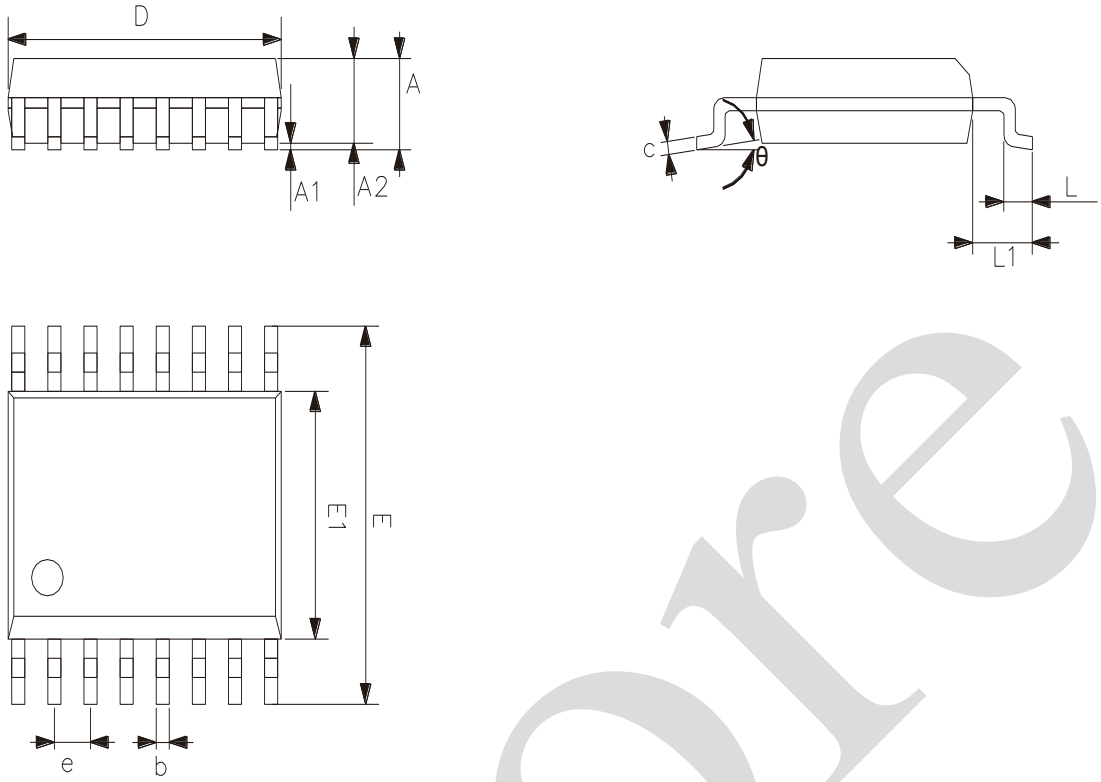
2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A2	3.00	3.60
A1	0.51	—
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

5.2、SOP16



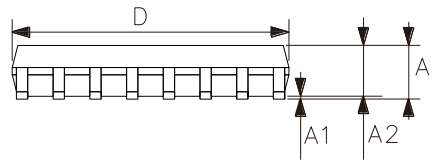
2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

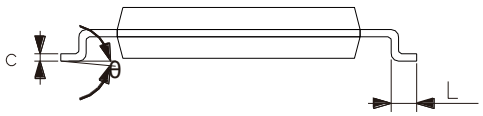
5.3、SSOP16

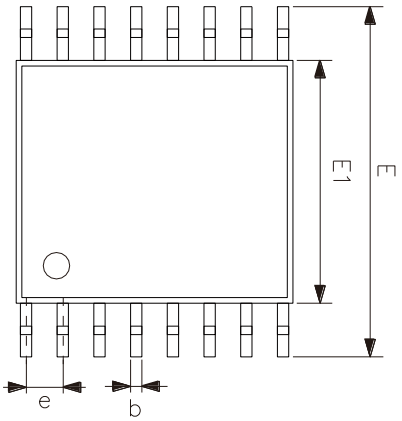


2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.75
A1	0.02	0.23
A2	1.30	1.50
b	0.23	0.31
c	0.20	0.24
D	4.70	5.10
E	5.80	6.25
E1	3.80	4.02
e	0.635	
L	0.45	0.80
L1	1.05	
θ	0°	8°

5.4、TSSOP16







2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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