Application Report
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ADC Gain Calibration—Extending the ADC Input Range in MSC12xx Devices

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ABSTRACT

The gain parameter plays an important role in analog-to-digital (A/D) conversion, especially in the high-resolution delta-sigma ($\Delta\Sigma$) A/D converter (ADC) implemented in the MSC1210, 1211 and 1212 devices. This application report discusses the following points:

a) Methods of ADC gain calibration (GC)

b) Adjusting the ADC gain

c) Extending the ADC input range

This article also applies to the ADS1216, ADS1217 and ADS1218 devices.

Contents

Figures

1 Introduction

The structure of the delta-sigma ADC used in the MSC12xx devices is described in an earlier application report [1], which analyzes the different aspects of ADC offset and the process of offset calibration. The ADC gain and offset parameters play an important role in obtaining precise conversion results. To ensure complete accuracy, it is necessary to do offset and gain calibration before collecting any data.

Ideally, the ADC gain for bipolar mode is:

$$\text{Gain} = 2\frac{V_{REF}}{V_{INMAX} - V_{INMIN}} \quad (1)$$

and for unipolar mode:

$$\text{Gain} = \frac{V_{REF}}{V_{INMAX} - V_{INMIN}} \quad (2)$$

where V_{INMAX} and V_{INMIN} are respectively a maximum and a minimum ADC input signal. Depending on the PGA setting, the ideal gain should be 1, 2, 4, 8, 16, 32, 64 or 128. In practice, the ADC gain is dependent on several factors: the voltage drop in the ADC input circuits; the precision of the PGA; the gain factor of the digital filter; and the precision of the value located in the gain calibration register (GCR). The purpose of the GCR is to compensate for gain variations in the previous ADC stages by multiplying the ADC output by the GCR constant. The data in the GCR is always positive, and is represented in binary two's complement code with the MSB always zero. This ADC output scaling is the last stage in A/D conversion, after which the ADC result is loaded into the output data register ADRES.

This article describes how to make the best use of the gain calibration register.

In the MSC12xx devices, the possible gain calibration procedures are:

a) Self-gain calibration

b) System gain calibration

c) Software gain calibration

Before considering each GC procedure, let us analyze what can influence the ADC gain and when the GC must be performed.

2 Factors Affecting ADC Gain: When is Gain Calibration Necessary?

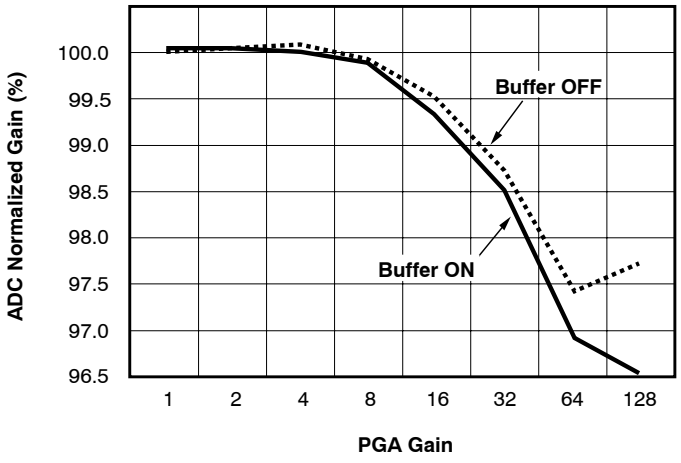
2.1 Input Circuitry

When the input buffer is OFF, there is some ADC input current caused by sampling capacitance recharge. This current ranges from approximately 1µA (PGA = 1) to 15µA (PGA = 128) and depends on the sampling frequency. This means that if the modulator clock doubles, the input current also doubles. (See [1] for further information.) During the system GC, the voltage drop caused by the input current can be compensated; but if the signal source resistance or capacitance has changed, it will affect the input circuit time constant and a new system GC may be needed.

2.2 PGA Setting

Each PGA setting has a different precision. For PGA 1, 2 and 4 the gain is close to ideal (see Figure 1), but higher PGA gains have more significant gain error. If the GC was performed at gain 1, and then the PGA is switched to a higher gain, a second GC may be needed; but performing a self-gain calibration will not help in this case, because a self-gain calibration is always done at gain 1. See Section 3 for more information.

ADC Normalized Gain After Self-Gain Calibration
AVDD = DVDD = 5V, V_{REF} = 2.5V



Buffer ON	100.0	100.0	100.0	99.8	99.4	98.5	96.9	96.6
Buffer OFF	100.0	100.0	100.0	99.9	99.5	98.8	97.4	97.7

Figure 1. ADC Gain Calibration after Self-Gain Calibration versus PGA Gain

2.3 Decimation Ratio

A change in the decimation ratio also changes the digital filter gain. Therefore, if the decimation ratio has changed, it is always necessary to perform GC.

2.4 Reference Voltage

A precise and stable gain is dependent on a precise and stable reference voltage. Changes in the reference voltage do not affect the ADC gain directly, but these changes do affect the precision and gain of the system as a whole, and can cause problems. Performing a self-GC will not help if the reference voltage has changed with respect to the rest of the system. However, a system GC can restore the scale in this case.

The user should be aware of the following features of the ADC reference input. The reference pin input current for the 2.5V reference is about 1.5μA, with PGA gain = 1 and a modulation frequency of 15KHz. If PGA gain increases, the current rises and reaches 7 – 10μA for gain = 128. When the modulation frequency doubles, the reference input current also doubles. Therefore, the actual reference voltage can be affected by the ADC operating conditions, such as the modulation clock and PGA gain. In the case of the MSC1211, each digital-to-analog converter (DAC) also adds about 12 – 25μA, depending on the V_{REF} value. If the external reference circuit has an RC filter with a 250Ω resistor, the 10μA reference current change will cause a 2.5 mV reference voltage drop, which is equivalent to 0.1% of V_{REF}. It is good practice to always verify the internal or external reference voltage with different ADC settings.

2.5 What Doesn't Affect the ADC Gain?

The MSC12xx ADC gain parameter is a much more stable parameter than the ADC offset described in [1]. As long as the signals stay within the allowable ADC input range (AGND + 50mV to AV_{DD} −1.5V for Buffer ON mode, and AGND − 0.1V to AV_{DD} + 0.2V for Buffer OFF mode), the gain is not significantly affected by the ADC common voltage, power supply voltage, differential reference common voltage and ADC inputs.

Also, the ADC gain is not significantly affected by the device temperature; see the typical curves in Figure 2.

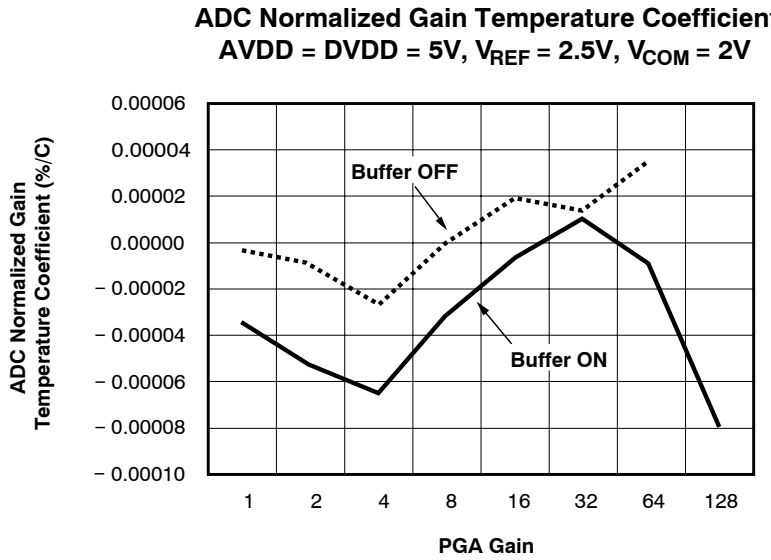


Figure 2. ADC Normalized Gain Temperature Coefficient versus PGA Gain

The three available ADC digital filters—Fast, Sinc2 and Sinc3—always have the same gain. Therefore, there is no need to do GC when switching between filters. This feature allows using Auto Mode in A/D conversion without changing the ADC gain.

2.6 When should Gain Calibration be Performed?

Each time the device is reset, the ADC should have both an offset and gain calibration done. As an alternative to performing a GC, the offset calibration register (OCR) and GCR may be reloaded with data stored from a previous calibration, if the environmental conditions have not changed.

A GC should also be done if one of the changes described in sections 2.1 – 2.4 has taken place.

3 Self-Gain Calibration Command

A self-GC is an internal calibration, which only corrects for internal error sources, since the ADC input circuitry is disconnected during a self-calibration.

The self-GC is usually performed after the offset calibration, and like the offset calibration, it requires seven data cycles. During self-GC the ADC inputs are internally connected to the reference pins, three samples are discarded, and the average of the four next samples is used to set the GCR. If the user initiates a combined self-offset and self-gain calibration command, it will require 14 data cycles before the ADC is ready to make data conversions.

There are two important points that the user should remember about self-gain calibration.

1. If the PGA gain is not 1, during self-GC the PGA switches to a gain of 1 before the GC is performed. This means that for gains larger than 1, there is no self-gain calibration and the user should use the typical gain curve shown in Figure 1 as a reference, or use either the system GC or software GC.

2. If the ADC buffer is used, then the ADC buffer input range limitation applies. Even though the signal range may be within the limits for data acquisition, it may not be acceptable for gain calibration. For example, if V_{REF_HIGH} is equal to AV_{DD}, which is 5V, V_{REF_LOW} is equal to 2.5V. For PGA = 1, a possible input signal range can be set between 0.5V and 3V, which will satisfy the buffer input criteria. But during self-GC one of the buffer inputs will be connected to V_{REF_HIGH} equal to 5V, which will cause an error. There are three possible options in this case: first, to disable the buffer; second, set V_{REF_HIGH} below AV_{DD} −1.5V; or third, switch the buffer OFF during self-gain calibration. Switching the buffer OFF does not introduce a significant error for the GC with PGA = 1 because the internal buffer gain is very close to 1 (see Fig. 1); for most cases, the error is negligible. But ADC offset is sensitive to the buffer presence, and therefore the buffer cannot be switched OFF during offset calibration.

4 System Gain Calibration Command

A system gain calibration is an external calibration, which corrects for external as well as internal error sources.

The system GC should also be done after offset calibration. To perform the system GC, the user should switch to the desired PGA gain, apply the desired positive full-scale input signal for this gain, and then initiate a system GC.

However, there is one problem that the user should be aware of. If the offset calibration was executed by self-offset calibration command (instead of system-offset calibration), the ADC zero can be shifted by the ADC offset value (see [1]). Now, when we apply the external full range signal, the ADC offset is added to the external full range signal; this changes the GC result. Therefore, a more precise gain calibration can be achieved when the system GC is used with the system-offset calibration. In this case, the ADC zero level and the ADC full-scale level are completely controlled by the user. The value of the external positive signal that can be applied to the ADC during system gain calibration is determined with this formula:

$$FS - ZL = K\frac{V_{REF}}{PGA} \tag{3}$$

where:

FS: The value of the full-scale signal for the chosen PGA gain

ZL: The value of the ADC zero-level signal used during system offset calibration for the chosen PGA gain

V_{REF}: ADC reference voltage

PGA: Programmable Gain Amplifier gain level.

K: Gain calibration coefficient. The allowable range of this coefficient is:

$$0.4 < K < 1.333$$

This means that with the system GC, the ADC input range can be changed from 60% below to 33% above the nominal input range set by V_{REF}/PGA. It is of little use, however, to make K less than 0.5, because it is then possible to simply use a greater PGA gain with better ENOB to achieve the same FS signal. For example, if we perform a system GC with gain = 1, V_{REF} = 2V, and input signal = 1V, K would be equal to 0.5, and the new input range for a unipolar signal will be between 0V and 1V. The same input range and resolution can be achieved by just switching from gain 1 to gain 2. In this case, however, ENOB is better, because when we switch to the next PGA gain, the resolution doubles but the noise increases only by a factor of 1.2 to 1.5.

5 Software Gain Calibration

There may be some cases when the precision of self-GC or system GC is not adequate. This condition usually occurs when the ADC has a low decimation ratio. A low ENOB leads to an imprecise average, since only four samples are used during GC, which in turn leads to an imprecise GC.

The simplest solution to this problem is to repeat the GC, store the content of the GCR, and reload it with the average value from several GC results. This method also protects the GC from accidental spikes during the calibration procedure. A spike while collecting data affects only some data, but a spike during calibration affects all subsequent results.

Another, more accurate GC method is to perform the self-GC and then, using the precise external signal and an average from as many ADC samples as needed, recalculate the GC value. This method is also convenient when we need to calibrate a high PGA gain, but a full-scale (FS) signal for a system GC is not available. The procedure consists of the following steps:

a) Perform a self-GC.

b) Apply a stable and precise external signal V_1 to the ADC (approximately one-quarter of the full-scale signal); obtain an average reading R_1 with as many samples as needed.

c) Apply a second external signal $V_2 = V_1 + U$ (where the value of U is around half of the FS value) to the ADC, and get the average reading R_2.

d) Read the GCR_{OLD} gain value from the GCR register, calculate the GCR_{NEW} gain value using Equation 4, and load the result to the GCR register.

$$GCR_{NEW} = \frac{U / V_{REF}}{R_2 - R_1} * GCR_{OLD} \quad (4)$$

This method works well, but its disadvantage is the need to switch from one precise voltage level to another during GC. To avoid using the two voltages, we need to eliminate or minimize ADC offset. For this purpose, one of the methods described in [1] can be used. If the offset value is close to zero, then it is possible to use only one input calibration signal V:

$$GCR_{NEW} = \frac{V / V_{REF}}{R} * GCR_{OLD} \quad (5)$$

where R is an average ADC reading for the input signal V.

Example

We need to calibrate the ADC with PGA gain 64. A precise FS input signal for the system GC is not available. Self-GC for this gain, according to Fig. 1, generates a gain error of around 3%.

One possible solution is to assign the input AINCOM to AGND and input AIN7 to the signal V, which should be approximately equal to (0.01)*V_{REF}. The signal V should be stable, but there is no need to have it precise. Perform both a self-offset and GC for these inputs with PGA = 1. Measure the signal V (using method 4.4 from [1]) with necessary averaging. This method assumes offset elimination by performing ADC input-swapping during measurement. Name the result P. Switch the PGA gain to 64. Perform an offset self-calibration for the gain 64. Measure the signal V with the gain 64 (using method 4.4 from [1]) with necessary averaging. Name the result R. Calculate the GCR_{NEW} value, using Equation 6, for gain 64 and load it to the GCR.

$$GCR_{NEW} = \frac{P * 64}{R} * GCR_{OLD} \quad (6)$$

Because ADC gain is not dependent on the input, when the GC for gain 64 is completed, we can switch the ADC to the other inputs for measurement.

In this example, we did not use an external precise signal for GC. Instead, we used a more precise PGA gain 1 to calibrate a PGA gain 64. Our experiments showed a gain error improvement from 3% to less than 0.2% for the PGA gain 64. Furthermore, for the MSC1211 device, instead of the external signal V, it is possible to use the signal from the internal voltage DAC, internally connected to ADC pin.

6 Adjusting ADC Gain

There are some cases when it is more convenient to have a gain different from the standard PGA gains of 1, 2, 4, 8, 16, 32, 64, or 128. The solution to this problem is very simple. When the GC is finished, the program reads the contents of the GCR, multiplies it by a desired scale factor (SF), and loads the result back to the GCR.

$$GCR_{NEW} = SF * GCR_{OLD} \quad (7)$$

For example, if there is a need to use a gain of 10, we select a PGA gain 16; after self-GC, simply multiply GCR_{OLD} by 0.625 (= 10/16). Now the ADC input signal gain will be 10.

If a scale factor smaller than 0.5 is needed, it is better to switch to the lower PGA gain, because the lower PGA gain has better ENOB performance for the same FS signal. If a user wants to choose a scale factor larger than one, there is a possibility of over-ranging the GCR after multiplication. The GCR value after self-gain calibration usually lies in the range of 0.5 – 0.8, depending on the ADC decimation value. For example, using a scale factor equal to 1.9, there is a strong probability that for many decimation values, this scale factor is too large, and an over-range will occur. This means that for scale factors greater than 1.0, some investigation may be needed to verify the functionality of the selected scale factor.

7 Extending the ADC Input Range

In the MSC12xx A/D conversion formula **AD** described in article [1], one can see the coefficient 0.75, which scales the input signal V_{IN}. This scaling coefficient means that when the positive FS input signal is applied, the output data of the ADC in the ADRES register (for bipolar mode) becomes 7FFFFF, and there are 25% 0s and 75% 1s in the ADC modulator output data flow. For a negative FS signal, which gives us the output data of 800000, there are 75% 0s and 25% 1s in the output data flow.

Here, we are talking about the situation when the GC is completed; the value in the GCR compensates the digital filter gain change from the decimation ratio and provides matching between the FS input signals and the maximum/minimum ADC output code. This also means that if we will increase the input signal beyond the V_{REF} value, the modulator will continue to work. Only when V_{IN} becomes equal to $\pm 1.33 * V_{REF}$ (1.33 = 1/0.75) will the modulator output saturate and become all ones. If now, after the GC procedure, we reload the GCR with the value $GCR_{NEW} = GCR_{OLD}/2$, we will be able to see the input signals greater than $V_{REF.}$ The ADC input range will look like that shown in Table 1.

Table 1. ADC Output Codes in Bipolar Mode

ADC Input, V_{IN}	ADRES After Calibration (Hex)	ADRES $GCR_{NEW} = GCR_{OLD}/2$ (Hex)
$>1.33 * V_{REF}$	7FFFFF†	555554†
$1.33 * V_{REF}$	7FFFFF†	555554†
V_{REF}	7FFFFF†	3FFFFF
+ 0	000000	000000
− 0	FFFFFF	FFFFFF
$- V_{REF}$	800000†	C00000
$-1.33 * V_{REF}$	800000†	AAAAAB†
$< - 1.33 * V_{REF}$	800000†	AAAAAB†

† ADC Code Saturated

The ADC input signal range is now $\pm 1.33 * V_{REF}$ / PGA, but input restrictions such as:

V_{IN} > AGND +50mV and V_{IN} < AV_{DD} −1.5V for buffer ON mode and

V_{IN} > AGND −100mV and V_{IN} < AV_{DD} +200mV for buffer OFF mode

should continue to be applied. All the ADC outputs in the ADRES register are now divided by two; the user should keep this in mind in the following calculation. It appears as if we lose some resolution when we divide the ADC result by two; but the actual ADC ENOB is lower than the 24-bit output resolution of the ADC, so significant information is not lost.

In addition to the advantage of the extended input signal range, there are two more reasons for using this method:

1. Working with the FS signal. If the ENOB for the signal near the FS is 16-bit, then the ADC data distribution is ±768 [= 3*(2^8)] LSB around the mean, or 0.009% of the FS. This means that the maximum applied signal should be FS minus this distribution; otherwise, the ADC result would be corrupted by the scale edge. This problem is resolved if the reduced GCR value is used.
2. Shift in the ADC input range. If, for example, as a result of the offset compensation procedure, or by applying the offset DAC or by some other reasons, the ADC range was shifted by 0.125 * V_{REF}, then the ADC scale for PGA = 1 bipolar mode will look like that given in Table 2.

Table 2. ADC Output Codes with and without Internal Shifting

ADC Input Signal	ADC Data Before Shifting	ADC Data After (0.125)*V_{REF} Shifting	ADC Data After Shifting, with $GCR_{NEW} = GCR_{OLD}/2$
V_{REF}	7FFFFF†	7FFFFF†	500000
0.875 * V_{REF}	700000	7FFFFF†	400000
0.125 * V_{REF}	100000	200000	100000
0	000000	100000	010000
− 0	FFFFFF	0FFFFF	07FFFF
− 0.125 * V_{REF}	F00000	000000	000000
− V_{REF}	800000†	800000†	C80000
− 1.125 * V_{REF}	800000†	800000†	C00000

† ADC Code Saturated

As you can see from column 3 of Table 2, instead of the standard input range ±V_{REF}, the input range now will be from −1.125 * V_{REF} to +0.875 * V_{REF}. But in column 4, where we have the offset shift and $GCR_{NEW} = GCR_{OLD} / 2$, the standard input range ± V_{REF} is again available.

8 Recommendations

Choose the reference voltage, the desired signal range, the ADC gain and gain precision that is needed for your system.

Analyze the factors that can affect the precision of the gain calibration or that can change the ADC gain during data conversions. Consider the reference voltage stability, PGA gain switching, device heating, and signal source internal resistance changes.

Choose the GC method and set the conditions that start the GC procedure besides the system reset. Consider the ratiometric method of measurements as another way to solve the gain error problem.

Conclusion

ADC gain error, beside ENOB, INL and offset, plays an important role in the system performance. Underestimating gain error can easily compromise the result. During the design period, the acceptable level of gain error should be set. After this baseline, the user should identify the most suitable method of gain calibration and determine when GC should be applied.

References

Gurevich, M. *ADC Offset in MSC12xx Devices.* Application Note (SBAA097A)

Wu, J. *Calibration Routines and Register Value Generation for the ADS121x Series*. Application Note (SBAA099)

MSC1210 Product data sheet (SBAS203A)

MSC1211 Product data sheet (SBAS267)

To obtain a copy of the referenced documents, visit the Texas Instruments web site at www.ti.com.

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