

Replaces X25043/X25045

4K

X5043/X5045

512 x 8 Bit

## CPU Supervisor with 4K SPI EEPROM

### FEATURES

- Selectable Timeout Watchdog Timer
- Low Vcc Detection and Reset Assertion
  - Five Standard Reset Threshold Voltages
  - Re-program Low Vcc Reset Threshold Voltage using special programming sequence.
  - Reset Signal Valid to Vcc=1V
- Long Battery Life With Low Power Consumption
  - <50 $\mu$ A Max Standby Current, Watchdog On
  - <10 $\mu$ A Max Standby Current, Watchdog Off
  - <2mA Max Active Current during Read
- 1.8V to 3.6V, 2.7V to 5.5V and 4.5V to 5.5V Power Supply Versions
- 4Kbits of EEPROM - 1M write cycle endurance
- Save Critical Data With Block Lock™ Memory
  - Protect 1/4, 1/2, all or none of E<sup>2</sup>PROM Array
- Built-in Inadvertent Write Protection
  - Write Enable Latch
  - Write Protect Pin
- 3.3MHz Clock Rate
- Minimize Programming Time
  - 16 Byte Page Write Mode
  - Self-Timed Write Cycle
  - 5ms Write Cycle Time (Typical)
- SPI Modes (0,0 & 1,1)
- Available Packages
  - 8-Lead MSOP, 8-Lead SOIC, 8 pin PDIP

### DESCRIPTION

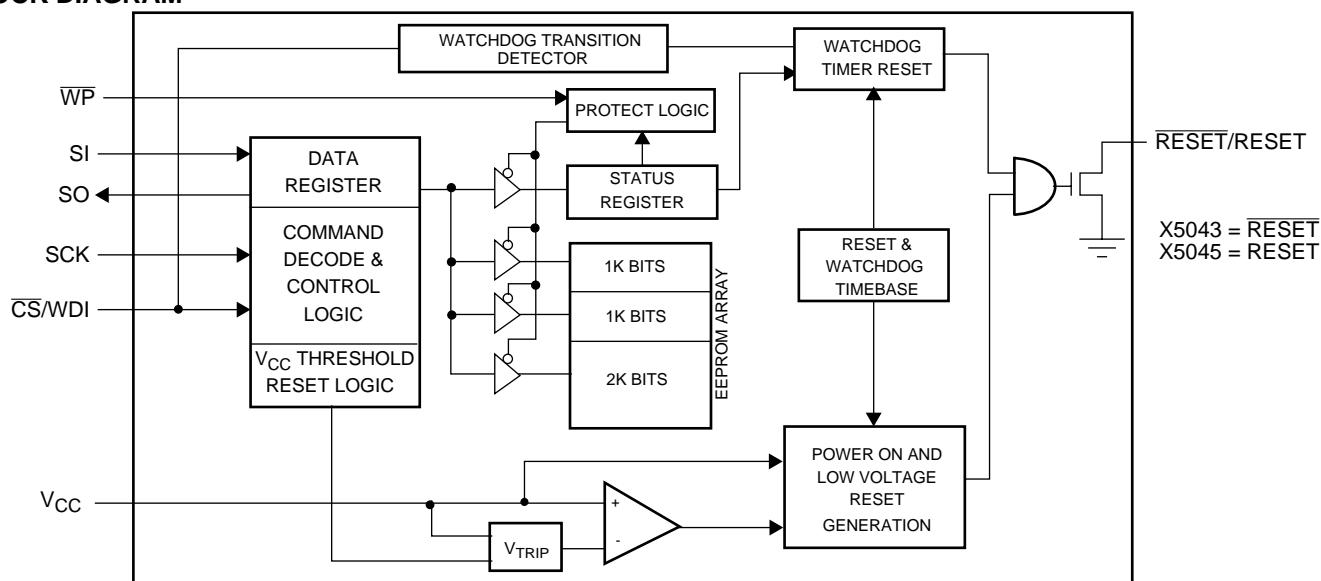
These devices combine four popular functions, Power-on Reset Control, Watchdog Timer, Supply Voltage Supervision, and Block Lock™ Protect Serial EEPROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power on reset circuit which holds  $\overline{\text{RESET}}$ /RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor executes code.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time-out interval, the device activates the  $\overline{\text{RESET}}$ /RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low Vcc detection circuitry protects the user's system from low voltage conditions, resetting the system when Vcc falls below the minimum Vcc trip point.  $\overline{\text{RESET}}$ /RESET is asserted until Vcc returns to proper operating level and stabilizes. Five industry standard Vtrip thresholds are available, however, Xicor's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.

### BLOCK DIAGRAM

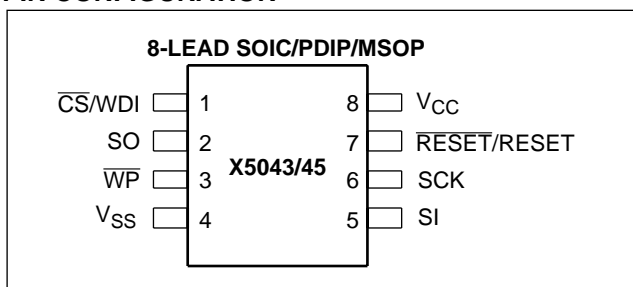


## X5043/X5045

The memory portion of the device is a CMOS Serial EEPROM array with Xicor's Block Lock™ Protection. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

### PIN CONFIGURATION



### PIN DESCRIPTIONS

PIN	Name	Function
1	CS/WDI	<b>Chip Select Input.</b> CS HIGH deselects the device and puts the SO output pin in a high impedance state. Unless a nonvolatile write cycle is underway, the device will be in the standby power mode when CS is HIGH. CS LOW enables the device, placing it in the active power mode. Prior to the start of any operation after power up, a HIGH to LOW transition on CS is required. After power-up, CS must transition HIGH-LOW prior to the start of any operation. <b>Watchdog Input.</b> A HIGH to LOW transition on the WDI pin restarts the Watchdog timer. The absence of a HIGH to LOW transition within the watchdog time-out period results in RESET/RESET going active.
2	SO	<b>Serial Output.</b> SO is a push/pull serial data output pin. A read cycle shifts data out on this pin. The falling edge of the serial clock (SCK) clocks the data out.
3	WP	<b>Write Protect.</b> When the WP pin is LOW, write operations to the X5043/5045 are disabled, but the part otherwise functions normally. When the WP pin is HIGH, all functions, including writes operate normally. WP going LOW while CS is LOW will interrupt a write to the X5043/X5045. If the internal nonvolatile write cycle has already been initiated, WP going LOW will have no effect on the write operation.
4	V <sub>SS</sub>	Ground
5	SI	<b>Serial Input.</b> SI is a serial data input pin. Input all opcodes, byte addresses, and memory data on this pin. The rising edge of the serial clock (SCK) latches the input data. Send all opcodes (Table 1), addresses and data MSB first.
6	SCK	<b>Serial Clock.</b> The Serial Clock controls the serial bus timing for data input and output. The rising edge of SCK latches in the opcode, address, or data bits present on the SI pin. The falling edge of SCK changes the data output on the SO pin.
7	RESET/RESET	<b>Reset Output.</b> RESET/RESET is an active LOW/HIGH, open drain output which goes active whenever V <sub>CC</sub> falls below the minimum V <sub>CC</sub> sense level. It will remain active until V <sub>CC</sub> rises above the minimum V <sub>CC</sub> sense level for 200ms. RESET/RESET will also go active if the Watchdog Timer is enabled and CS remains either HIGH or LOW longer than the selectable Watchdog time-out period. A falling edge of CS will reset the Watchdog Timer. For the X5043, the RESET output is active LOW. For the X5045, the RESET output is active HIGH. Since the RESET/RESET output is open drain it requires a pull up resistor.
8	V <sub>CC</sub>	Supply Voltage

### PRINCIPLES OF OPERATION

#### Power On Reset

Application of power to the X5043/X5045 activates a Power On Reset Circuit. This circuit pulls the RESET/RESET pin active. RESET/RESET prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator.

When V<sub>CC</sub> exceeds the device V<sub>TRIP</sub> value for 200ms (nominal) the circuit releases RESET/RESET, allowing the processor to begin executing code.

#### Low voltage monitoring

During operation, the X5043/X5045 monitors the V<sub>CC</sub> level and asserts RESET/RESET if supply voltage falls below a preset minimum V<sub>TRIP</sub>. The RESET/RESET

## X5043/X5045

signal prevents the microprocessor from operating in a power fail or brownout condition. The RESET/RESET signal remains active until the voltage drops below 1V. It also remains active until  $V_{CC}$  returns and exceeds  $V_{TRIP}$  for 200ms.

### Watchdog timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the WDI input. The microprocessor must toggle the CS/WDI pin periodically to prevent an active RESET/RESET signal. The CS/WDI pin must be toggled from HIGH to LOW prior to the expiration of the watchdog time-out period. The state of two nonvolatile control bits in the Status Register determines the watchdog timer period. The microprocessor can change these watchdog bits. With no microprocessor action, the watchdog timer control bits remain unchanged, even during total power failure.

### Vcc Threshold Reset Procedure

The X5043/X5045 is shipped with a standard  $V_{CC}$  threshold ( $V_{TRIP}$ ) voltage. This value will not change over normal operating and storage conditions.

However, in applications where the standard  $V_{TRIP}$  is not exactly right, or if higher precision is needed in the  $V_{TRIP}$  value, the X5043/X5045 threshold may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

### Setting the $V_{TRIP}$ Voltage

This procedure is used to set the  $V_{TRIP}$  to a higher voltage value. For example, if the current  $V_{TRIP}$  is 4.4V and the new  $V_{TRIP}$  is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new  $V_{TRIP}$  voltage, apply the desired  $V_{TRIP}$  threshold voltage to the  $V_{CC}$  pin and tie the  $\overline{WP}$  pin to the programming voltage  $V_P$ . Then send a WREN command, followed by a write of Data 00h to address 01h.  $\overline{CS}$  going HIGH on the write operation initiates the  $V_{TRIP}$  programming sequence. Bring  $\overline{WP}$  LOW to complete the operation.

**Note:** This operation also writes 00h to array address 01h.

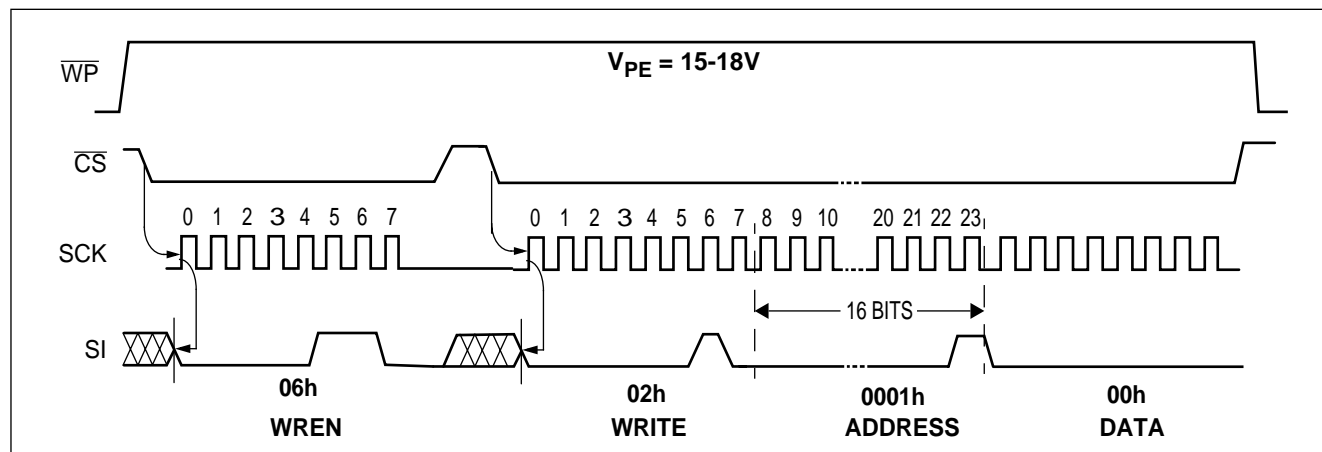


Figure 1. Set  $V_{TRIP}$  Level Sequence ( $V_{CC}$ =desired  $V_{TRIP}$  value. )

### Resetting the $V_{TRIP}$ Voltage

This procedure is used to set the  $V_{TRIP}$  to a "native" voltage level. For example, if the current  $V_{TRIP}$  is 4.4V and the new  $V_{TRIP}$  must be 4.0V, then the  $V_{TRIP}$  must be reset. When  $V_{TRIP}$  is reset, the new  $V_{TRIP}$  is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the  $V_{TRIP}$  voltage, apply at least 3V to the  $V_{CC}$  pin and tie the  $\overline{WP}$  pin to the programming voltage  $V_P$ . Then send a WREN command, followed by a write of Data 00h to address 03h.  $\overline{CS}$  going HIGH on the write operation initiates the  $V_{TRIP}$  programming sequence. Bring  $\overline{WP}$  LOW to complete the operation.

**Note:** This operation also writes 00h to array address 03h.

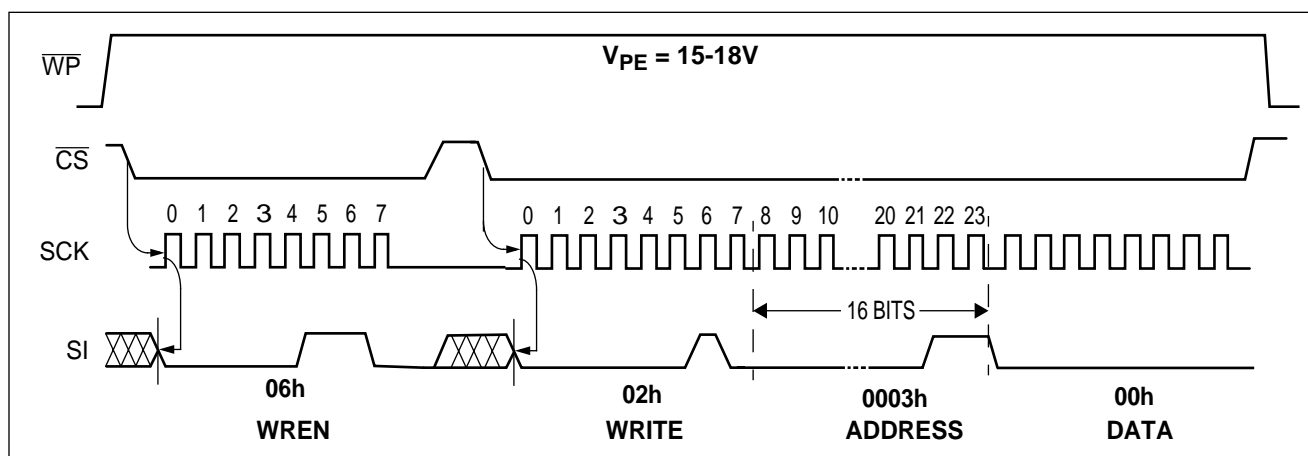


Figure 2. Reset  $V_{TRIP}$  Level Sequence ( $V_{CC} > 3V$ ,  $\overline{WP} = 15-18V$ )

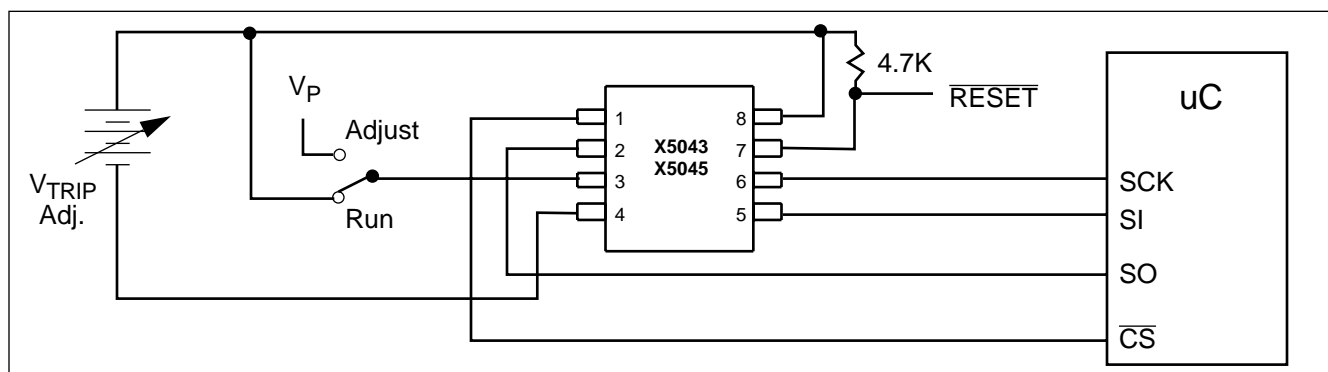


Figure 3. Sample  $V_{TRIP}$  Reset Circuit

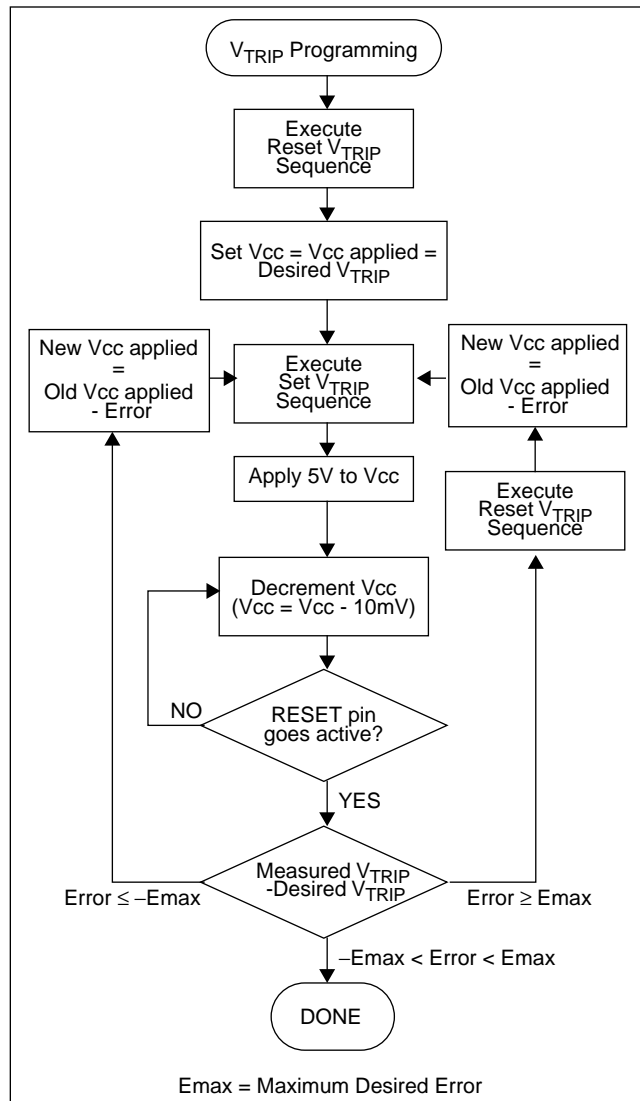


Figure 4.  $V_{TRIP}$  Programming Sequence

## SPI Serial Memory

The memory portion of the device is a CMOS Serial EEPROM array with Xicor's Block Lock™ Protection. The array is internally organized as x8 bits. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The device contains an 8-bit instruction register that controls the operation of the device. The instruction code is written to the device via the SI input. There are two write operations that requires only the instruction byte. There are two read operations that use the instruction byte to initiate the output of data. The remainder of the operations require an instruction byte, an 8-bit address, then data bytes. All instruction, address and data bits are clocked by the SCK input. All instructions (Table 1), addresses and data are transferred MSB first.

## Clock and Data Timing

Data input on the SI line is latched on the first rising edge of SCK after  $\overline{CS}$  goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.  $\overline{CS}$  must be LOW during the entire operation.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RSDR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Watchdog and BlockLock)
READ	0000 A <sub>8</sub> 011	Read Data from Memory Array Beginning at Selected Address
WRITE	0000 A <sub>8</sub> 010	Write Data to Memory Array Beginning at Selected Address (1 to 16 bytes)

\*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

## Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid byte, page, or status register write cycle. The latch is also reset if  $\overline{WP}$  is brought LOW.

When issuing a WREN, WRDI or RDSR commands, it is not necessary to send a byte address or data.

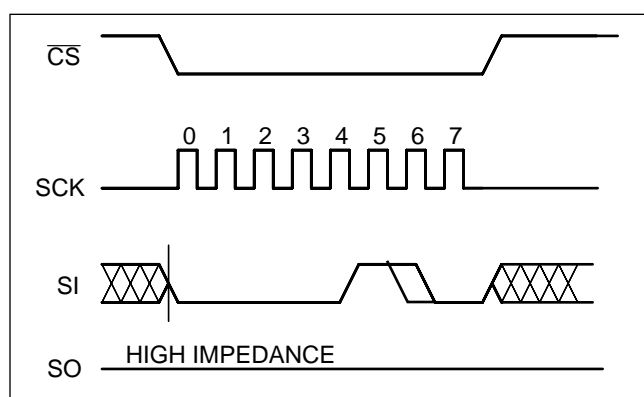


Figure 5. Write Enable/Disable Latch Sequence

## Status Register

The Status Register contains four nonvolatile control bits and two volatile status bits. The control bits set the operation of the watchdog timer and the memory Block Lock protection. The Status Register is formatted as shown in "Status Register".

### Status Register: (Default = 00H)

7	6	5	4	3	2	1	0
0	0	WD1	WD0	BL1	BL0	WEL	WIP

The Write-In-Progress (WIP) bit is a volatile, read only bit and indicates whether the device is busy with an internal nonvolatile write operation. The WIP bit is read using the RDSR instruction. When set to a "1", a nonvolatile write operation is in progress. When set to a "0", no write is in progress.

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When WEL=1, the latch is set and when WEL=0 the latch is reset. The WEL bit is a volatile, read only bit. The WREN instruction sets the WEL bit and the WRDS instruction resets the WEL bit.

The Block Lock bits, BL0 and BL1, set the level of Block Lock™ Protection. These nonvolatile bits are programmed using the WRSR instruction and allow the user to protect one quarter, one half, all or none of the EEPROM array. Any portion of the array that is Block Lock Protected can be read but not written. It will remain protected until the BL bits are altered to disable Block Lock Protection of that portion of memory..

Status Reg Bits		Array Addresses Protected
BL1	BL0	X5043/X5045
0	0	None
0	1	\$180-\$1FF
1	0	\$100-\$1FF
1	1	\$000-\$1FF

The Watchdog Timer bits, WD0 and WD1, select the Watchdog Time-out Period. These nonvolatile bits are programmed with the WRSR instruction.

Status Register Bits		Watchdog Time-out (Typical)
WD1	WD0	
0	0	1.4 Seconds
0	1	600 Milliseconds
1	0	200 Milliseconds
1	1	Disabled

## Read Status Register

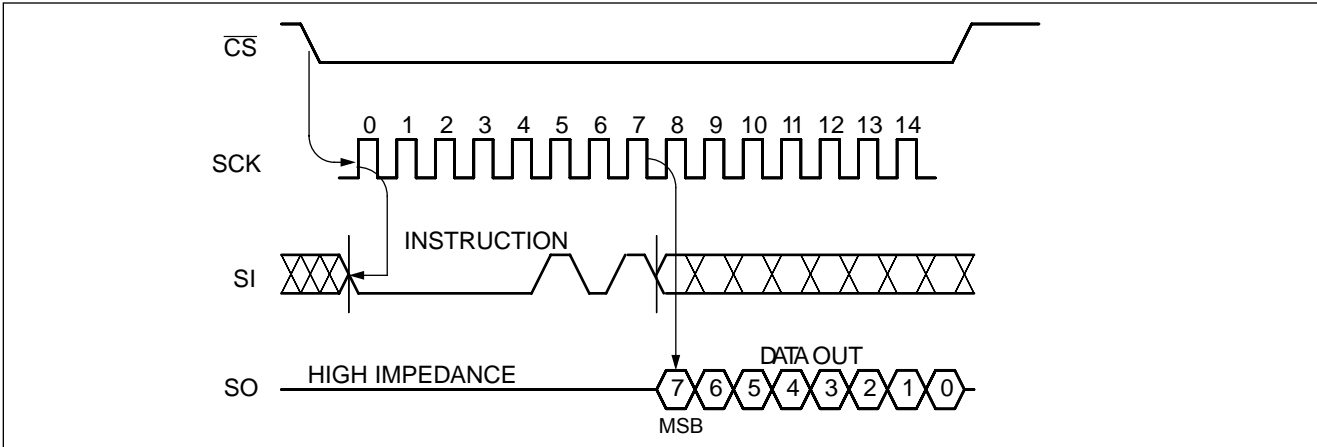
To read the Status Register, pull  $\overline{CS}$  low to select the device, then send the 8-bit RDSR instruction. Then the contents of the Status Register are shifted out on the SO line, clocked by CLK. Refer to the Read Status Register Sequence (Figure 6). The Status Register may be read at any time, even during a Write Cycle.

## Write Status Register

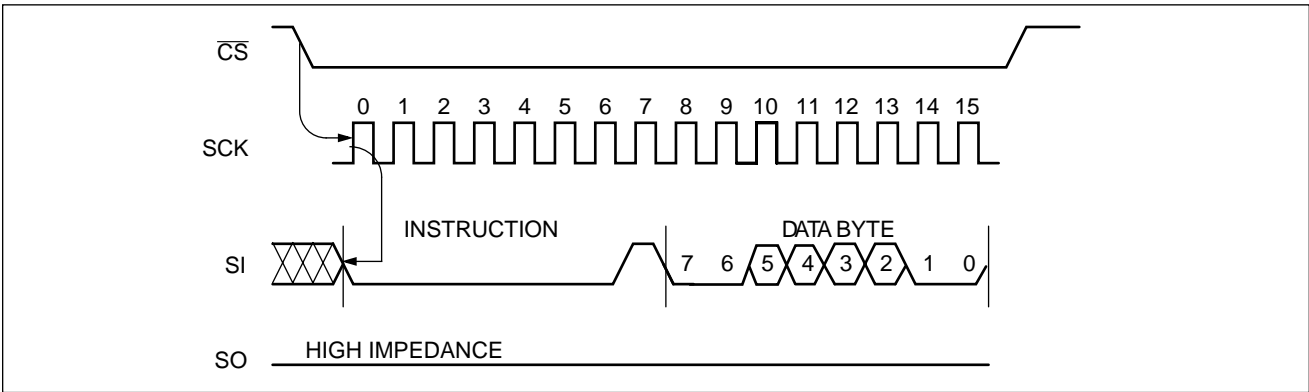
Prior to any attempt to write data into the status register, the "Write Enable" Latch (WEL) must be set by issuing the WREN instruction (Figure 5). First pull  $\overline{CS}$  LOW, then clock the WREN instruction into the device and pull  $\overline{CS}$  HIGH. Then bring  $\overline{CS}$  LOW again and enter the WRSR instruction followed by 8 bits of data. These 8 bits of data correspond to the contents of the status register. The operation ends with  $\overline{CS}$  going HIGH. If  $\overline{CS}$  does not go HIGH between WREN and WRSR, the WRSR instruction is ignored.

**Table 2. Device Protect Matrix**

WREN CMD (WEL)	DEVICE PIN (WP)	Memory Block		STATUS REGISTER (BL0, BL1, WD0, WD1)
		Protected area	Unprotected area	
0	x	Protected	Protected	Protected
x	0	Protected	Protected	Protected
1	1	Protected	Writable	Writable



**Figure 6. Read Status Register Sequence**



**Figure 7. Write Status Register Sequence**

**Read Memory Array**

When reading from the EEPROM memory array,  $\overline{CS}$  is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 8-bit address. Bit 3 of the READ instruction selects the upper or lower half of the device. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address

can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address \$000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high. Refer to the Read EEPROM Array Sequence (Figure 8).

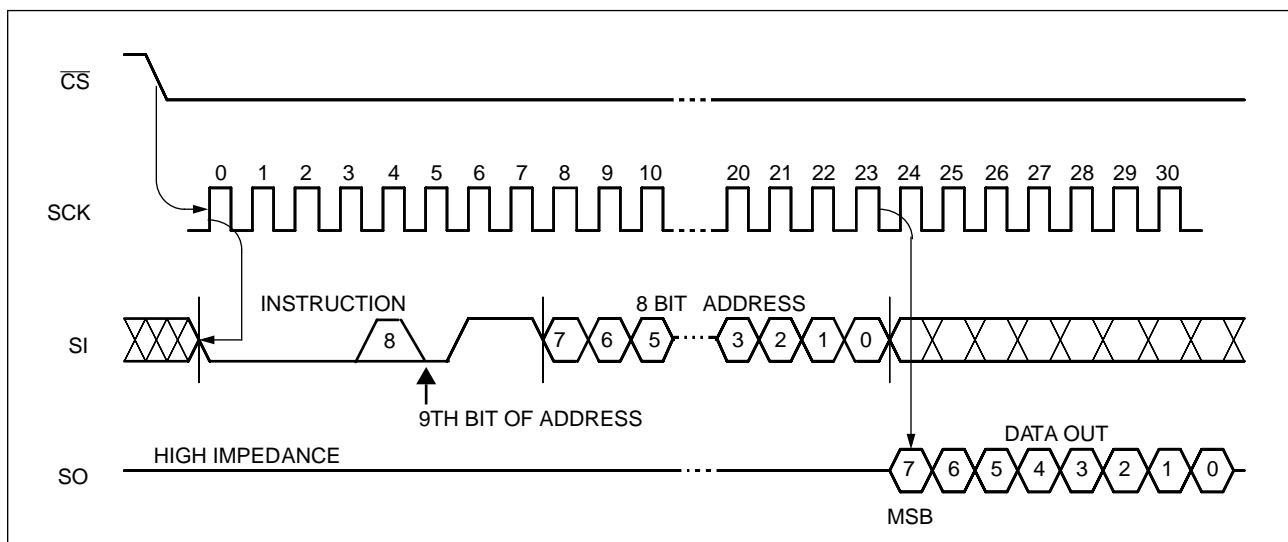


Figure 8. Read EEPROM Array Sequence

### Write Memory Array

Prior to any attempt to write data into the memory array, the “Write Enable” Latch (WEL) must be set by issuing the WREN instruction (Figure 5). First pull  $\overline{CS}$  LOW, then clock the WREN instruction into the device and pull  $\overline{CS}$  HIGH. Then bring  $\overline{CS}$  LOW again and enter the WRITE instruction followed by the 8-bit address and then the data to be written. Bit 3 of the WRITE instruction contains address bit  $A_8$ , which selects the upper or lower half of the array. If  $\overline{CS}$  does not go HIGH between WREN and WRITE, the WRITE instruction is ignored.

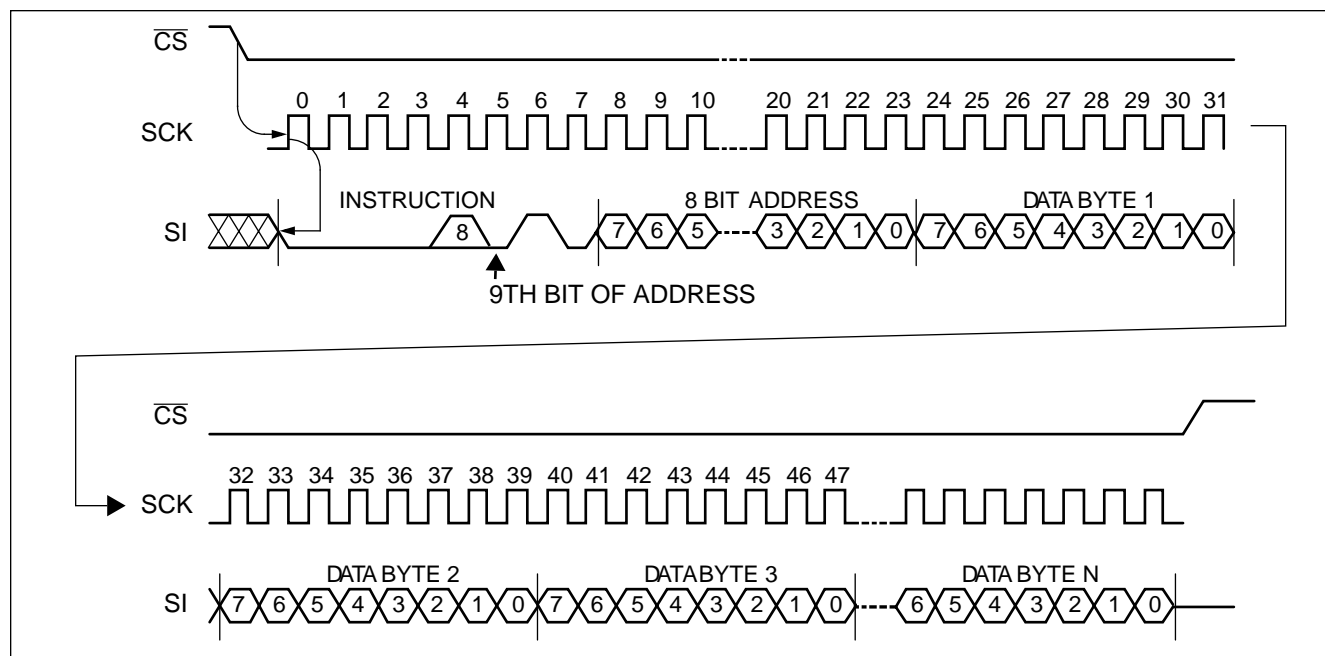
The WRITE operation requires at least 24 clocks.  $\overline{CS}$  must go low and remain low for the duration of the operation. The host may continue to write up to 16 bytes of data. The only restriction is that the 16 bytes

must reside within the same page. A page address begins with address [x xxxx 0000] and ends with [x xxxx 1111]. If the byte address reaches the last byte on the page and the clock continues, the counter will roll back to the first address of the page and overwrite any data that has been previously written.

For the write operation (byte or page write) to be completed,  $\overline{CS}$  must be brought HIGH after bit 0 of the last complete data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 9).

While the write is in progress following a status register or memory array write sequence, the Status Register may be read to check the WIP bit. WIP is HIGH while the nonvolatile write is in progress.





**Figure 9. Write Memory Sequence**

## Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on  $\overline{CS}$  is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The Write Enable Latch is reset.
- The Flag Bit is reset.
- Reset Signal is active for  $t_{PURST}$ .

## Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the Write Enable Latch.
- $\overline{CS}$  must come HIGH at the proper clock count in order to start a nonvolatile write cycle.
- Block Protect bits provide additional level of write protection for the memory array.
- The  $\overline{WP}$  pin LOW blocks nonvolatile write operations.

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## ABSOLUTE MAXIMUM RATINGS\*

Temperature under Bias ..... -65°C to +135°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on any Pin with Respect to  $V_{SS}$  ... -1.0V to +7V  
 D.C. Output Current ..... 5mA  
 Lead Temperature (Soldering, 10 seconds) ..... 300°C

## RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Option	Supply Voltage Limits
-1.8	1.8V to 3.6V
-2.7, -2.7A	2.7V to 5.5V
Blank, -4.5A	4.5V to 5.5V

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions/Comments
		Min.	Typ. <sup>(2)</sup>	Max.		
$I_{CC1}$	$V_{CC}$ Write Current (Active)			3	mA	SCK = 3.3MHz <sup>(3)</sup> ; SO, RESET, RESET= Open
$I_{CC2}$	$V_{CC}$ Read Current (Active)			2	mA	SCK = 3.3MHz <sup>(3)</sup> ; SI= $V_{SS}$ , RESET, RESET= Open
$I_{SB1}$	$V_{CC}$ Standby Current WDT=OFF			10	μA	$\overline{CS} = V_{CC}$ , SCK, SI = $V_{SS}$ , $V_{CC} = 5.5V$
$I_{SB2}$	$V_{CC}$ Standby Current WDT=ON			50	μA	$\overline{CS} = V_{CC}$ , SCK, SI = $V_{SS}$ , $V_{CC} = 5.5V$
$I_{LI}$	Input Leakage Current		0.1	10	μA	SCK, SI, WP = $V_{SS}$ to $V_{CC}$
$I_{LO}$	Output Leakage Current		0.1	10	μA	SO, RESET, RESET = $V_{SS}$ to $V_{CC}$
$V_{IL}^{(1)}$	Input LOW Voltage	-0.5		$V_{CC} \times 0.3$	V	SCK, SI, WP, $\overline{CS}$
$V_{IH}^{(1)}$	Input HIGH Voltage	$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V	SCK, SI, WP, $\overline{CS}$
$V_{OL}$	Output LOW Voltage (SO)			0.4	V	$I_{OL} = 2mA$ @ $V_{CC} = 2.7V$ $I_{OL} = 0.5mA$ @ $V_{CC} = 1.8V$
$V_{OH1}$	Output HIGH Voltage (SO)	$V_{CC} - 0.8$			V	$V_{CC} > 3.3V$ , $I_{OH} = -1.0mA$
$V_{OH2}$	Output HIGH Voltage (SO)	$V_{CC} - 0.4$			V	$2V < V_{CC} \leq 3.3V$ , $I_{OH} = -0.4mA$
$V_{OH3}$	Output HIGH Voltage (SO)	$V_{CC} - 0.2$			V	$V_{CC} \leq 2V$ , $I_{OH} = -0.25mA$
$V_{OLRS}$	Output LOW Voltage (RESET, RESET)			0.4	V	$I_{OL} = 1mA$

## CAPACITANCE $T_A = +25^\circ C$ , $f = 1MHz$ , $V_{CC} = 5V$ .

Symbol	Test	Max.	Units	Conditions
$C_{OUT}^{(2)}$	Output Capacitance (SO, RESET, RESET)	8	pF	$V_{OUT} = 0V$
$C_{IN}^{(2)}$	Input Capacitance (SCK, SI, $\overline{CS}$ , WP)	6	pF	$V_{IN} = 0V$

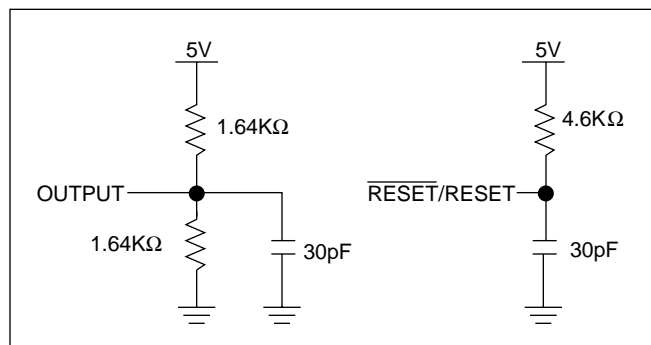
Notes: (1)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.

(2) This parameter is periodically sampled and not 100% tested.

(3) SCK frequency measured from  $V_{CC} \times 0.1/V_{CC} \times 0.9$  @

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### EQUIVALENT A.C. LOAD CIRCUIT AT 5V $V_{CC}$



### A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$

### A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

#### Data Input Timing

Symbol	Parameter	1.8-3.6V		2.7V-5.5V		Units
		Min.	Max.	Min.	Max.	
$f_{SCK}$	Clock Frequency	0	2	0	3.3	MHz
$t_{CYC}$	Cycle Time	500		300		ns
$t_{LEAD}$	$\overline{CS}$ Lead Time	250		150		ns
$t_{LAG}$	$\overline{CS}$ Lag Time	250		150		ns
$t_{WH}$	Clock HIGH Time	200		130		ns
$t_{WL}$	Clock LOW Time	200		130		ns
$t_{SU}$	Data Setup Time	50		30		ns
$t_H$	Data Hold Time	50		30		ns
$t_{RI}^{(3)}$	Input Rise Time		2		2	$\mu s$
$t_{FI}^{(3)}$	Input Fall Time		2		2	$\mu s$
$t_{CS}$	$\overline{CS}$ Deselect Time	250		100		ns
$t_{WC}^{(4)}$	Write Cycle Time		10		10	ms

#### Data Output Timing

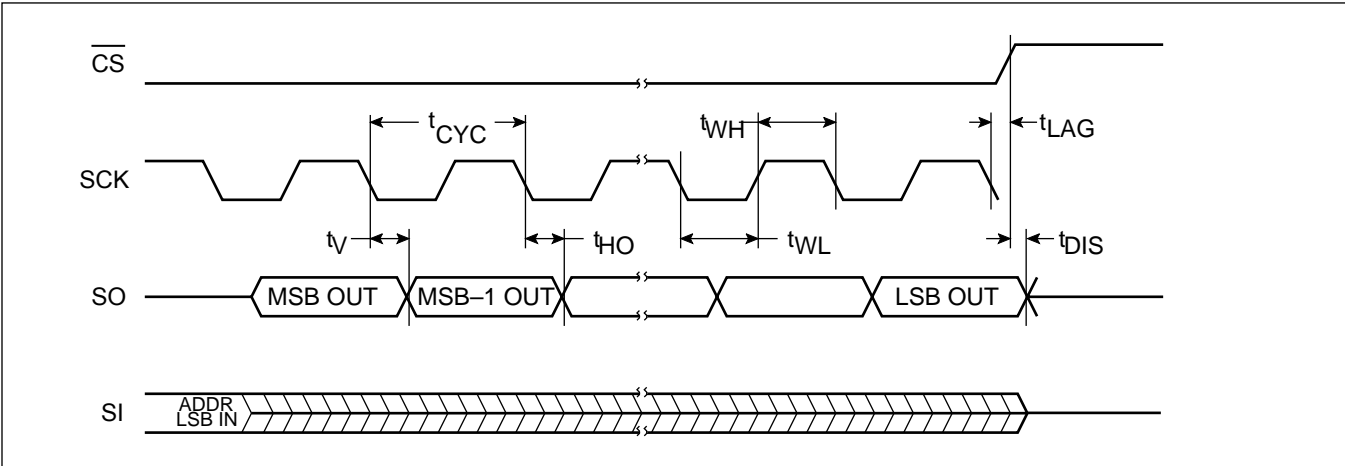
Symbol	Parameter	1.8-3.6V		2.7V-5.5V		Units
		Min.	Max.	Min.	Max.	
$f_{SCK}$	Clock Frequency	0	2	0	3.3	MHz
$t_{DIS}$	Output Disable Time		250		150	ns
$t_V$	Output Valid from Clock Low		200		120	ns
$t_{HO}$	Output Hold Time	0		0		ns
$t_{RO}^{(3)}$	Output Rise Time		100		50	ns
$t_{FO}^{(3)}$	Output Fall Time		100		50	ns

**Notes:** (3) This parameter is periodically sampled and not 100% tested.

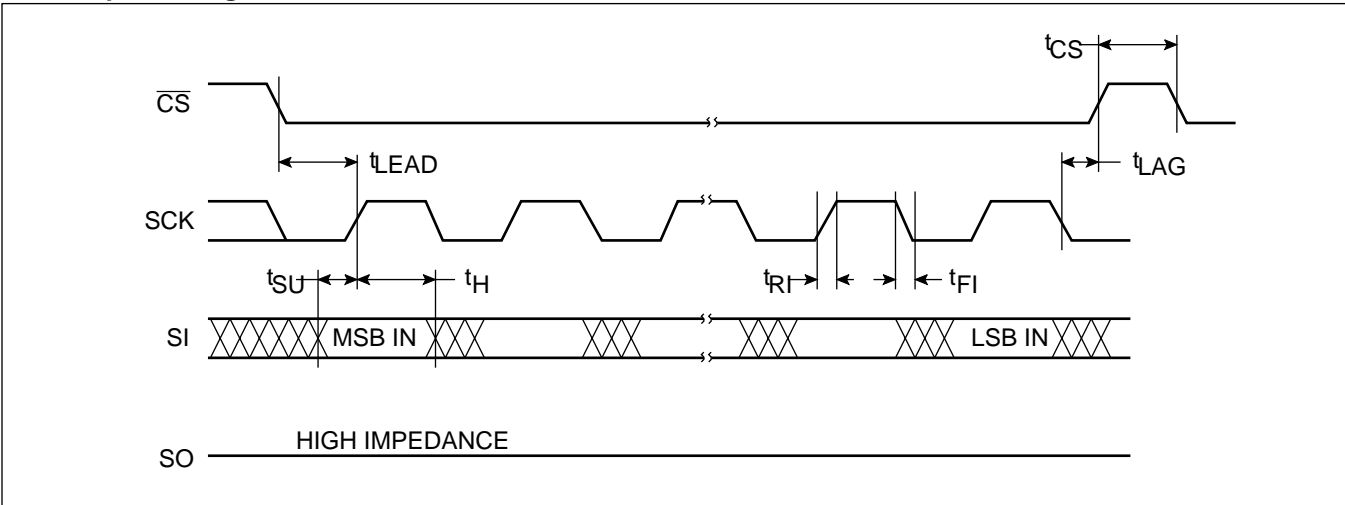
(4)  $t_{WC}$  is the time from the rising edge of  $\overline{CS}$  after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

# X5043/X5045

## Serial Output Timing



## Serial Input Timing

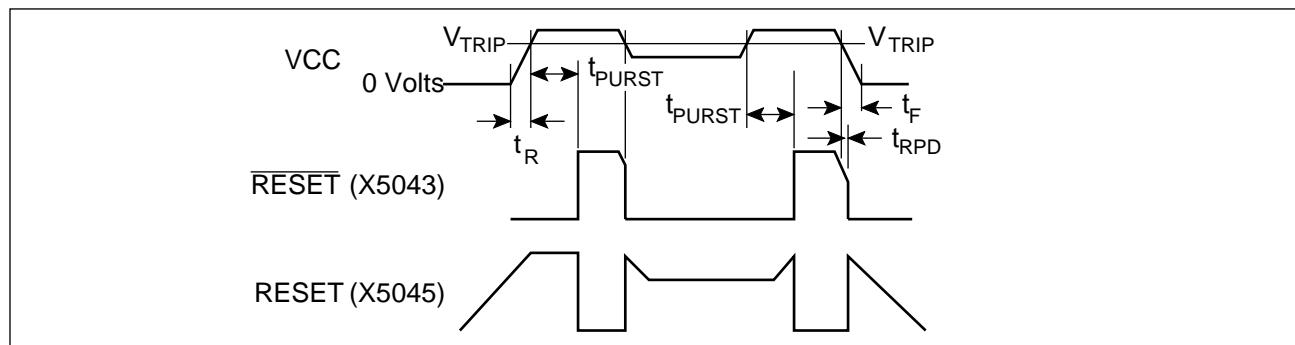


## Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

## X5043/X5045

### Power-Up and Power-Down Timing

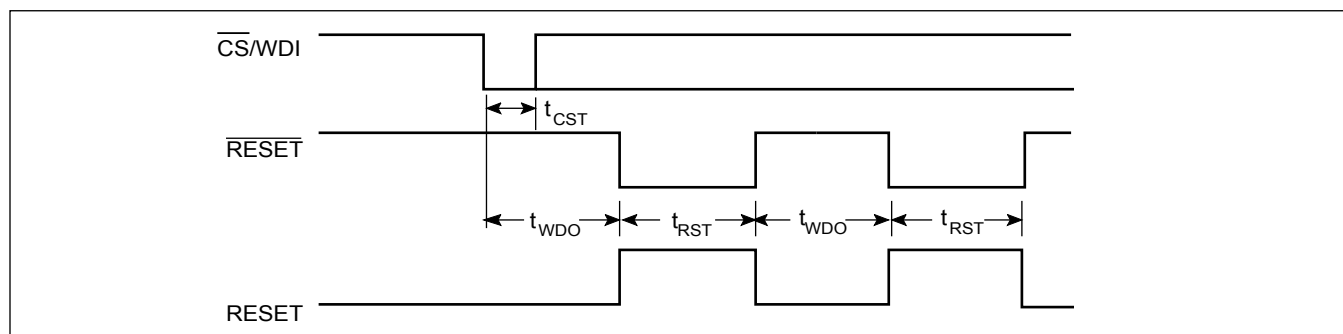


### RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{TRIP}$	Reset Trip Point Voltage, (-4.5A)	4.5	4.62	4.75	V
	Reset Trip Point Voltage, (Blank)	4.25	4.38	4.5	V
	Reset Trip Point Voltage, (-2.7A)	2.85	2.92	3.0	V
	Reset Trip Point Voltage, (-2.7)	2.55	2.62	2.7	V
	Reset Trip Point Voltage, (-1.8)	1.7	1.75	1.8	V
$t_{PURST}$	Power-up Reset Timeout	100	200	400	ms
$t_{RPD}^{(5)}$	$V_{CC}$ Detect to Reset/Output			500	ns
$t_F^{(5)}$	$V_{CC}$ Fall Time	10			$\mu$ s
$t_R^{(5)}$	$V_{CC}$ Rise Time	0.1			ns
$V_{RVALID}$	Reset Valid $V_{CC}$	1			V

**Notes:** (5) This parameter is periodically sampled and not 100% tested.

### $\overline{CS}/WDI$ vs. RESET/RESET Timing

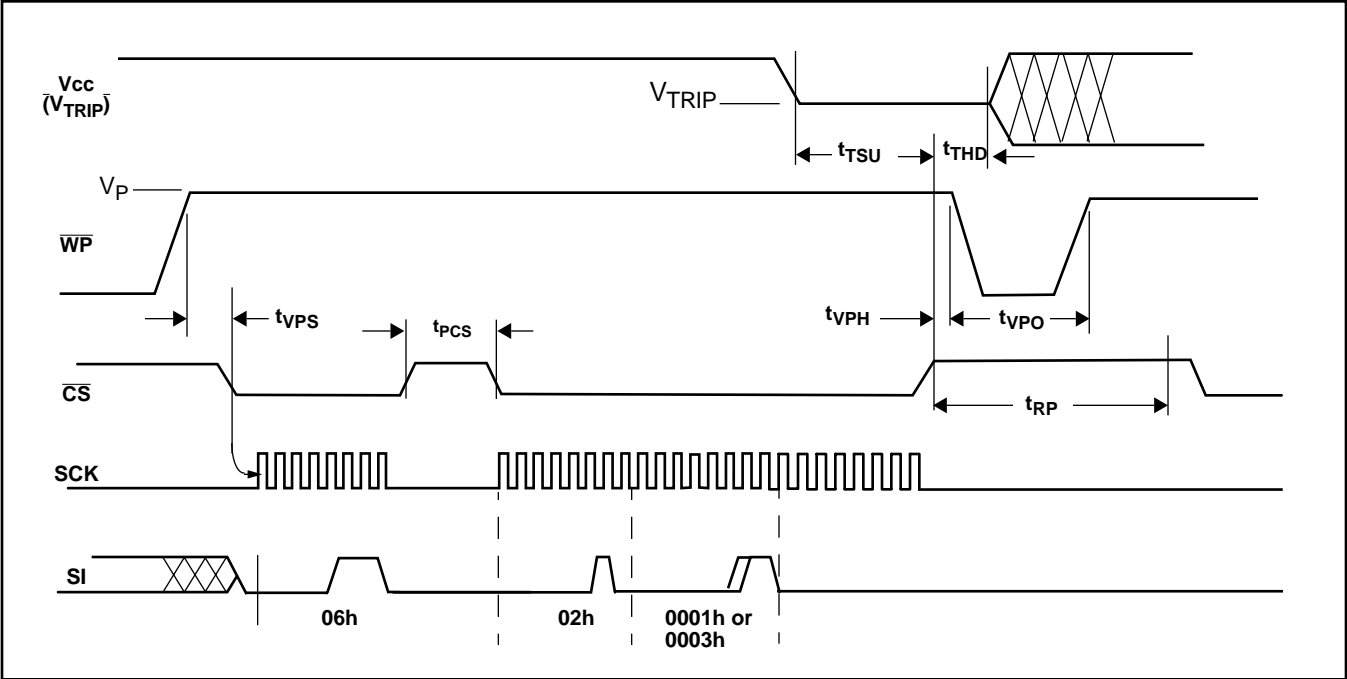


### RESET/RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{WDO}$	Watchdog Timeout Period, WD1 = 1, WD0 = 0	100	200	300	ms
	WD1 = 0, WD0 = 1	450	600	800	ms
	WD1 = 0, WD0 = 0	1	1.4	2	sec
$t_{CST}$	$\overline{CS}$ Pulse Width to Reset the Watchdog	400			ns
$t_{RST}$	Reset Timeout	100	200	400	ms

# X5043/X5045

**V<sub>TRIP</sub> Programming Timing Diagram**



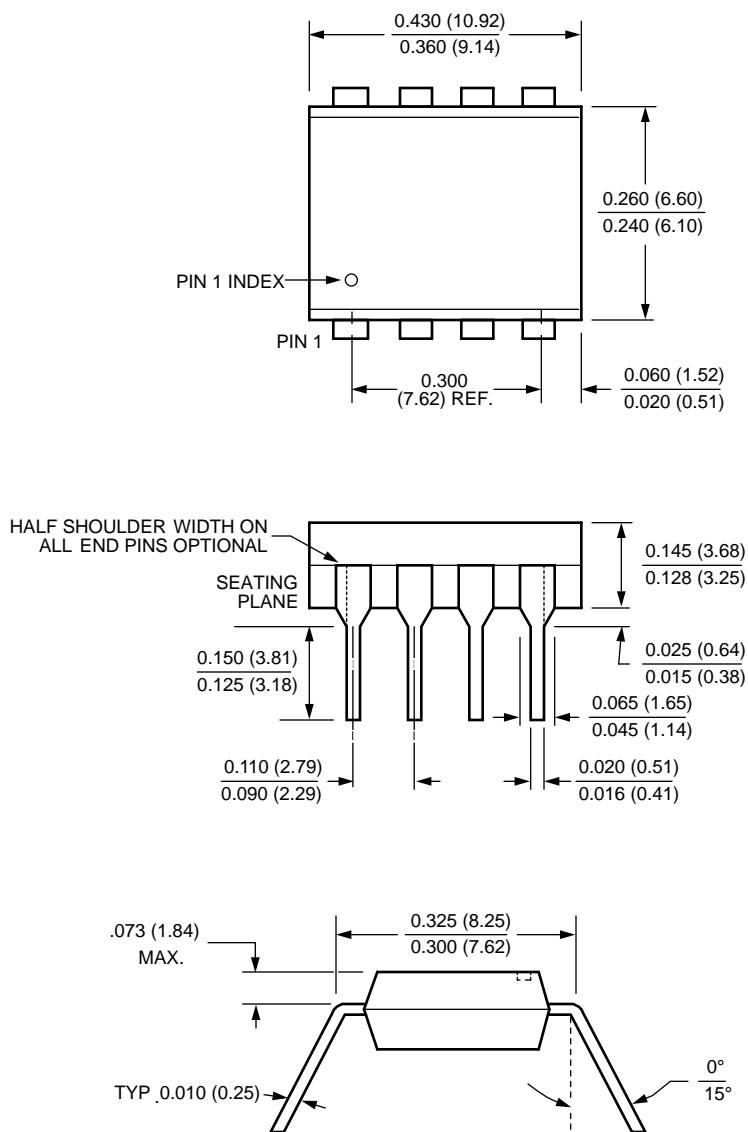
## X5043/X5045

### V<sub>TRIP</sub> Programming Parameters

Parameter	Description	Min	Max	Units
t <sub>VPS</sub>	V <sub>TRIP</sub> Program Enable Voltage Setup time	1		μs
t <sub>VPH</sub>	V <sub>TRIP</sub> Program Enable Voltage Hold time	1		μs
t <sub>PCS</sub>	V <sub>TRIP</sub> Programming $\overline{CS}$ inactive time	1		μs
t <sub>TSU</sub>	V <sub>TRIP</sub> Setup time	1		μs
t <sub>THD</sub>	V <sub>TRIP</sub> Hold (stable) time	10		ms
t <sub>WC</sub>	V <sub>TRIP</sub> Write Cycle Time		10	ms
t <sub>VPO</sub>	V <sub>TRIP</sub> Program Enable Voltage Off time (Between successive adjustments)	0		us
t <sub>RP</sub>	V <sub>TRIP</sub> Program Recovery Period (Between successive adjustments)	10		ms
V <sub>P</sub>	Programming Voltage	15	18	V
V <sub>TRAN</sub>	V <sub>TRIP</sub> Programmed Voltage Range	1.7	5.0	V
V <sub>ta1</sub>	Initial V <sub>TRIP</sub> Program Voltage accuracy (V <sub>cc</sub> applied - V <sub>TRIP</sub> ) (Programmed at 25°C.)	-0.1	+0.4	V
V <sub>ta2</sub>	Subsequent V <sub>TRIP</sub> Program Voltage accuracy [(V <sub>cc</sub> applied - V <sub>ta1</sub> ) - V <sub>TRIP</sub> . Programmed at 25°C.)	-25	+25	mV
V <sub>tr</sub>	V <sub>TRIP</sub> Program Voltage repeatability (Successive program operations. Programmed at 25°C.)	-25	+25	mV
V <sub>tv</sub>	V <sub>TRIP</sub> Program variation after programming (0-75°C). (Programmed at 25°C.)	-25	+25	mV

V<sub>TRIP</sub> Programming parameters are periodically sampled and are not 100% Tested.

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

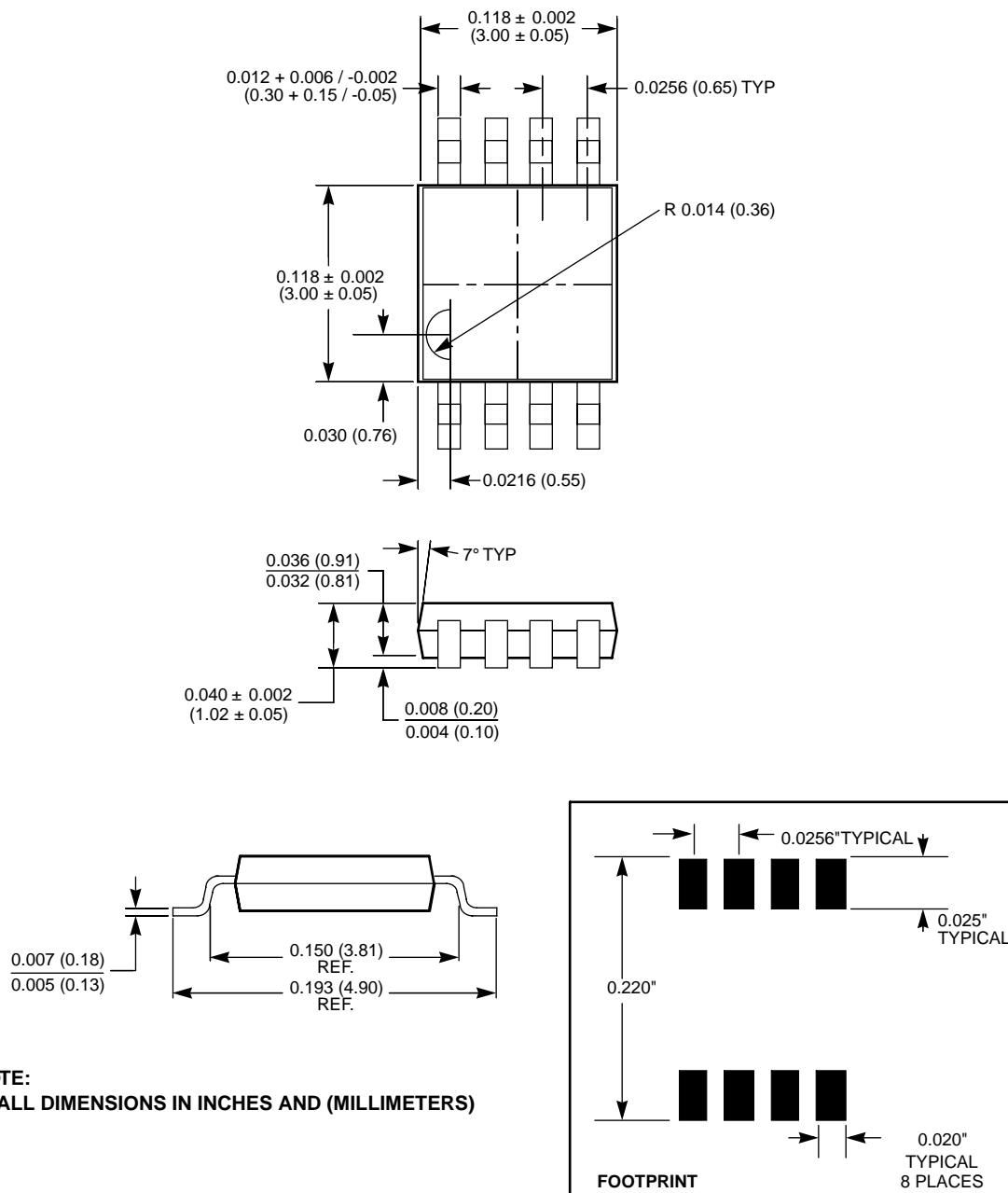


NOTE:

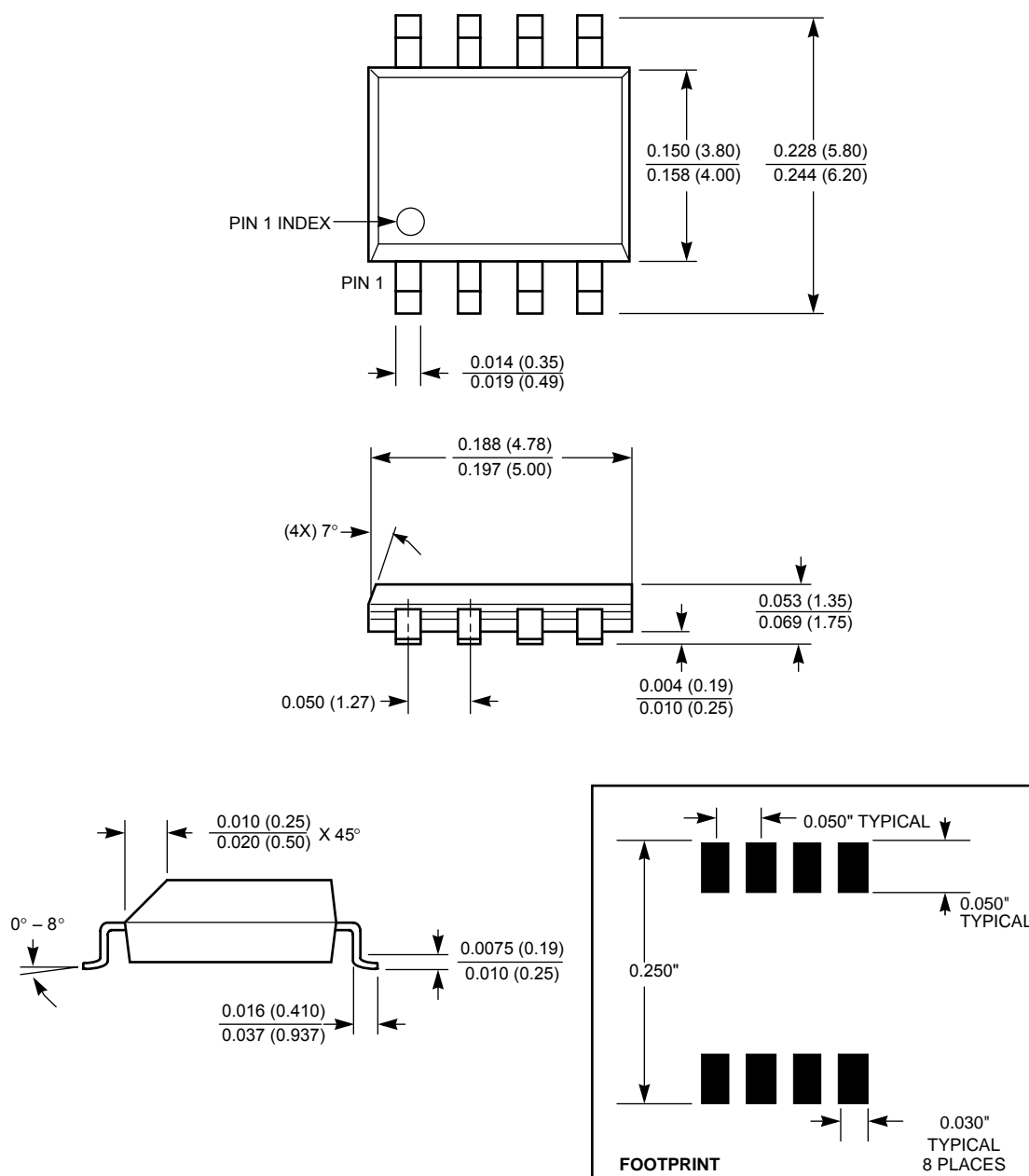
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH



**8-LEAD MINIATURE SMALL OUTLINE GULL WING PACKAGE TYPE M**



## 8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

## X5043/X5045

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### Ordering Information

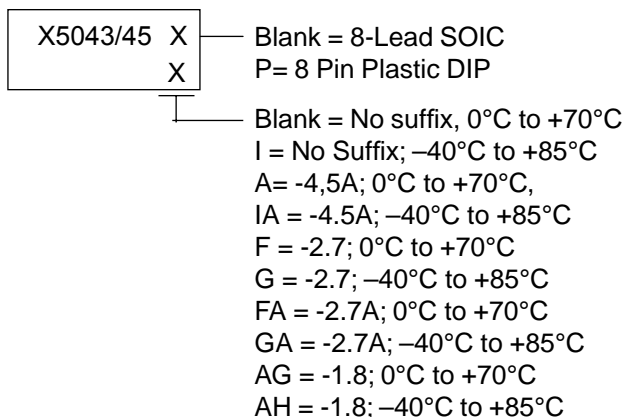
Vcc Range	Vtrip Range	Package	Operating Temperature Range	PART NUMBER RESET (Active LOW)	PART NUMBER RESET (Active HIGH)
4.5-5.5V	4.5.4.75	8 pin PDIP	-40°C - 85°C	X5043PI-4.5A	X5045PI-4.5A
		8L SOIC	-40°C - 85°C	X5043S8I-4.5A	X5045S8I-4.5A
		8L MSOP	-40°C - 85°C	X5043M8I-4.5A	X5045M8I-4.5A
	4.25.4.5	8 pin PDIP	-40°C - 85°C	X5043PI	X5045PI
		8L SOIC	0°C - 70°C	X5043S8	X5045S8
			-40°C - 85°C	X5043S8I	X5045S8I
		8L MSOP	-40°C - 85°C	X5043M8I	X5045M8I
2.7-5.5V	2.85-3.0	8L PDIP	-40°C - 85°C	X5043PI-2.7A	X5045PI-2.7A
		8L SOIC	-40°C - 85°C	X5043S8I-2.7A	X5045S8I-2.7A
		8L MSOP	-40°C - 85°C	X5043M8I-2.7A	X5045M8I-2.7A
	2.55-2.7	8 pin PDIP	-40°C - 85°C	X5043PI	X5045PI
		8L SOIC	0°C - 70°C	X5043S8-2.7	X5045S8-2.7
			-40°C - 85°C	X5043S8I-2.7	X5045S8I-2.7
		8L MSOP	-40°C - 85°C	X5043M8I-2.7	X5045M8I-2.7
1.8-3.6V	1.7-1.8V	8L SOIC	-40°C - 85°C	X5043M8I-1.8	X5045M8I-1.8
		8L MSOP	-40°C - 85°C	X5043M8I-1.8	X5045M8I-1.8

# X5043/X5045

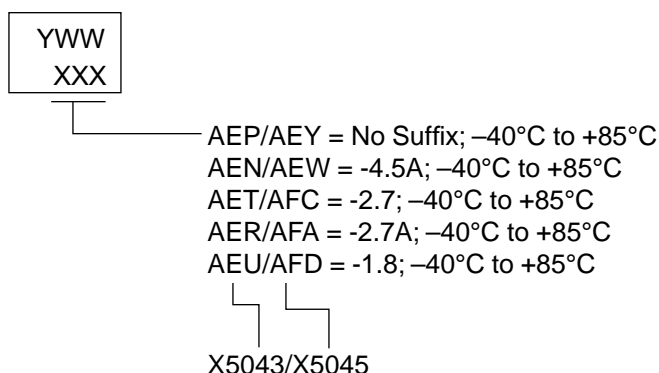
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## Part Mark Information

### PDIP/SOIC



### MSOP



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.